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# Emulation of the AN/UYK-20 tactical data computer on the Burroughs D-machine

Anzelmo, Ralph Harry; Kaye, Theodore Lawrence

Monterey, California. Naval Postgraduate School

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# NAVAL POSTGRADUATE SCHOOL

## Monterey, California



# THESIS

EMULATION OF THE AN/UJK-20  
TACTICAL DATA COMPUTER  
ON THE BURROUGHS D-MACHINE

by

Ralph Harry Anzelmo  
and  
Theodore Lawrence Kaye

March 1977

Thesis Advisor:

L. V. Rich

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20. (cont.)

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Emulation  
of the  
AN/UYK-20  
Tactical Data Computer  
on the  
Burroughs D-machine

by

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Submitted in partial fulfillment of the  
requirements for the degree of

MASTER OF SCIENCE IN COMPUTER SCIENCE

from the

NAVAL POSTGRADUATE SCHOOL  
MARCH 1977

---



## ABSTRACT

A representation of the Univac AN/UYK-20 computer system has been emulated on the Burroughs D Interpreter-Based System. The entire AN/UYK-20 instruction repertoire has been emulated with the exception of the 'math pac' option (floating point arithmetic and cordic functions), clock and interrupt codes, and input/output operation codes. Modular design with extensive documentation has been implemented throughout program development allowing for ease of modification and further extensions to the existing emulation. Emulation and the hardware architecture of the AN/UYK-20 and the Burroughs D-machine, are discussed in conjunction with the AN/UYK-20 emulation itself. Methods of testing and debugging, sample test programs and recommendations for continued design modifications to the emulation are presented.



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## I. INTRODUCTION

### A. STATEMENT OF THE PROBLEM

The Navy has been challenged with maintaining the newest, most efficient tactical data systems consistent with the continually increasing demands and requirements of the real-time environment. There is an extensive conversion effort required to change from existing systems to newer more sophisticated technology such as the AN/UYK-20. Inherent in upgrading to a new system is the complex software redesign and modification process which is often hindered by the absence of the new computer system.

Unfortunately, the demands of a military installation require software generation prior to implementation of an upgraded computer system. One solution to this problem is to utilize for software development an intermediate computer system which has the capability of emulating the anticipated target machine. This provides a vehicle for software design, development, and testing prior to transitioning to the new system.

Currently, the Naval Postgraduate School (NPS) Computer Science Department maintains a Burroughs Interpreter-Based System known as the Burroughs D-machine. The D-machine is capable of being microprogrammed to emulate any of a myriad



of target machines. It effectively enables students to create their own computer knowing only the machine instruction repertoire for the control unit in the target machine.

The problem presented was to develop a feasible working model of the AN/UYK-20 on the microprogrammable Burroughs D-machine. The project provided an opportunity to obtain practical experience with contemporary hardware and to manipulate writeable control stores to imitate a Navy tactical computer.

## B. APPLICATIONS OF THE AN/UYK-20

The Univac AN/UYK-20 minicomputer is a general purpose militarized digital computer adaptable to numerous tactical applications. The AN/UYK-20 has been successfully utilized in many time-critical, real-time systems including fire control radar, communication controllers, signal processing analyzers for sonar and beacon signals, and numerous weapons control systems. A subsequent chapter will be devoted to the technical aspects and internal design of the AN/UYK-20.

Because of its size, ruggedness, and computing capabilities, the AN/UYK-20 has been designated the Navy's standard tactical minicomputer [1b]. It was selected for emulation in order to provide a feasible platform for software development to those military installations either contemplating or in the process of receiving an AN/UYK-20.





A workable emulation would allow military applications such as data reduction, navigation, telemetry, sensor processing, range tracking and logistics to have software packages developed, tested, and modified prior to arrival of the AN/UUK-20. Furthermore, it would permit personnel to become familiar with the machine by providing advanced training, thereby easing the transition phase to the new system.

### C. PROJECT DESIGN OBJECTIVES

Several design techniques were used throughout the development of this project: 1) modularity, 2) structured programming, and 3) extensive documentation. These design features will aid the interested reader as well as simplify any future extensions or modifications to the existing emulation.

Modular design was utilized by creating independent program segments which were individually developed, debugged, and tested. These modules or subroutines provided a strong foundation which were readily modified throughout the entire programming effort. Conceptually, the emulation was divided into relatively small entities which were further reduced to program segments rarely exceeding one page in length.

Structured programming was demonstrated by utilizing a limited number of control flow structures and maintaining a common logical design throughout the entire emulation. Comprehensible code held precedence over extremely efficient



code.

In addition to modularity and structured programming, the entire programming endeavor was supplemented with extensive commenting to provide the necessary self-documentation to promote and facilitate program translation, modification, and fusing with the other independent modules. These concepts promoted the extensive team effort required to achieve the research goals. In addition, it will provide ease of program maintenance and modification in the future.



## II. EMULATION

### A. HISTORICAL BACKGROUND

The term microprogramming was first utilized in an article by Professor M. V. Wilkes of the Cambridge University Mathematical Laboratory in 1951 [24]. His paper concentrated on a control section within the computer which, when programmatically controlled, performed register-to-register data transfers sequentially and in parallel for the execution of a single machine instruction. A sequence of operations (microinstructions) required for execution of a machine instruction is considered a microprogram.

Traditionally, the computer has been composed of essentially five components: the arithmetic/logic unit, the control unit, memory or storage, input, and output (Figure II-1). The control section sets the proper conditions for the opening and closing of required gates in the logic network. Historically, the control section has been hardware consisting of a series of decoders and flip-flops along with their associated circuitry. Therefore, every machine instruction had a fixed interpretation which was hardwired within the control unit.

In 1957, Wilke's definition of microprogramming was slightly modified. It was defined as a technique of design-



ing the control circuits of an electronic digital computer to interpret and execute a given set of machine operations as an equivalent set of micro-operations [15].

The hardwired control section can be modified by interchanging ROM modules or other hardware components, by replacing the control section with a programmable (dynamically writeable) control store which in itself is a separate word-organized memory (Figure II-2) or by combining both approaches. A programmable control store allows rapid changes in the machine's instruction repertoire while maintaining maximum design flexibility. The resulting computer system is microprogrammable and capable of storing a series of changeable machine personalities.

The computer control store can thus be modified to allow the execution of machine language programs intended for a variety of machine architectures. This process can be compared to replacing hardware components found in conventionally designed computer systems. The primary advantage of microprogrammed logic is the capability to perform various control sequences without hardware modifications. The process through which the hardware components of one machine (host) are made to imitate the specific hardware characteristics of another machine (target) is known as emulation.





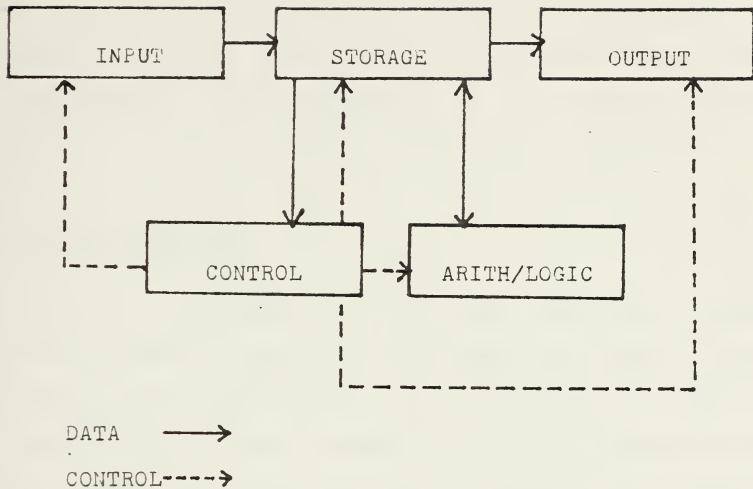


Figure II-1 (11)

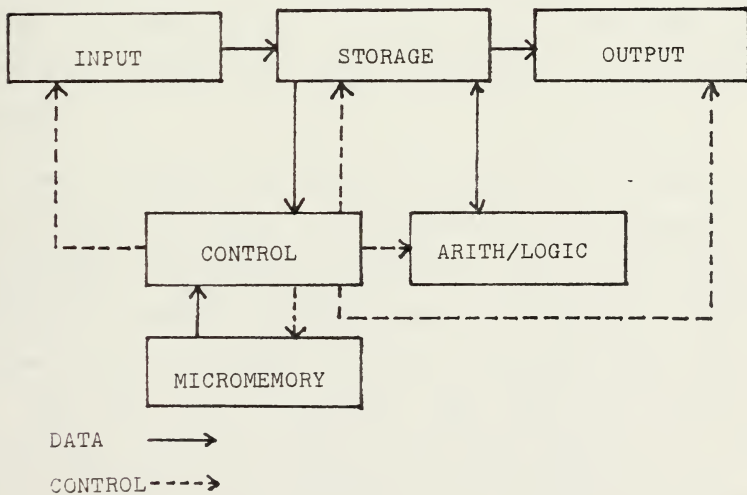


Figure II-2



Emulation allows the computer scientist to create various machine architectures from a single microprogrammable host. The complete set of microprograms (firmware) and the necessary hardware, as well as the required software, added to one computer system enabling it to execute programs designed for another system is known as an emulator.

## B. MICROPROGRAMMING

Computer manufacturers have made available numerous microprogrammable machines which permit the user to tailor his instruction repertoire to meet the needs of his particular application. Some examples of microprogrammable computer systems are the Burroughs D-machine, the Nanodata QM-1, the Varian 73, the Standard Logic CASH-8, or the Hewlett-Packard 2100. These microprogrammable systems provide the benefits of flexibility, lower system costs and a systematic approach to system design if utilized effectively.

When a manufacturer designs a dynamically writeable control store, the amount of parallelism to be allowed must be determined. Parallelism is defined to be the simultaneous control of numerous hardware resources. There are basically three forms of control: vertical, horizontal, and residual. In vertical microprogramming, each instruction controls a single operation with program flow being sequential, unless the instruction was a conditional or unconditional branch. By contrast, a horizontally microprogrammed machine is



programmed via instructions which simultaneously control multiple resources including condition testing and microinstruction sequencing.

Horizontal microinstructions usually are not encoded which means each bit controls one machine resource or operation. They usually have a wider word than vertical instructions and consequently consume more memory. Vertical instructions are usually encoded with one or two levels. Encoding means the value of a control field in the microinstruction is a binary code specifying which resource or operation is to be performed. The horizontal microinstructions have the potential of being much more efficient resource managers and consequently are more difficult to optimally design than their vertical counterparts.

Combining the attributes of horizontal and vertical microprogramming results in residual control. This method saves memory by using vertical microinstructions while simultaneously controlling multiple parallel resources via setup registers.

Microinstruction implementation severely effects the speed of microprogram execution. In serial implementation, one microinstruction is fetched and fully executed prior to fetching the next instruction. This technique offers the advantage of logical simplicity while suffering from lack of efficiency since it consumes the maximum amount of time.

'Parallel' implementation permits fetching of the next



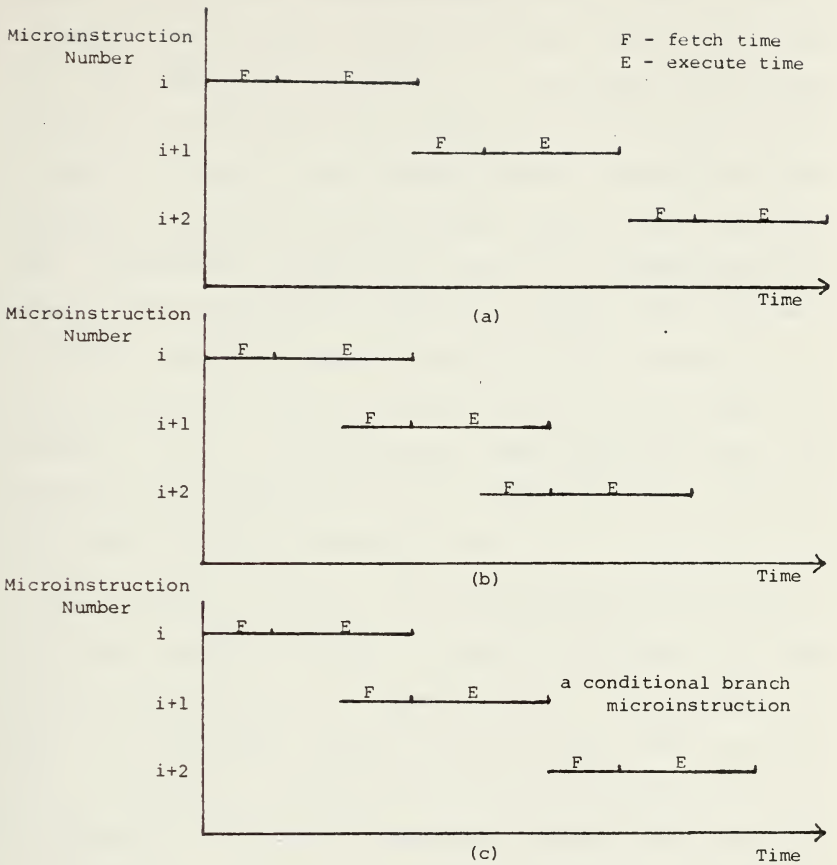
instruction before termination of the previous instruction. The obvious advantage is execution speed which is of utmost importance when emulating another machine (Figure II-3) [2].

Another significant microprogramming characteristic is the number of phases used in the execution of each microinstruction. A monophasic system means there are no subdivisions of the basic clock pulse and consequently each microinstruction is controlled by the transmission of the leading edge of a clock cycle. In a polyphase implementation scheme, the basic clock cycle is subdivided into minor phases which are independently generated via hardware. Although polyphase operations are more complex and require complicated control, they do permit faster resource manipulation when they are efficiently coded by allowing multiple operations to be performed during the same phase(s).

The microprogrammability of a given computer and the capabilities of its associated microprogramming language are directly effected by the the presence or absence of each of the alternative microprogramming characteristics described above. The microprogramming language spectrum ranges from the lowest level or microlanguage through the assembly languages to the high level procedural languages.







- (a) Serial fetch and execute.
- (b) Parallel fetch and execute.
- (c) Combined serial-parallel where next address depends on conditions in present cycle.

Figure II-3 [2]



The problems of microprogramming can be significantly reduced if suitable software support exists and is readily available. This support is usually in the form of simulators and debuggers. Typically, a simulator provides an alternative to assembly level coding by permitting the user to code in a higher level language and yet achieve the same results at the expense of some added memory and execution time. Debuggers are extremely useful in the developmental stages of microprogramming especially for new and experimental system design. Debuggers permit dynamic access to the machine status and register contents at the instant they are employed, i.e. a trace feature. Some debuggers offer the opportunity of assembling in-line. This option can drastically reduce required debugging time.

The primary application of microprogramming is to implement the necessary control structure required for the analysis and execution of machine level instructions by means of programmed control stores rather than hardwired logic. Therefore, a dynamically microprogrammable computer can provide a software development system which can be a cost-effective approach to experimentation with potential candidates for replacement computer systems or the design of completely new systems to fit the needs of unique applications.



## C. THE GOALS OF EMULATION

A well-designed emulation can provide an opportunity to experiment and create software for new computer systems before the actual hardware is available. The utilization of an emulator can almost eliminate reprogramming, consequently smoothing the system transition period. In addition, emulation has provided a workable model of new systems under consideration for procurement, providing a much more detailed cost-benefit analysis of system conversion.

Furthermore, it is often economically sound to emulate a second generation computer with a third generation system. This provides growth to a contemporary system while fulfilling the requirements of the past in a cost-effective manner. However, this can be a disadvantage if the programming staff uses the emulation as a link to the old system and consequently fails to take advantage of the attributes of the new system.

## D. EMULATION VERSUS SIMULATION

To accomplish the emulation objectives, certain design features must be incorporated into an emulation. Naturally, execution time and allocated memory are the two foremost considerations. Traditionally, the concept of mimicking another computer has been accomplished by either a simulator or an emulator, two concepts often confused with one another.



A simulator is a series of high level language (HLL) or assembly language statements which individually do not behave like the target machine instructions. The host machine executes its own native instructions in order to imitate the target machine operations. Consequently, simulation is a rather slow technique because it requires an intermediate translation. In addition, simulation of certain instructions such as bit manipulation and shifting operations can require an enormous amount of intermediate code generation demanding a significantly larger memory allocation.

An emulator is a microprogram that is executed on the host machine, performing machine instructions of the target machine. Since an emulator accepts the binary object code of the target machine and directly executes these instructions, it can be extremely efficient in terms of time and space requirements. The execution time of an emulation is dependent upon many factors: clock rates of the two machines, frequency of memory references, high speed shifting compatibility, required register mapping between target and host machines, bit manipulation capability of the two machines, condition code selection and testing, flexible data path selection capability, interrupt similarities, input/output compatibility, and microprogramming efficiency. If the hardware features between target and host machines are extremely compatible and highly efficient microprogramming has been employed, an emulation performance ratio (host





to target) of nearly one to one can be attained. This emulation performance ratio (EPR) has been demonstrated by the emulation of the SKC-2070 on the Nanodata QM-1 computer. It is possible to achieve an EPR better than one to one under ideal situations, when the host machine has a much faster internal operation execution rate [1].

Several distinct advantages can be realized using emulation as compared to simulation. The execution speed is significantly better by at least an order of magnitude. The target machine representation in firmware is closer to the actual hardware design and total access to the lowest machine level is achievable. Perhaps most noteworthy, emulation provides the opportunity to rapidly create test beds for numerous machine architectures and provide a basis for new system development.

#### E. EMULATION TECHNIQUES

Traditionally, there have been three approaches for emulating machine instructions: 1) hardware or firmware assistance to a software simulation as demonstrated by the IBM 360/b5 emulation of the IBM 7090, 2) independent host system hardware or firmware which provides for complete execution of the target machine's instruction repertoire of which the Burroughs D-machine emulation of the AN/UYK-20 is an example, and 3) an auxiliary processor which is operated in conjunction with the host machine to execute target machine instructions [14].



Software-controlled emulation is usually characterized by categorizing the target machine instructions into three distinct classes: easily emulated instructions, complex instructions not readily emulated, and those instructions not deemed necessary for the desired application. Instruction usage is significant in this classification process. Each class of instructions becomes a candidate for direct hardware or firmware implementation. The first emulated function in this approach is usually the fetch and analysis operation. After the instruction is analyzed, the appropriate opcode subfunction can be executed.

An alternative emulation technique is the firmware-controlled method. This approach is identified by having system control reside completely in firmware or hardware during the emulation process. All instructions are executed on the host machine as if they were indigenous to the target machine. This method is much more efficient than the software-controlled technique; however, it is more expensive and the cost differential is directly related to the required performance level. Performance is dependent upon the number of required data paths, arithmetic units, and other additional logic circuitry which must supplement the host machine architecture.

Upon entering the emulation mode in a firmware-controlled emulator, the machine performs like the target machine until encountering an exit situation. There exists three exit modes: 1) priority interrupt, 2) not implemented



instruction, and 3) deliberate exit because of a debugging routine.

The third emulation technique consists of utilizing auxiliary hardware electronically attached to the host computer for the sole purpose of executing target machine instructions. In effect, a target machine is composed of host machine hardware with the necessary additional components required to create an effective emulator.

#### F. EMULATION HARDWARE

The development of writeable control stores and microprogramming techniques have significantly influenced computer design. This section will describe some of the available dynamically microprogrammable hardware (Figure II-4).

The Hewlett-Packard 2100 is a general purpose minicomputer. It has a unique control store divided into two segments. One section is ROM and the other section is user programmable. The machine is vertically microprogrammed using a standard 80 instruction machine language repertoire. A debugger and assembler assist the user in microprogram development [2].

The Standard Logic CASH-8 is a high speed digital controller with a separate control store. It consists of 16 general purpose registers and an accumulator. The CASH-8 is vertically microprogrammed but does not support any language



above microlanguage [2].

The Varian 73 is a general purpose minicomputer that has a 150 instruction set. The horizontal microinstruction consists of 64 bits with 25 fields, some of which indicate register transfers, ALU operations, shifting, control store addressing, condition testing, I/O control and memory operations. The Varian 73 contains both a ROM control store and a writeable control store loadable from main memory. A microprogram assembler and interactive simulator are available [2].

The Nanodata QM-1 is unique in that it contains both a control store and a nanostore which are both loaded under user program control. The 18-bit vertical microinstructions are stored in the control store, fetched and then interpreted under nanoprogram control. A horizontal nanoinstruction is 360 bits which is subdivided into five 72-bit vectors. Assemblers for both microprograms and nanoprograms are available [2].

The previously described machines represent a small sample of the available microprogrammable computer architectures. The availability and flexibility of these computer systems has stimulated demand for these devices. Consequently, hardware manufacturers have been compelled to produce writeable control store equipment to satiate the needs of the computer market.





CONTROL STORE  
REALIZATION

MICROPROGRAMMED

USER MICROPROGRAMMABLE

Main Memory

• IBM S/360 Model 25  
IBM S/370

• Burroughs B1700

• Nanodata QM-1

Interdata 85 •

•  
Varian 73

Fast Read/  
Fast Write

•  
Hewlett Packard 2100

•  
DSC Meta 4

ROM

• Interdata 80  
IBM S/360 Models 30,40,50,65  
RCA Spectra 70 Model 45

None

Preparation of  
User Microprograms

Provision of  
Translator or  
Simulator

SUPPORT AVAILABLE TO USERS

Note: Relative microprogrammability is the distance from the origin to the machine point in two space.

Figure II-4 [2]



### III. AN/UYK-20 ARCHITECTURE

Constructing an efficient emulation requires a precise understanding of the architecture and performance characteristics of the machine being emulated. An emulation must attempt to match the target machine's features and maintain its flexibility of hardware design as closely as possible. Although it is not required, an operational demonstration of the emulated machine can solve many emulation questions.

In emulating the AN/UYK-20, architecture and performance criteria were derived from technical publications, since an actual machine was unavailable. When inconsistencies appeared in the documentation, specific questions were posed to a UNIVAC field engineer, who often tested programs on the AN/UYK-20 to resolve inconsistencies. Documentation coupled with an expert consultant provided sufficient information for emulating the AN/UYK-20 successfully.

The intent of this chapter is to outline those features of the AN/UYK-20 significant to the emulation. A detailed hardware description can be found in Refs. 20, 22, 28.



## A. HARDWARE DESIGN

The AN/UYSK-20 was designed for the Navy to fulfill the requirements for small or medium size general purpose data processing in shipboard, mobile shelter, or other military environments. Sperry Univac incorporated minicomputer technology in constructing the AN/UYSK-20, including MSI circuitry design, microprogrammed control, memory modularity, and asynchronous or synchronous input/output channels.

The AN/UYSK-20 had to be extremely flexible in its applications, offering a wide range of configuration possibilities which were derivatives of the basic design. Modularity, a concept highly desirable in a military environment, was achieved by offering options that could be easily added using printed circuit cards and/or memory modules.

The AN/UYSK-20 can accommodate up to eight 8K, sixteen-bit word boards of magnetic core storage with an access time of 750 nanoseconds. The central processor is controlled by a programmable micromemory which can be expanded by an additional 512 words. The microprogram controller is programmed at the factory, but the additional micromemory option is user defined. Both sections of micromemory are programmed using fusible links, and once programmed they are completely static (Figure III-1).

A memory interface is responsible for the transfer of data to memory from the central processor (CP) and input/output controller (IOC). Both the IOC and the CP are



capable of accessing all of memory (65,536 words maximum). The addition of direct memory access (DMA) provides a second memory interface and an additional access port which is connected to each of the two 32K memory segments.

The input/output controller permits the central processor to communicate with the external devices without interfering with program execution. The IOC has a maximum of 16 parallel or serial channels. Parallel data transfer takes place asynchronously using 8-bit, 16-bit, or 32-bit transfers. Serial interfaces are either synchronous or asynchronous, with word-to-serial or serial-to-word conversions occurring in the IOC. The IOC and CP compete for memory access through the memory interface with priority given to the IOC in the event of a simultaneous request. The IOC is permanently assigned several memory addresses for command word and interrupt word storage.

The addressable high-speed registers available in the AN/UYK-20 include the program address register (P-register), two 16-bit status registers (SR1 and SR2), a real-time clock register (32-bits), a monitor clock register (16-bits), and a set of sixteen 16-bit general registers. An additional stack of 16 general registers is an available hardware option.

The sixteen general registers were included to enhance the speed and performance of the AN/UYK-20, allowing most programs to use a great proportion of register-to-register





instructions. These general registers can be used as accumulators for arithmetic, shift, or logical functions, as index registers, or as temporary storage locations. The second set of general registers can be readily employed via a status bit. This status bit designates which general register stack is to be utilized. The duplicate set of general registers yields dividends in a multi-task or heavy-interrupt processing environment. This additional register set can be used to provide high-speed temporary storage, thus avoiding slower main memory storage of working variables.

The two 16-bit status registers and the program address register represent the machine status of the AN/UYK-20. When these registers are collectively referenced, they are called the program status word (48-bit PSW). The P-register indicates the next instruction to be executed. This instruction may be a 16-bit single-word instruction or a 32-bit double-word instruction. Program control can be modified by using an instruction which manipulates the contents of the P-register.

Status register 1 contains bit information concerning condition code settings, overflow, and carry bits, interrupt codes, and numerous other machine indications (Figure III-2).



AN/UJK-20 FUNCTIONAL ARCHITECTURE

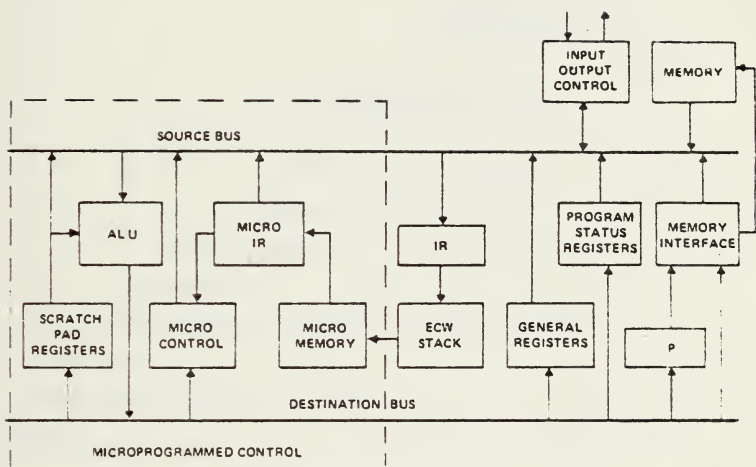
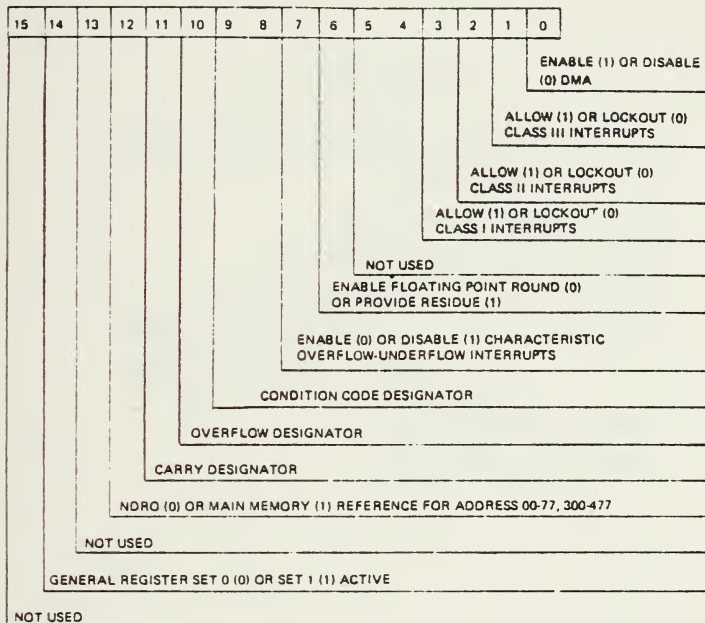


Figure III-1 [22]



STATUS REGISTER 1



CONDITION CODES

SR BITS 8 and 9	ARITHMETIC	COMPARE
00	0	$(R_a) = (R_m)$ or (Y)
01	>0 (POS)	$(R_a) > (R_m)$ or (Y)
10	Not Used	Not Used
11	<0 (NEG)	$(R_a) < (R_m)$ or (Y)

Figure III-2 (23)



Status register 2 holds control bits for direct or indirect addressing, and holds interrupt codes. Interrupt processing routines set bits in the interrupt code field corresponding to the IOC interrupt (Figure III-3).

STATUS REGISTER 2

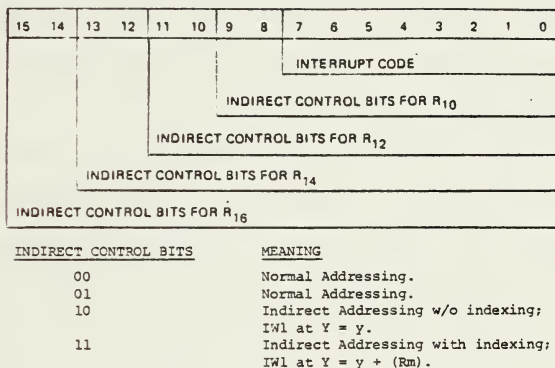


Figure III-3 (23)

The real-time clock and monitor clock registers provide program-controlled interrupt capability which is useful for timing and synchronizing program segments with real-time events. The real-time clock (RTC) is a 32-bit register used as count-up storage while the monitor clock (MON) is a 16-bit count-down register. A one kHz internal oscillator controls the counting speed of both registers. An optional





external clock operating at a frequency up to 50 kHz is also available.

Interrupt processing in the AN/UYK-20 is conducted using a priority level scheme which classifies interrupts into three priority levels (classes). Interrupts within the same class are assigned a priority ranking and a code which identifies which processing routine to execute. During interrupt handling, all interrupts of the same level or lower level are locked out until the CP is completed processing the current interrupt. Higher priority interrupts can override the lockout and cause the CP to honor them first, holding the lower level interrupts in abeyance until higher level interrupt processing is completed. The highest priority interrupts are hardware malfunctions, followed by software interrupts, and at the lowest level, IOC interrupts.

Permanent locations in memory corresponding to each interrupt class hold the PSW and RTC when an interrupt is being honored. Likewise, other permanent memory addresses assigned to each interrupt class hold the appropriate interrupt routine entrance location to be loaded into the PSW.

Memory addressing is accomplished using 64 page address registers which separate memory into 1024-word pages. Absolute addresses are formed by isolating the upper six bits of the relative address to find the page address register number, and then concatenating the lower six bits of the



page address register contents with the lower ten bits of the relative address (Figure III-4). Any operation that stores into memory sets the most significant bit of the page address register used in generating the address.

Some additional hardware features of the AN/UYK-20 are those functions available on the maintenance panel of the machine itself. These include a breakpoint feature which allows an operator to insert from the panel an address which causes the AN/UYK-20 to stop execution when the selected address is referenced. Other available toggles allow halting execution programmatically using Key 1 or Key 2 on the maintenance panel. These additional hardware features are useful debugging tools.



MEMORY ADDRESS GENERATION

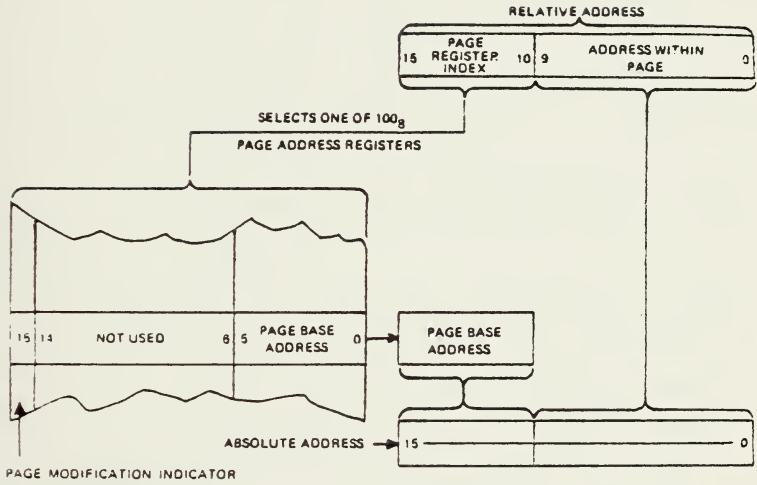


Figure III-4 [22]



## B. INSTRUCTION FORMATS AND REPERTOIRE

### 1. Repertoire of Instructions

The AN/UYK-20 instruction set is composed of nearly 260 separate instructions designed to be both versatile and comprehensive. Both single-word (16-bit) and double-word (32-bit) instructions are available. Some of these instructions are specifically designed to meet the requirements of a real-time environment. A few sample instructions include:

- a. Local jump - used to facilitate loops, saving several steps in program execution.
- b. Reverse register - used in a communication environment when data is received in one sequence but must be transmitted in reverse sequence.
- c. Set bit, clear bit, and test bit - used to test individual bits in registers saving considerable execution time in programs that communicate via flags and status words.

Additional flexibility is provided when the 'math pac' hardware option is included in the AN/UYK-20 configuration. Some 33 additional opcodes are added to the instruction set in order to increase the computational capabilities of the machine. An instruction for square root, double precision multiply/divide instructions, as well as hardware trigonometric and hyperbolic functions which utilize coordinate conversion algorithms (cordic) are included.





Single-word instructions are generally employed when manipulating operands in high-speed registers. Double-word instructions are used in operations involving direct or indirect addressing with or without indexing, or supplying 16-bit constants to programs. Typical instruction speeds for a single-word versus a double-word instruction are:

	SINGLE-WORD	DOUBLE-WORD
ADD	.75 - 1.5 usec	1.5 - 2.25 usec
LOAD	.75 - 1.5 usec	1.5 - 2.25 usec
MULTIPLY	3.8 - 4.0 usec	4.4 - 4.6 usec
DIVIDE	6.8 - 7.0 usec	7.4 - 7.5 usec

Nearly all instructions affect condition bits in status register 1. The AN/UUK-20 sets these bits as a result of two types of operations. Most instructions that do not involve compare logic are categorized as arithmetic instructions. When the result of the arithmetic operation is determined and is about to be stored in memory or a register, a condition code is set indicating whether the result is positive, negative, or zero. Compare instructions set the condition bits based on a greater than, less than, or equal to comparison of two registers or a register and the contents of a memory address.

Two other bits in SR1 are set as a result of computational or shifting instructions. The overflow designator is set whenever an arithmetic or shift operation requires more bits than are provided for in a register (16 bits).



The carry designator is set when an arithmetic operator generates a carry beyond the most significant bit of the register.

The AN/UUK-20 allows five different types of operand formats: single-length, byte, literal, optional floating point, and double-length. Single-length operands are 16-bit values with the sign bit assumed to be in the most significant bit. In arithmetic calculations, the single-length word is assumed to be a two's complement integer. Byte operands are considered 8-bit unsigned integers, and can be the most significant or least significant half-word of a memory location. Literal operands are 4-bit unsigned integers denoted by the 'm' field of a literal type instruction. Floating point operands are formed using two adjacent registers or memory locations with fields containing the sign of the fraction, the characteristic, and 24 bits of the fraction.

Double-length operands are concatenated from two adjacent registers or two adjacent memory addresses. The most significant half of the double-length operand is contained in the low-order register or memory address, and the least significant half in the next sequential register or address. The sign bit for both words resides in the high-order bit position of the most significant half-word and when used in an arithmetic calculation, the double-length operand is treated as a two's complement integer. Instructions involving double-length operands require the low-order



register or memory address to be even, since the adjacent cell address is formed by 'OR'-ing a 1 in the least significant bit of the address.

## 2. Instruction Format

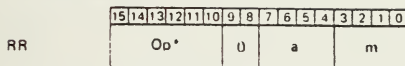
The AN/UYK-20 has five different instruction word formats, designated by two-letter mnemonic codes. These codes are: RR (Register-Register), RL (Register-Literal), RI (Register-Immediate), RK (Register-Constant), and RX (Register-Index). Each of these formats are designated in the instruction word by a combination of the opcode field and the subfunction code. Registers are identified in the 'a' and 'm' fields of the instruction, and are referred to by the notation  $R_a$  and  $R_m$ . The 'v' field is treated as an address or arithmetic constant, depending on the instruction (Figure III-5).

The format RR single-word instructions perform operations involving the registers specified by the 'a' and 'm' fields. No memory references are made to access operands, causing considerable savings in execution time. The 'a' or 'm' field may be used to index special operations on registers.

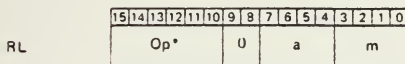
Format RL instructions use a 16-bit instruction word, using one or two general registers. The 'a' designator selects the general register  $R_a$  or register pair  $R_a, R_a + 1$ . The 'm' designator contains the 4-bit literal value which will be used in the instruction.



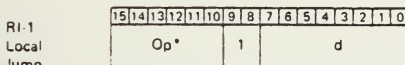
### INSTRUCTION FORMATS



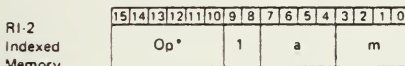
a selects  $R_a$ ; m selects  $R_m$ .



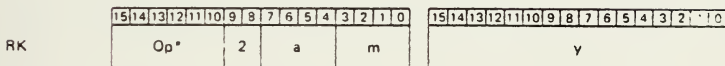
a selects  $R_a$ ; m contains 4-bit constants.



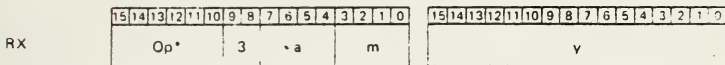
d is signed number of instructions to jump, relative to current position.  
(+ is forward; - is backward)



a selects  $R_a$ , m selects  $R_m$ .  $R_m$  selects memory address.



a selects  $R_a$ ,  $m \neq 0$  selects  $R_m$ ,  $m = 0$  selects 0.  
Operand =  $y + R_m$  or 0.



a selects  $R_a$ ,  $m \neq 0$  selects  $R_m$ ,  $m = 0$  selects 0.  
 $y + R_m$  or 0 selects memory address.

\*Op is operation code

Figure III-5 [23]





RI format single-word instructions are separated into two categories. RI Type 1 instructions are local jump instructions where the P-register is increased or decreased by the 'd' field in the instruction. The 'd' field represents the two's complement deviation value and allows the P-register to be altered a maximum of +177 octal or -200 octal. RI Type 2 instructions involve operations that use the general registers Ra and Rm, and a memory address specified by the contents of Rm.

The format RK instructions contain 32 bits of information. The upper 16-bits contain the operation code and the designator fields. The 'a' field selects the general register Ra, and the 'm' field denotes how the next word, containing 'y', is to be used. If 'm' equals zero, then the effective operand address Y, equals 'y'. If 'm' does not equal zero, then Y is formed by adding the contents of Rm to 'y'.

Format RX are double-word instructions similar to the RK instruction that use direct and indirect addressing techniques determined by the 'm' field. If the 'm' field equals zero, then direct addressing without indexing is employed, with the effective operand address formed from the 'y' field itself. If the 'm' field equals 1 through 7, 11, 13, 15, or 17 (octal), then direct addressing with indexing is employed. The effective operand address is formed by adding the contents of Rm to 'y'. An 'm' field value of 10, 12, 14, or 16 (octal) indicates indirection is to be



employed, and the indirect address control fields in status register 2 contain information which is used to generate the effective operand address or a pair of indirect words. When the control fields equal 0 or 1, then direct addressing with indexing results. If the control field equals 2, then the contents of the first indirect word (IW1) is located at 'y'. Finally, if the control field equals 3, then IW1 is located at 'y' indexed by the contents of Rm. Indirect word format is shown in Figure III-6. Cascaded indirection is possible provided that the indirect words are properly encoded.

Byte addressing is accomplished using RX format instructions. A byte identifier (B) is used to determine which half-word (8-bit) is to be referenced. If B equals 0, then the most significant half-word in address Y is the operand byte. If B equals 1, then the least significant byte at Y is the operand. The least significant bit in the indexing register is used as the byte identifier, and the remaining 15 bits are used as the indexing value for finding Y. Indirect byte operand addressing formulae are included in Figure III-6. The following formulae apply for direct byte operand addressing:

$$m=0, Y=y, \text{ and } B=0$$

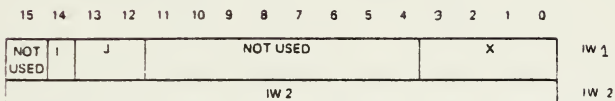
$$m=1-7, 11, 13, 15, \text{ or } 17 \text{ octal}$$

$$Y=y + (Rm)/2 \text{ and } B=\text{LSB of } (Rm)$$



The preceding section has described the fundamentals of the AN/UYK-20 instruction formats. References 21 and 23 should be consulted for further information concerning instruction formats and decoding.

INDIRECT WORD FORMATS



OCTAL J VALUE	ADDRESS DETERMINATION
0	$Y = IW2$ ; if byte mode, upper byte is used.
1	$Y = IW2 + (R_x)$ ; if byte mode, LSB of $R_x$ determines byte. *
2	$Y = IW2 + (R_m)$ ; if byte mode, LSB of $R_m$ determines byte. *
3	$Y = IW2 + (R_{m+1})$ ; if byte mode, LSB of $R_{m+1}$ determines byte. *

I = 0, DIRECT ADDRESSING, OPERAND AT ADDRESS Y

I = 1, CASCADED INDIRECT ADDRESSING, NEW INDIRECT WORD 1 AT ADDRESS Y

\* To determine the operand address when in byte mode, the contents of  $R_x$ , or  $R_m$ , or  $R_{m+1}$  are right shifted 1 bit position and zero filled in the left most position

Figure III-6 (23)



## IV. BURROUGHS D-MACHINE

### A. HARDWARE DESCRIPTION

The microprogramming facility at the Naval Postgraduate School is composed of a Burroughs Interpreter-Based system. This system possesses the characteristic of being dynamically microprogrammable and is designed using a simple building block structure. A typical system is made up of a number of interpreters (processors), main memory modules, and input/output devices, along with a switch interlock device (SWI) controlling data flow on the data bus connecting the interpreters to main memory and peripheral devices. The heart of the system is the interpreter, also referred to as the D-machine.

A D-machine possesses five functional modules: the logic unit (LU), the control unit (CU), the memory unit (MU), nanomemory (NM), and microprogram memory (MPM). The system presently installed in the Computer Science Department combines nanomemory and microprogram memory into one functional unit. The architecture of the D-machine is designed around 8-bit word slices. Word lengths from 8 bits to 64 bits are permissible using the same functional unit (Figure IV-1).





INTERPRETER BLOCK DIAGRAM

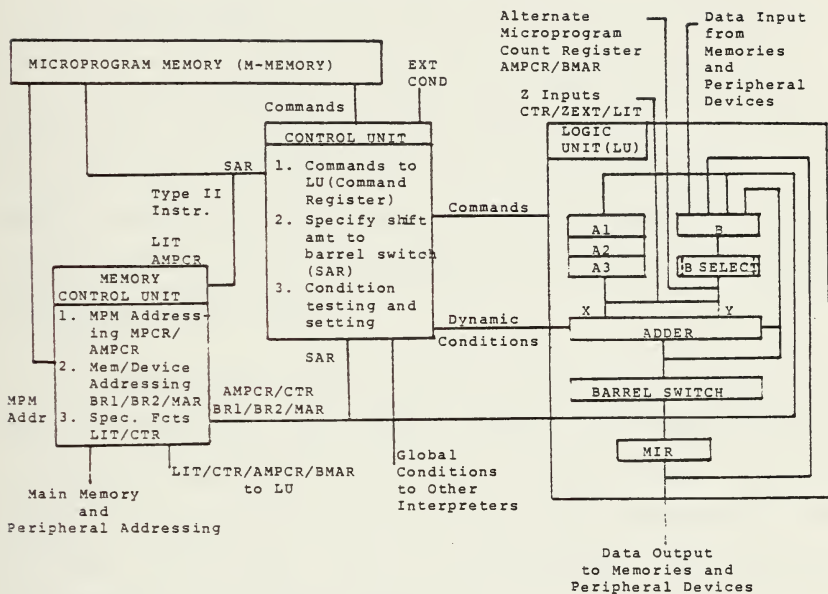


Figure IV-1 (a)



The D-machine used for this thesis has been configured as a 32-bit word processor. Reference 17 provides a thorough and concise description of the architecture of an interpreter-based microprogramming system. Reference 6 details the specifics of D-machine microprogramming which must be thoroughly understood by the programmer.

## 1. Logic Unit

The D-machine's logic unit performs shifting, arithmetic, and logic functions and contains scratch pad registers and data interfaces for the switch interlock. All adder operations are performed using two's complement arithmetic, and shifting is accomplished in a matrix of gates called the barrel switch.

The scratch pad registers A1, A2, and A3 are identical in function. They act as temporary storage registers within the D-machine and serve as primary inputs to the adder. The control unit determines which register will be an input to the adder. Any of the A-registers can receive the output from the barrel switch.

The B register functions as the primary external input interface from the switch interlock. It acts as the second input to the adder and can receive certain direct inputs from the adder's arithmetic operations. The b register can be loaded from any of the following sources:



- a. The barrel switch output.
- b. The adder output.
- c. External data from the switch interlock (or control panel switches).
- d. The memory information register (MIR).
- e. The complements of four bit or eight bit carries.
- f. The barrel switch ORed with the adder, external data from the switch interlock, or MIR.

The output of the B register is filtered prior to gating into the adder. The 'filter' consists of true/complement selection gates which are divided into three sections: the most significant bit, the least significant bit, and all the remaining central bits. The output of this filter is the independent result of these sections and may be either all zeroes, all ones, or the true contents or one's complement of the contents of the respective bits of the B register.

The memory information register is the interface to the switch interlock. MIR functions as a buffer to main memory or to a peripheral device. It is an output destination of the barrel switch and its output can be sent to the B-register or the switch interlock.

The adder in the logic unit performs all arithmetic functions and can be categorized as a version of a carry look-ahead adder. The control unit can gate various combi-



nations of A, B, and Z inputs to the adder. An 'A' input is defined as an input from one of the three scratch pad registers. A 'B' input is the output of the B register's true/complement filter gates. A 'Z' input is an external input to the logic unit and can originate from one of the following sources:

- a. The output of the counter in the memory control unit (MCU) which is gated to the most significant eight bits of the adder with the remaining bits zeroed.
- b. The output of the literal register in the MCU which is gated to the least significant eight bits of the adder with the remaining bits zeroed.
- c. An optional input which is gated into the middle bytes of the adder with the most and least significant bytes zeroed.
- d. The output of the alternate microprogram count register (AMPCCR) in the MCU which is gated into the least significant 12 bits of the adder (13 bits for 8K micromemory machines) with all other bits being zeroed.
- e. All zeroes.

Two inputs, selected from the A, B, or Z sources, are always gated to the adder. These inputs are referred to as X-select and Y-select. An X-select input may be either an A input or a Z input. If it is not specified, it is





assumed to be zero. A valid Y-select has either a B, Z or 1 as its input. Some Z inputs, however, are valid only as Y-select inputs. Any combination of valid X-selects and Y-selects are permissible addends, with an option of adding a one to the least significant bit. For subtraction operations, the value to be subtracted must be a Y-select; the Y-select input is subsequently two's complemented and gated to the adder. All binary Boolean operations between two adder inputs are allowed, and dynamic condition bits for overflow (AOV), all bits true (ABT), and most/least significant bit test (MST/LST) are available to the control unit for testing. Bit testing is a valuable feature for decoding instruction words.

The barrel switch is a matrix of gates that accepts parallel data from the adder and shifts the data any number of places to the left or right with zero fill. It also can right shift the word in an end-around fashion. The output of the barrel switch may be directed to any of the following destinations simultaneously:

- a. The A registers.
- b. The B register.
- c. The memory information register.
- d. The least significant 16 bits to the MCU registers.
- e. The least significant three to six bits to the control unit shift amount register (bit length depending on the word size of machine).



## 2. The Control Unit

The control unit has five major sections: the shift amount register (SAR), the condition register (COND), part of the control register (CR), the decoder for microprogram memory content, and clock control. This module of the D-machine manages the functions of the processor, and is directly responsible for logic unit operation.

SAR and its associated logic control shifting operations by loading shift amounts into SAR and generating the required controls indicated by the current microinstruction for the barrel switch. In addition, the SAR's logic generates the 'word length complement' of the SAR contents where the complement is defined to be that amount which would restore the bits of a word to their original position after an end-around shift of  $N$  followed by an end-around shift of the 'complement' of  $N$ . For example, if an end-around right shift of 20 was required in a 32-bit D-machine, another end-around shift of the complement of 20 (12) would be required to restore the contents to its original value.

The condition register has four major functions:

- a. It stores 12 resettable bits which are used as error indicators, interrupts, status, and lockout indicators.
- b. It selects one of 16 condition bits for performing conditional operations. These 16 bits are composed of the 12 condition bits of the



condition register plus the 4 dynamic conditions generated by the LU adder during the present clock time.

- c. It decodes bits from the memory for resetting, setting, or requesting the setting of designated bits of the condition register.
- d. It resolves priority between interpreters in the setting of global condition bits (GC), thereby providing a method of controlling inter-  
interpreter lockout.

The control register stores the control bits of the 56-bit microinstruction that are not being used in the first phase of the execution cycle. The control register is subdivided into sections which are used by the memory control unit, the logic unit, and the control unit during the execution phase of a microinstruction. For a description of timing and phases, see section C of this chapter.

### 3. Memory Control Unit

The memory control unit provides the basic addressing interface between the D-machine and both main memory (S-memory) and microprogram memory (M-memory). One MCU can address 64K words (256K bytes) of main memory, and if the D-machine is configured with a second MCU, a maximum of 128K words can be addressed.

The memory control unit has three major sections:



- a. The microprogram address section controls the addressing of microprogram memory and the sequencing of microinstructions. It contains the microprogram count register (MPCR), the alternate microprogram count register (AMP CR), the incrementer, the microprogram address controls register, and their associated logic. For standard 4K M-memories, the MPCR and AMP CR are 12 bits long. For 8K M-memories, MPCR and AMP CR are 13 bits in length (the D-machines installed at the Postgraduate School employ 8K M-memories). AMP CR is a Y-select input to the logic unit adder.
- b. The memory/device address section contains the 8-bit memory address register (MAR), two 16-bit base registers (BR1 and BR2), output selection gates, and associated control logic. When forming a memory address, the lower eight bits of a base register and MAR are concatenated. The concatenated 24-bit contents of BR1/ BR2 and MAR (BMAR) is a valid Y-select input to the logic unit adder.
- c. The Z register section contains two registers which are Z inputs to the logic unit adder. The literal register (LIT) is an 8-bit register into which constants are loaded. An 8-bit counter (CTR) is used in conjunction with a counter overflow condition bit to control iterative





looping. The Z register section also contains selection gates for the loadable counter and its associated logic.

#### 4. Microprogram memory (M-memory)

A D-machine may have a dual or single microprogram memory scheme. As indicated earlier, the D-machines used in this emulation project had a single microprogram memory, consolidating the microprogram memory and nanomemory into one 56-bit programmable store memory, often referred to as M-memory. Microprograms, consisting of 56-bit microinstructions, are dynamically changeable by the user, thus distinguishing the D-machine as an extremely flexible computing device.

The sequencing of microprogram instructions is controlled by a condition bit procedure which determines the successor command to be executed. M-memory provides data to the condition testing logic which then determines which condition is to be tested. The output of the condition testing logic is a true/false signal that is gated to the successor selection logic. This logic then selects between the three true and three false successor bits also provided by the M-memory word. The three selected bits provide eight possible successor combinations:



- a. WAIT Repeat the current instruction.
- b. STEP Step to the next instruction.
- c. SKIP Skip the next instruction.
- d. JUMP Jump to another M-memory address.
- e. RETN Return from a microprogram subroutine.
- f. CALL Call a microprogram subroutine.
- g. SAVE Step and save the instruction address.
- h. EXEC Execute one instruction out of sequence.

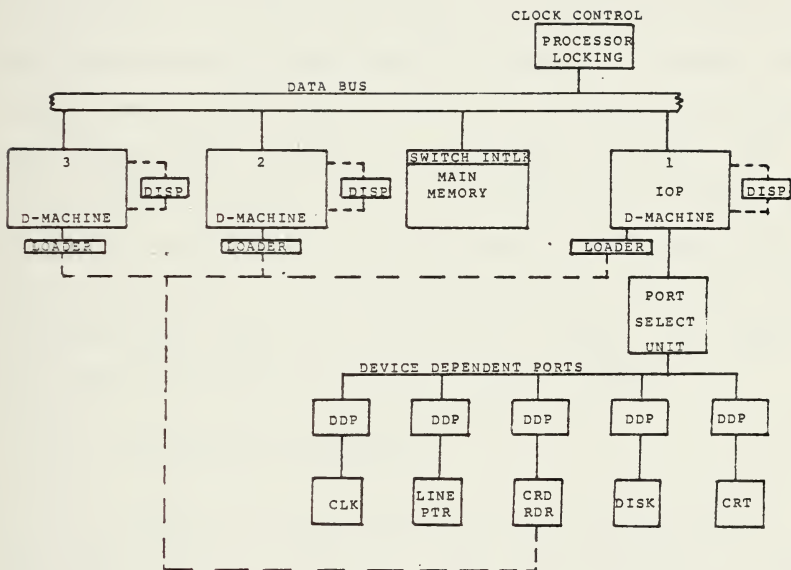
The particular successor command chosen controls gates which select the appropriate M-address from MPCR or AMPCR and provides incrementing logic for generating the next M-memory address. Except for the EXEC command, the MPCR is loaded with this M-memory address.

## B. NPS MICROPROGRAMMING FACILITY

### 1. Physical Description

The Computer Science Department of the Naval Postgraduate School possesses a Burroughs Interpreter-Based System consisting of three interpreters (processors) also known as D-machines, a 64K 32-bit word, main memory module, a card reader, a dual cartridge disk drive, a line printer, and a Datamedia 2500 CRT functioning as a supervisor's console (Figure IV-2). All input and output is performed through a single D-machine processor, hardware configured with device dependent ports (DDP) for peripherals and the external clock.





NAVAL POSTGRADUATE SCHOOL MICROPROGRAMMING FACILITY  
 BURROUGHS INTERPRETER-BASED SYSTEM

Figure IV-2



After initial light-off and bootstrap, the system is configured into two Burroughs 6700 - LIFO ALGOL Stack-machines, each addressing 32K of memory and each communicating with the input output processor (IOP) in a pseudo-multiprocessing environment. Software, written in ALGOL, is provided which runs on the B-6700 system. A resident monitor control program and disk file manager control the maintenance of system files and the execution of jobs in a batch environment. Both D-machines compete for system jobs input from the card reader or CRT. Other software available includes an ALGOL compiler (a derivative of ALGOL 60), a microprogram translator called TRANSLANG, a line editor, and a simulation program for microprograms. TRANSLANG provides the medium by which microprograms are written. User microprograms loaded into a D-machine change its identity and destroy the Stack-machine previously loaded.

## 2. Input/Output Interface

Pivotal to the operation of the Burroughs system is the input/output interface. Only one processor, the IOP, communicates with peripherals, and the other D-machines, configured as Stack-machines, must compete for its services. The IOP communicates asynchronously, using a conventional 'handshake' method. Since all interpreters have access to the main memory module, a communications link has been established using the upper two 32-bit words of main memory. If a Stack-machine wishes to communicate with the IOP, it places a message into address 65,535 known as the 'mailbox',





and issues an interrupt (INT) to the IOP. The IOP periodically tests INT, and if set, will retrieve the contents of the mailbox (and mailbox - 1 if required) and perform the desired operation. The other Stack-machine is locked out from interrogating the IOP until it has completed processing the request. Normally, the operation requires transferring a buffer to some output device. When the IOP has completed honoring the request, it places a completion code in the mailbox and sets INT for the Stack-machine requesting the I/O. This interpreter must halt execution and check mailbox to see if the I/O was performed successfully, completing the handshaking process. This protocol permits both Stack-machines to perform input/output independently of each other, provided both maintain strict memory boundaries.

Another function of the IOP is interfacing character code formats between the peripherals and the other two D-machines. When the machines are configured as Stack-machines, characters are passed to the IOP in 6-bit BCL (Burroughs Common Language). The IOP must convert this character set to ASCII for output to the line printer and CRT. A similar translation must be made for input data converting from either EBCDIC or ASCII depending on whether the input source is the card reader or the CRT.

### 3. Memory Interface

Since all three D-machines must share the 64K of main memory, a priority scheme was developed to resolve



memory reference conflicts. The main memory module is actually a single-ported, 32-bit word, core memory which can be made to appear multiported using a switch interlock unit (SWI) developed by Burroughs. The switch interlock controls the main data bus of the system, and resolves conflicts using a priority scheme. The D-machine with the highest priority is the IOP, with the priority of the other two machines being relative to their physical proximity to the IOP. Once a memory reference has been made, a D-machine may continue execution without waiting for a completion signal from the switch interlock. Although this technique of memory referencing minimizes unnecessary delay, it restricts the program from changing the read or write addresses or the content of MIR (write only) prior to a completion signal.

### C. MICROINSTRUCTION TIMING

The Burroughs D-machine initiates a microinstruction once every clock cycle. The D-machines utilized for the AN/UUK-20 emulation operated from a one MHz internal clock, which produced a clock pulse once every microsecond. A D-machine designed with an eight MHz clock, emitter-coupled logic (ECL), and a faster memory cycle time, however, could execute eight times faster. This implies that advances in circuit technology can permit emulations to achieve improved speed and performance with no change in the microprograms.

Every microinstruction is executed using one or more sequential time periods, called phase 1, phase 2, and phase



3. A phase is a constant interval of time equivalent to one clock duration measured from the trailing edge of each successive clock pulse. Some microinstructions only require phase 1 to complete execution. Some require phase 1 and phase 3, and still others require phases 1,2, and 3. A new microinstruction is initiated at each clock cycle, allowing for overlapping of microinstruction execution in phase 1 and phase 3.

Microinstructions consist of two types. In a type 1 microinstruction, events can take place in all three phases:

Phase 1: condition testing, (conditional) external operations or (conditional) logic operation initiation after completion of a prior logic operation, and successor M-memory address control.

Phase 2: a holding phase for phase 3 logic operation controls.

Phase 3: the completion phase for logic unit operations and destination register gating specified by logic operation.

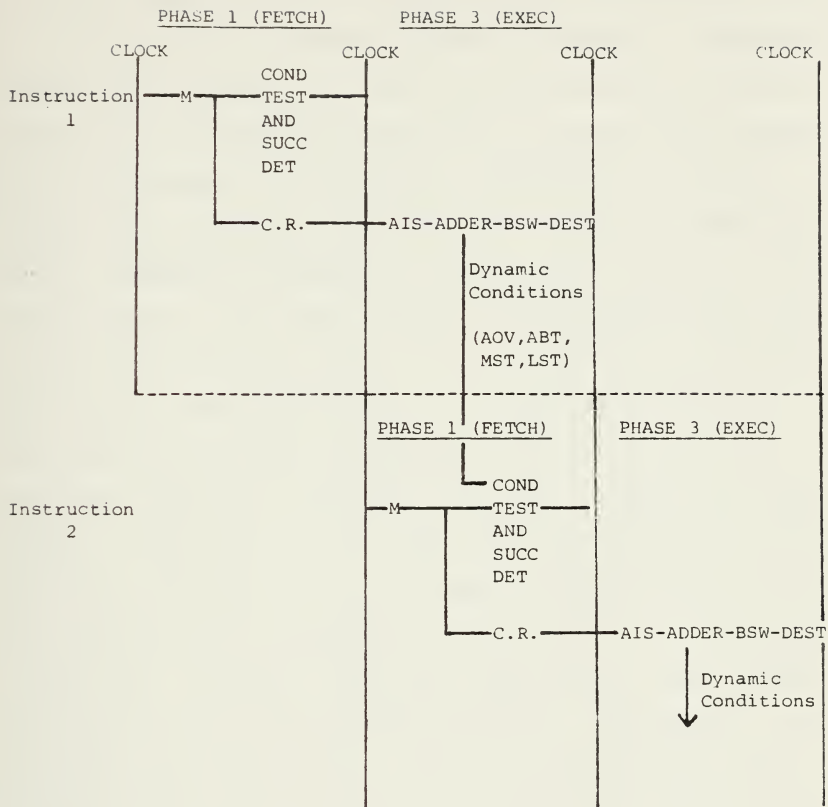
During the optional phase 2 period, a type 1 microinstruction execution completion is held in abeyance while a subsequent type 2 instruction is executed. A type 2 microinstruction requires only phase 1 to complete execution, and involves literal assignments to three registers: LIT, SAR, and AMPCR. Phase 2 may also be initiated if the



next sequential type 1 instruction does not execute its conditional logic operation and therefore can complete its execution in phase 1 (Figure IV-3). Appendix D of Ref. 6 has a complete discussion of microinstruction timing.







- M - MPM ACCESS TIME
- COND TEST AND SUCC DET - CONDITION TEST AND SUCCESSOR DETERMINATION
- BSW - BARREL SWITCH
- DEST - BARREL SWITCH OUTPUT DESTINATIONS; I.E., REGISTERS (B,CTR,ETC.) AND THEIR INPUT LOGIC
- C.R. - COMMAND REGISTER AND ASSOCIATED LOGIC
- AIS - ADDER INPUT SELECTION FROM COMMAND REGISTER

Timing Analysis, Type I Instructions

Figure IV-3 [17]



## D. TRANSLANG

Microprogramming on the D-machine is accomplished using a microtranslator/assembler called TRANSLANG. TRANSLANG allows the programmer to write microinstructions mnemonically without concentrating on the bit patterns that compose the microinstructions themselves. TRANSLANG is written in ALGOL, the language of the B6700 Stack-machine. Nearly the entire language of TRANSLANG is composed of reserved words recognized by the ALGOL program. Each reserved word has a special meaning which causes the translator to construct particular microinstructions. A TRANSLANG instruction is equivalent to one microinstruction consisting of the set of parallel D-machine functions performed during the clock phases. TRANSLANG is a free form language and instructions may be written in almost any order. Multiple instructions may appear on a line, separated by a period '.'. TRANSLANG constructs include iterative mechanisms, input/output, assignment functions, control transfers, and Boolean, and computational operations. In addition, TRANSLANG permits label definitions and symbolic references for program control flow. Reference 6 is the programming manual for TRANSLANG and contains the complete syntax for the language. Appendix A of Ref. 10 documents additions to the TRANSLANG instruction repertoire.

A microprogrammer may construct complicated microinstructions that perform many different tasks, some interacting closely with D-machine clock timing. Microinstruction



gating to several devices permits a single TRANSLANG instruction to accomplish some or all of the following actions:

- a. test a condition.
- b. set/reset a condition.
- c. initiate an external operation.
- d. add.
- e. shift the result of an add.
- f. store the result into several registers.
- g. increment a counter.
- h. complement a shift amount.
- i. determine the successor microinstruction.

By judiciously composing his microprogram, a programmer may minimize execution time by taking advantage of microinstruction phase overlap and using highly parallel microcode.

The TRANSLANG assembler constructs an object program consisting of non-relocatable 56-bit microinstructions. TRANSLANG maintains a cross reference table that resolves label references during assembly. The object code created is stored on a disk and may be loaded into the micromemory of a D-machine using a special control word recognized by the operating system. Once loaded, the D-machine assumes the control structure dictated by the users microprogram.



## V. AN/UYK-20 EMULATOR

### A. EMULATION DESIGN

#### 1. Functional Components

The architecture of the AN/UYK-20 emulator microprogram was developed using general guidelines provided by references and previous emulation experience on Burroughs D-machines [10]. The first decision incorporated in the emulator design was to integrate the entire emulation within one D-machine. Since the D-machines had the capacity to handle nearly 8K of microinstructions, no microprogramming capacity limitations were envisioned. The design objectives of a modularized, well-documented, structured microprogram could also be realized.

With the emulator entirely contained in one D-machine, several secondary benefits also existed. First, the emulator was more immune to hardware problems. If one D-machine was malfunctioning, the emulator could still be run on the alternate D-machine. Second, it was possible to have two AN/UYK-20 emulators resident in the system at one time. Not only would two emulators speed up testing of the individual emulation, but they would also permit their eventual use in a system configured for AN/UYK-20 multiprocessing. The third and final benefit of a totally integrated





emulator was recognized during the design of the input/output controller (IOC). Since the AN/UYK-20's IOC was capable of independent processing, an emulation of its IOC would not be possible within the same D-machine. An emulation of the IOC could be accomplished in a second D-machine, which would behave as an independent channel for the D-machine configured as the AN/UYK-20 processor. Although this emulation does not attempt to emulate the AN/UYK-20 IOC, the fact that a second D-machine exists makes its implementation a realistic extension to the project.

The emulator program organization was created following the basic guidelines of Ref. 17. The loader occupied the lowest section of M-memory with the emulator microcode following sequentially. Microprogram control passed from the loader to the emulator via the execution of a 'G' card which signified execution commencement.

The emulator microprogram was organized into three modules positioned such that forward address referencing would be minimized in the TRANSLANG assembler to save time and space. The utilities section was in the lowest portion of the emulator, since its routines were referenced frequently by the succeeding sections. Individual subroutines within the utility section were organized alphabetically.

The instruction and memory fetch routines comprised the next module. These routines incorporated all fetch options available in the AN/UYK-20 emulator.



The opcode routines occupied the last section of the emulator. The opcodes were arranged numerically with further indexing determined by the remaining fields of the individual instruction. Figure V-1 shows the M-memory mapping of the AN/UYK-20 emulator layout. Appendix F contains the emulation program listing.

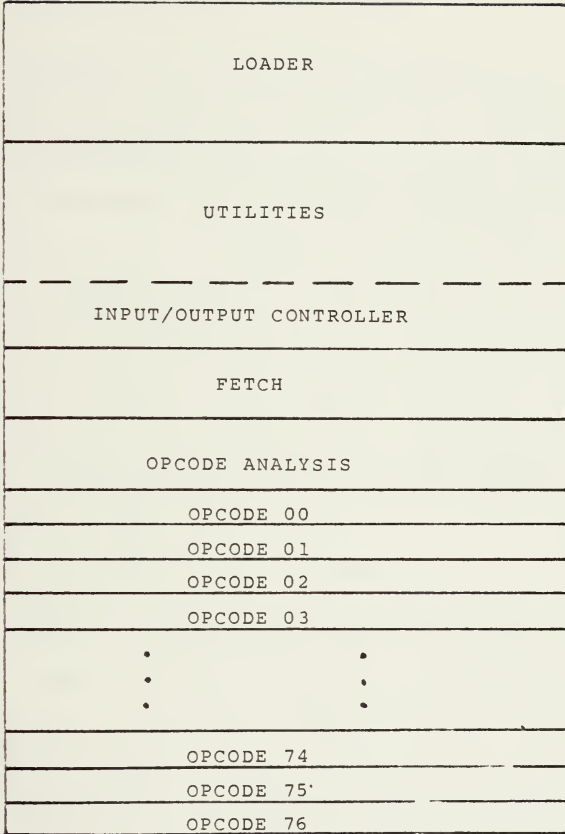
## 2. Main Memory Organization

Of primary importance in the emulation design was the logical organization of the Burroughs system's main memory. Since the AN/UYK-20 was a 16-bit word machine, it was decided that only the lower half-word of a Burroughs 32-bit word would be used by the emulator. This design restriction permitted the addressing structure of the AN/UYK-20 to be directly projected on the D-machine. A one-to-one correspondence between the memory address of the AN/UYK-20 and the Burroughs system was also achieved.

Since the number of high-speed registers available in the D-machine was small, a 1K portion of main memory was reserved for the AN/UYK-20 addressable register set, the page address registers, the temporary storage space, and the emulation buffers. The mapping of the AN/UYK-20 high-speed registers to main memory greatly simplified the microprogramming requirements of the emulation, but added considerable execution time overhead. Memory access times for the mapped registers were much slower than the actual transfer



0000



AN/UYK-20 EMULATION ORGANIZATION

Figure V-1



rates of the AN/UYK-20 registers. Figure V-2 shows the complete main memory mapping of the emulation reserved storage area.

### 3. Emulation Program Status Word

Although the emulation duplicated all the AN/UYK-20 registers, the registers which comprised the program status word (PSW) possessed unique characteristics. Status register 1 was combined with the program address register to form a single 32-bit PSW. The emulator's PSW always co-existed in the A1 register of the D-machine and in main memory during execution of AN/UYK-20 programs. The fields of SR1 were modified to include certain emulator toggles, along with the normal condition bits (Figure V-3). The condition bits for DMA and non-destructive read only (NDRO) mode were removed from the SR1 since they were hardware features of the AN/UYK-20 that would not be emulated.

Status register 2, the remaining 16 bits of the AN-UYK-20's PSW, was not resident in any D-machine registers during emulation execution for two reasons: the emulation could not afford the luxury of 48 bits of reserved register space, and SR2 was less frequently referenced than SR1 and the P-register. Consequently, SR2 had to be read from its reserved location in main memory. The contents of the upper 16 bits of SR2's memory location also contained additional emulation toggles which were used by the debugger package (Figure V-3).





MAIN MEMORY MAPPINGS

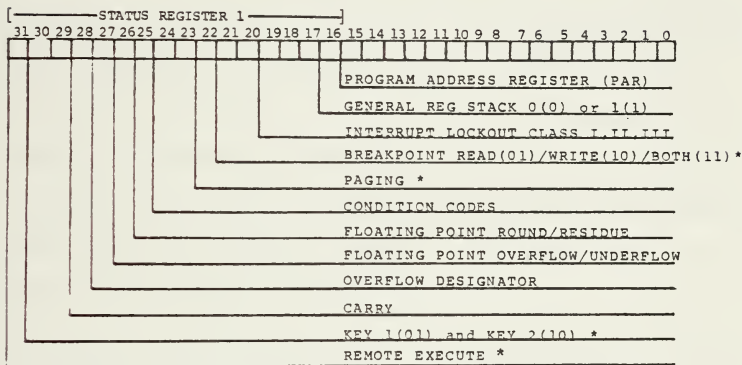
DECIMAL ADDRESS	OCTAL ADDRESS	USE
0 - 15	0 - 17	GENERAL REGISTER STACK 1
16 - 31	20 - 37	GENERAL REGISTER STACK 2
32	40	PROGRAM STATUS WORD
33	41	BREAKPOINT REGISTER
34	42	STATUS REGISTER 2 (SR2)
35	43	NEXT LOAD ADDRESS
36	44	CLOCKTIME
37	45	REAL TIME CLOCK
38 - 43	46 - 53	WORKSPACE (TEMP STORAGE)
44 - 49	54 - 61	STACK (TEMP STORAGE STACK)
50 - 53	62 - 65	I/O COMMAND WORDS (IOCW)
54 - 119	66 - 167	UNUSED
120 - 121	170 - 171	HEX ADDRESS FOR INPUT
122 - 141	172 - 215	INPUT CARD BUFFER
142 - 152	216 - 230	UNUSED
153 - 185	231 - 271	OUTPUT PRINT BUFFER
186 - 205	272 - 315	CRT BUFFER
206 - 229	316 - 345	ERRORLIST
230 - 767	346 - 1377	UNUSED
768 - 1023	1400 - 1777	PAGE ADDRESS REGISTERS

Figure V-2

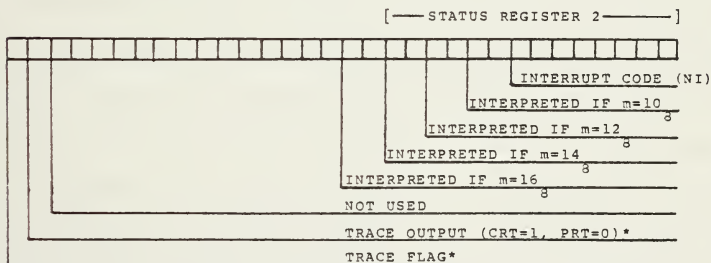


AN/UYK-20 EMULATION  
PROGRAM STATUS WORDS (PSW)

ACTIVE PSW: RESIDES IN LU REGISTER A1 (MEMORY ADDRESS 32)



INACTIVE PSW: RESIDES IN MEMORY ADDRESS 33



\* FIELDS ADDED FOR USE BY THE EMULATOR

Figure V-3



#### 4. D-Machine Registers

with only a limited number of high-speed registers available in the D-machine, the emulation design had to include a well-developed plan for their usage. Since only seven registers in the D-machine were 16 bits or longer, they were used exclusively for manipulating the AN/UYK-20 addresses, instructions, and data. The register environment had to be consistent throughout every execution cycle to allow utility routines to be called in the same manner by all opcode subroutines. The primary goal of the emulation was to use as few memory references as possible to conserve execution time and memory space. Judicious use of the existing registers was a necessity.

Several factors had to be considered before selecting a register for a particular function. The most important consideration was its flexibility within the D-machine. The B register, for example, was used as a general purpose register, since its contents could be gated through a masking filter prior to being utilized. A second factor was the type of operand it could contain. Double-word operands (32-bit) could only be stored in the 32-bit logic unit registers while 16-bit operands could also be stored in the memory control unit registers.

The A1 register contained the emulation's 32-bit program status word (PSW) at the commencement of the emulator program. It was not affected by individual instruction



microcode, except when incrementing the PAR, or when a particular instruction modified the PSW. Emulator toggles resident in SR1 could not be altered by an AN/UYSK-20 instruction because their settings were independent of program execution.

The A3 register held the instruction word for the duration of its execution cycle. Each field of the instruction could be decoded and interpreted from the A3 register without having to retrieve it from memory. Once the instruction had been completely decoded, A3 was made available as a scratch pad register.

The A2 and B registers were used as scratch pad registers during each opcode execution cycle. In general, their contents were volatile, except when they were specifically documented in the the program listing. The contents of A2, for example, was not altered in the EMULIN subroutine, because of its use in the calling fetch routine. A2 and B were manipulated as either single or double-word operands during the arithmetic operations.

The only remaining logic unit register was the memory information register (MIR). MIR was used for storing information into memory and as a temporary storage location. Intermediate results were deposited in MIR during instruction execution and returned through the B register.

The base registers, BR1 and BR2, were used as storage for addresses and single-length operands, and for





temporary storage of intermediate results. In addition, all memory addressing in the emulation was accomplished using the lower 8 bits of BR2 and MAR (MAR2). These memory control unit registers had to be used carefully, because they required a sequence of several microinstructions to properly reference their contents.

## B. LOADER

The loader incorporated into the AN/UYK-20 emulation provided a simple mechanism for loading AN/UYK-20 instructions into main memory (S-memory) of the Burroughs microprogramming system (Figure V-4). Its control word repertoire was flexible, allowing a variety of AN/UYK-20 program environments. Job control statements were included to execute and halt individual programs anywhere in S-memory.

The loader module consisted essentially of a scanner and a translator written in the microcode. Information was read into a 20-word buffer from cards or CRT input, then the buffer contents were scanned for control code consisting of one or more characters. Once these characters were interpreted, control was passed to the translator section which decoded the rest of the data in the buffer and performed the required function. The translator section consisted of a variety of routines that handled specific control words in the loader repertoire. The loader control statements, however, had to appear in a logical sequence (See Appendix A). All loader control statements are contained in Appendix B.



AN/UJK-20 LOADER

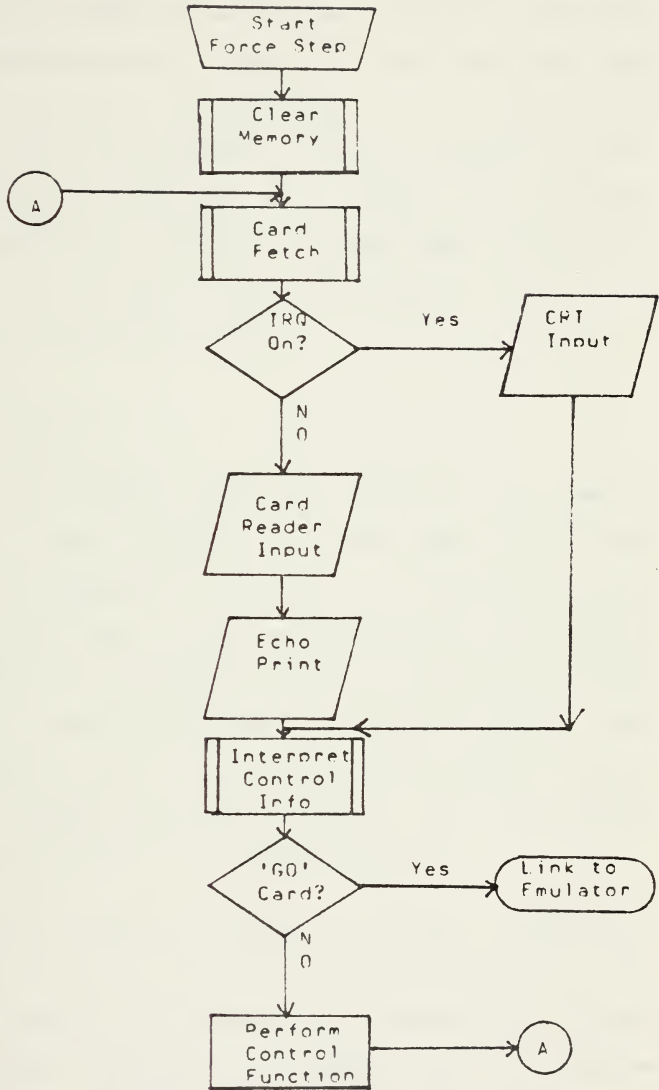


Figure V-4



The actual interface pipeline between the loader and the emulator consisted of two small emulator utility routines which started and stopped the external clock of the Burroughs microprogramming system. These routines were inserted for emulation timing purposes, and provided a 'stop watch' for AN/UUK-20 programs. The time recorded (in milliseconds) by this 'stop watch' was placed in a reserved memory location in the emulation memory map, and could be read using either a trace control instruction ('T'), or a machine status control word ('M').

#### C. THE FETCH MODULE

In order to emulate AN/UUK-20 execution and memory referencing, fetch microcode was developed which incorporated memory addressing algorithms and instruction fetch routines. Since both data and instructions were equally accessible from the processor, the memory addressing scheme was closely linked to the instruction fetch concept. Data and instructions could be interspersed throughout memory, and proper program execution required that the program address register point to an instruction word.

The emulation used two routines for memory addressing, EMULIN for reading, and EMULOUT for writing (Figures V-5, V-6). These subroutines performed both paging and break-point checking, depending on toggles set in the program status word. Paging was incorporated into the emulation in order to gauge the execution overhead required in emulating



the AN/UYK-20's paging scheme. The paging scheme implemented in the emulator divided main memory into 256-word pages, instead of 1024-word pages used by the AN/UYK-20. Since the Burroughs D-machine was organized for 256-word pages, the microprogramming required for the paging was straightforward. The 256 page address registers resided in the emulator's memory mapping, each initialized to the page number corresponding to their relative address (0-255). The paging algorithm imitated the AN/UYK-20's method of page addressing, and included the setting of a page modification bit.

The breakpoint option was added to provide a method of debugging AN/UYK-20 programs, once the emulation was completed. EMULIN and EMULOUT tested toggles set in the PSW to determine if breakpoint read, write, or both was desired.

The memory addressing convention required all memory references from 1K to 64K to use EMULIN and EMULOUT. All memory references to the memory mapping area (0-1023) did not use these routines, but instead utilized absolute memory referencing microcode.





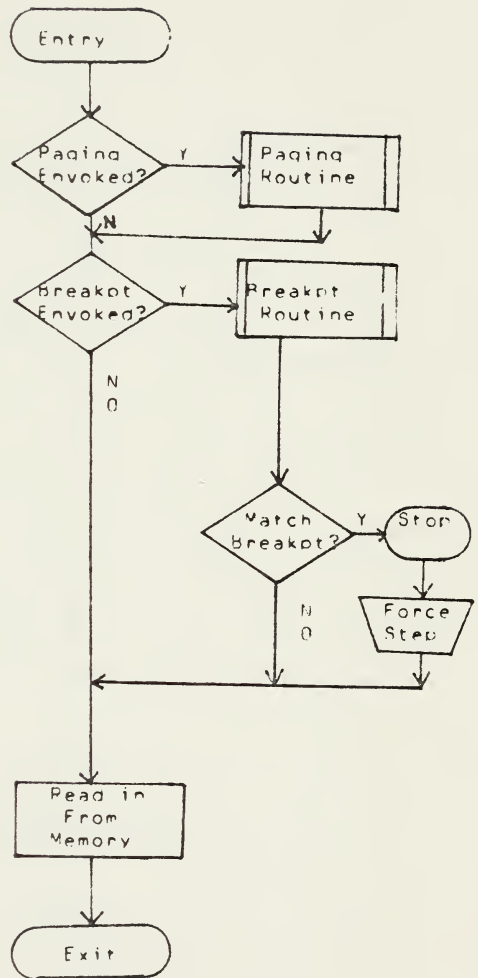


Figure V-5



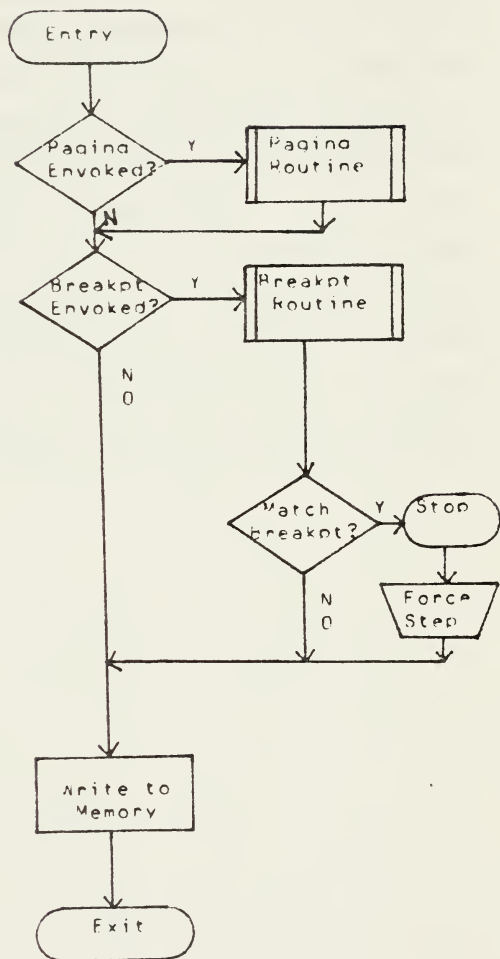


Figure V-6



The instruction fetch routine (IFETCH) retrieved instructions from main memory based on the contents of the program address register. Since IFETCH used EMULIN to read the instructions from memory, it could operate in a paging environment, with or without breakpoints (Figure V-7). IFETCH was also responsible for incrementing the PAR, and for testing the trace toggle prior to fetching an instruction. IFETCH was capable of retrieving any instruction word in the program address space (1024-65,535). In the event that the upper memory limit was reached, IFETCH would set the PAR to 1024 and continue execution. Trace toggle testing was inserted into IFETCH as part of the built-in debugging package. Since IFETCH was called prior to every instruction, it was the logical choice for placing a call to the debugger.



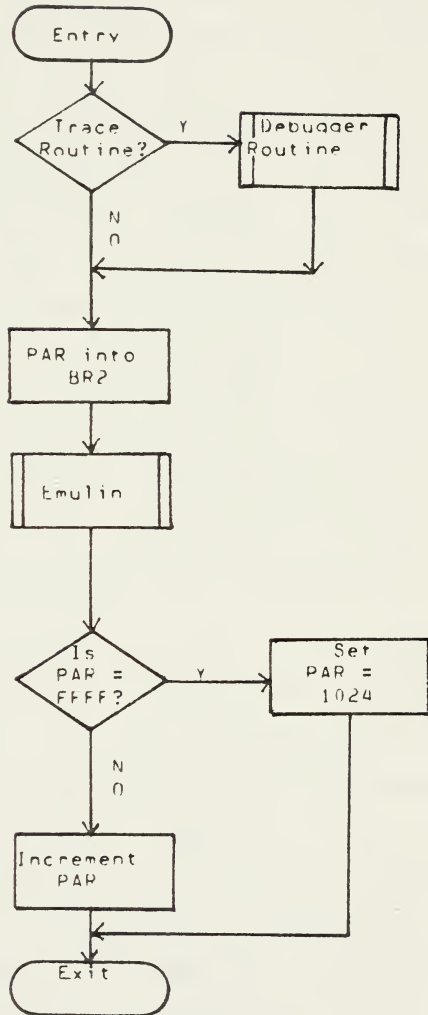


Figure V-7





#### D. OPCODE IMPLEMENTATION

All of the 205 individual instructions emulated were microprogrammed using an identical instruction decoding mechanism. The routines that performed the required operations were terminal nodes on a large tree network, whose root was the OPCODE routine. OPCODE fetched an instruction and isolated the operation code field. The binary value of the opcode field was an index to an operation jump table containing individual opcode M-memory addresses. Within each opcode routine was microcode which isolated the sub-function 'f' field of the instruction and used its value as an index to the next level of opcode analysis. Depending on the opcode, this last jump could identify which instruction was to be performed. If it did not, further analysis of the 'm' or 'a' fields provided the final index to the instruction. Instruction formats are described in Appendix C.

After the instruction had been executed, control passed back to the opcode routine, and then the execution cycle was repeated for the emulation of the next AN/UYK-20 instruction. The AN/UYK-20 programmer could cause this microprogram loop to be exited by either inserting an executive return instruction (03,0,a,00) which caused a 'priority interrupt' and halted program execution, or by coding an instruction that was not implemented, not assigned, or caused a division overflow. The last three cases caused an execution fault, while the former resulted in normal program termination (Figure V-8).



AN/DYK-20 EMULATION GENERAL STRUCTURE

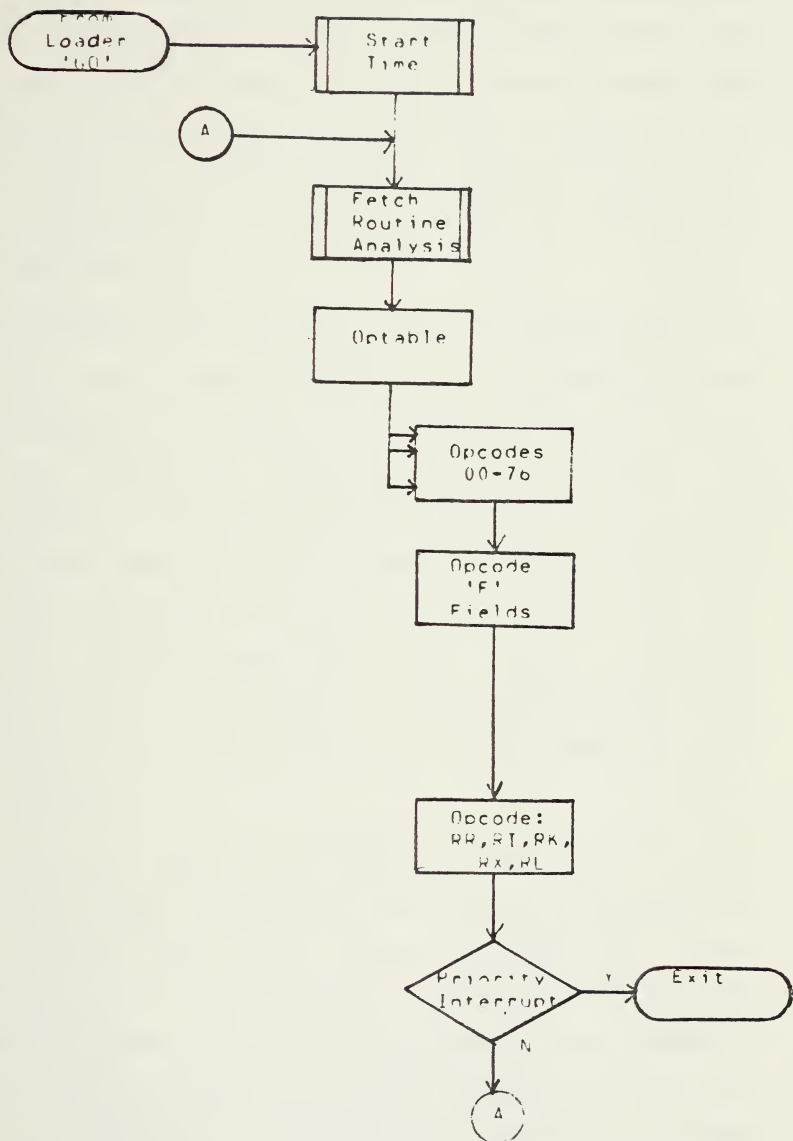


Figure V-8



The instruction fetch mode of OPCODE assumed that the PAR always pointed to an instruction word. Double-word instructions always had their 'y' field fetched after they were determined to be two words in length. Conditional double-word instructions performed their condition test before the 'y' field was fetched. If the test failed, the PAR was incremented by two prior to returning to OPCODE for continued execution.

The OPCODE routine was also written to accommodate the AN/UJK-20 'remote execute' instruction. When this operation was performed, a bit was set in the PSW which would indicate that one instruction out-of-line was being executed. For this operation, the current PSW was stored in memory, and the PAR was loaded with the address of the instruction to be executed. The OPCODE routine always checked the remote execute bit during an instruction cycle. If the bit was set, it would fetch the instruction indicated by the remote execute PAR, and restore the actual PAR, incremented by two, into the PSW.

Some of the opcode repertoire of the AN/UJK-20 was not emulated. Those instructions that were not emulated, however, retained slots in the opcode hierarchy for future inclusion. Any instruction not implemented by the emulator caused the machine to fault, and printed an error diagnostic on the selected output device ('NOT IMPLEMENTED - EXECUTION ENDS '). Similarly, locations were reserved for those instructions not assigned by the AN/UJK-20 were reserved



locations in the emulation . This permitted the emulator to be responsive to any future AN/UYK-20 hardware modifications. Whenever an instruction to be executed was not assigned, the emulator generated a fault interrupt and printed an error diagnostic on the selected output device ('FAULT INTERRUPT - EXECUTION ENDS').

## E. UTILITIES

Although each emulated instruction performed different operations, each depended upon a common set of utility subroutines to accomplish their task. These subroutines varied in complexity, but each performed a function that contributed to successful instruction execution. A simple operation often required register addressing, condition code setting, and memory addressing, before the task was completed.

Utility subroutines were included in the emulation whenever feasible to simplify microprogramming and to alleviate programming redundancy. These subroutines were called using the successor command constructs available in TRANSLANG. Depending on the purpose of the utility routine, parameters were passed via D-machine register(s) or condition bit(s). This information was utilized by the utility in determining what operation was to be performed. In the carry subroutine, for example, a local condition bit was passed which indicated the appropriate condition code to be inserted into the PSW. A more complex example, the RX





format utility routine, required two parameters to be set by the instruction. Register A3 contained the instruction word and LC2 was set or cleared depending on whether or not byte formatting was required. The RX routine called other routines and could perform considerable processing before the final result, the effective operand address, was returned to the calling routine via the B register.

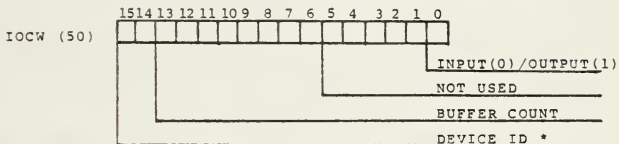
The utility section encompassed a number of routines which performed complex data manipulation. Arithmetic utilities for multiplication, division, and square root were accessed by nine separate AN/UYK-20 instructions. Indirection routines, which were called by the RX format routines, emulated the AN/UYK-20 cascaded addressing capabilities. A general purpose move subroutine permitted up to 256 cells of main memory to be moved from one location to another. This routine was used by the emulator's error diagnostic utilities, as well as the load and store multiple address register instructions.

#### F. INPUT/OUTPUT CONTROLLER

Although the AN/UYK-20's IOC was not emulated, several of its design features were imitated in creating a general purpose input/output controller for the emulator. The input/output command instruction (35 RR) initiated the I/O sequence, and reserved several cells in the memory mapping for I/O control words (Figure V-9). These control words contained fields which indicated what peripheral device was



AN/UYK-20 EMULATION  
 INPUT/OUTPUT COMMAND WORDS



BUFFER ADDRESS  
 THE MICROCODE ALTERS THE IOCW + 1  
 DURING BUFFER TRANSFER



BUFFER SIZE  
 USED FOR CRT OUTPUT



NUMBER OF SECTIONS  
 USED FOR DISK TRANSFERS (NOT IMPLEMENTED)  
 \* CODE: 00 - CRT  
 01 - PRT (OUTPUT)/CRD RDR (INPUT)  
 10 - DISK (NOT IMPLEMENTED)

Figure V-9



selected, the number of buffers that would be passed, whether input or output was desired, and where the buffer was located. Two additional words were reserved for control data required to interface with the disk and the CRT. The disk input/output microcode was not incorporated into the controller, but the framework was provided so the IOC could be readily inserted in the future.

The emulator's IOC section was located in the utility section of the emulation, and operated asynchronously with the Burroughs IOP. Since the IOC was collocated with the emulator in the same D-machine, it was not capable of independent processing. Once it was initiated, emulation execution waited until input/output was completed. The emulation had to use the Burroughs Common Language, since the IOP was microprogrammed to accept only this character set from other D-machines.

In order to transfer a 33-word line printer buffer to the IOP, the AN/UYK-20 emulator IOC had to use 66 AN/UYK-20 words. In order to send 20 words to the CRT, the IOC had to construct a 40-word buffer. The COMPRES subroutine packed an AN/UYK-20 buffer of 66, 16-bit words into a 32-bit, 33-word buffer, suitable for output to the IOP.



Similarly, on input, a 20-word IOP buffer from the card reader or CRT expanded into a 40-word AN/UYK-20 buffer. In this case, the EXPAND subroutine split every packed 32-bit word of the IOP's buffer into two 16-bit words, suitable for processing by the emulator. These additional data transformations were required because of the buffering requirements of the Burroughs IOP.





## VI. EMULATION TESTING

### A. METHOD OF TESTING

The fundamental testing technique utilized throughout the development of the emulation consisted of three distinct phases: 1) each module was independently assembled and debugged until successful assembly was achieved, 2) each program segment was then tested for accuracy of the intended operation, and 3) the composite emulation program was tested under actual program conditions allowing for interaction among several modules. A debugging package, which was developed early in the emulation project, was the primary test vehicle for verifying emulation coding. Development and testing of the loader was, however, completed prior to the creation of the debugger.

Loader testing was accomplished by monitoring the control panel lights and synthetically halting program execution via the insertion of 'WAIT' statements, forcing the desired register to be transferred to 'MIR', and then re-examining the panel lights. This process was extremely tedious and time consuming but proved to be an invaluable tool for recognizing peculiar TRANSLANG constructs and microinstruction execution side effects.



Each module was subjected to an extensive desk checking process in order to reduce trivial assembly errors before running it on the machine. After a successful assembly had been achieved, the code was merged with previously existing assembled modules. The emulator was expanded as more modules were added, with utility routines being incorporated prior to the opcode programs.

Initially, the loader was designed, programmed, and thoroughly tested prior to the microprogramming of any AN/UYK-20 instructions or utilities. With the loader implemented, the emulation of the UYK-20 instruction repertoire could proceed with a minimum of loader induced problems.

Independent opcodes and various utility routines were added to the previously assembled programs. The final emulation consisted of a total of 205 opcodes, a set of utility programs, and a workable loader.

In the next phase of testing, every module was subjected to a representative number of test cases which demonstrated how closely they compared to the documented AN/UYK-20 operation. Artificial environments were created to subject every opcode to a variety of situations. Whenever the operation of the opcode disagreed with the documented AN/UYK-20 operation, the opcode's function was thoroughly researched. The opcode's side effects were categorized and questions formulated. Often the answers could only be obtained from the Univac field engineer.



To illustrate the complexity of testing, an add instruction was tested with numerous operand combinations: two positive operands, two negative operands, one of each sign yielding a negative result, opposite signs producing a positive result, and opposite signs producing a zero sum. During each addition operation, the overflow, carry, and condition bits had to be monitored in status register 1 to verify their appropriate setting. This level of detail was achieved with all of the implemented opcodes in order to produce an efficient and accurate emulation.

Throughout the entire testing scenario, which composed 20% of the emulation project, the debugger routine (DUMPREG) provided the necessary information for examining opcode execution. A representative sample debugger output is provided in Appendix D.

DUMPREG permitted a snapshot of both AN/UYK-20 general register stacks, PSW, SR1, and SR2, in addition to the D-machine registers (A1, A2, A3, BR1, AMPCR, MIR) and the Burroughs external clock. DUMPREG possessed sufficient flexibility to be incorporated into the microcode at any point. In the final emulator, however, the debugger is user specified, and will dump the AN/UYK-20 emulator environment either at every instruction fetch and program stop, or when called by a loader control card.



## B. SAMPLE TEST PROGRAMS

After subjecting the entire emulation to extensive testing, some representative test programs were developed to demonstrate the feasibility of the emulation and its capabilities and performance as compared to an actual AN/UYK-20. There were two programs which were selected because they incorporated numerous emulation features. The two programs were the solution of simultaneous linear equations by Cramer's rule and generation of prime numbers. It must be noted that streamlined program design was not emphasized but rather utilization of a variety of opcodes and features of the emulation.

The program for solving linear equations contained a total of 28 opcodes, requiring 28 opcode execution cycles and 43 instruction fetches. The program demonstrated all four fundamental mathematical operations, numerous store and load functions, a comparison test and a jump instruction. The capability of performing card reader input and output was added when the emulator IOC was completed.

The prime number program demonstrated 30 instructions which required 116 opcode execution cycles, and 122 instruction fetches. This program illustrated numerous comparison tests, looping structures, several jump instructions, a load multiple instruction, addition, and division. The test programs are included in Appendix E.





### C. TEST RESULTS

The performance analysis of the test programs consisted primarily of running numerous test cases, examining the results for accuracy and computing the total time required to execute the emulated AN/UYK-20 programs. The timing of the programs was accomplished by using an external clock available on the ICP. The clock time provided a fairly close representation of the emulation execution time, but it cannot be considered a completely accurate measure since the emulation must interrogate the IOP to retrieve the external clock contents. Approximately 50 microseconds are used when sampling the clock.

The time requirements of the AN/UYK-20 program execution were hand-calculated by summing the published instruction execution times as presented in Ref. 21. The emulation performance ratio (EPR) was computed merely to give an approximate indication of the emulation performance. The EPR is the ratio of measured Burroughs emulation time to the calculated AN/UYK-20 execution time. Two EPR figures are recorded: one with paging implemented and one without. The paging EPR figure is significant only in that it indicates how much additional overhead must be incurred when emulating the paging mechanism of the AN/UYK-20. The required additional execution time was about 26%. Naturally, paging overhead is directly proportional to the number of instruction fetches or memory references performed during a program.



The results of program testing are as follows:

	CRAMER'S RULE	PRIME NUMBERS
Number of Opcodes	28	30
Number of Fetches	43	122
Execution Cycles	28	116
Time w/o paging	5000 usec	13000 usec
Time with Paging	8000 usec	17000 usec
AN/UYK-20 Time	78 usec	193 usec
EPR w/o Paging	64 :: 1	67 :: 1
EPR with Paging	103 :: 1	88 :: 1

These figures represent only approximate comparisons of the two machines. These computations provide an estimate of emulation characteristics. An effective EPR without paging was projected to be 65::1.



## VII. SUMMARY AND RECOMMENDATIONS

### A. EXPERIENCE WITH HARDWARE

The emulation project provided the unique opportunity of learning about two computer systems. The Burroughs D-machine demanded a detailed knowledge of hardware operation, as well as a thorough understanding of the microprogramming language, TRANSLANG. The computer architecture and processor capabilities of the AN/UYK-20 had to be investigated and then integrated into the control store memory of the Burrough's D-machine.

On several occasions, hardware malfunctions with the Burroughs equipment prevented normal system operation. The card reader was inoperable for several weeks, and the disk drive unit had to be repaired several times. During the final three weeks of project development, one D-machine ceased to function properly. This restricted emulation testing to the remaining D-machine.

Although these hardware difficulties impeded normal progress of the project, they did not prevent the emulation from successfully being completed. If a hardware problem prevented emulation testing or debugging, other modules were designed and testing was postponed. This permitted continual emulation development regardless of the hardware



status. In addition, considerable time and effort was invested in trouble-shooting hardware malfunctions, so they could be isolated, diagnosed, and repaired.

## B. LESSONS LEARNED

The emulation project brought together many different computer science techniques and disciplines which will be useful in future computer science endeavors. A great deal of experience in both computer architecture and operation was gained in two different types of computers. Microprogramming provided new insight into computer design and revealed many potential applications for programmable control store machines.

Since emulations normally require a large development effort, this project had to incorporate judicious system design and project management principles in order for it to be completed successfully. Careful monitoring of critical stages of the emulation, and coordination of the programming effort to meet scheduled requirements, was necessary throughout this research. The small programming team concept proved to work extremely well in this project.

Finally, several software practices were strictly followed that proved to be invaluable in constructing the emulation. First, modular programming succeeded in partitioning the emulation into discrete modules which could be designed, coded, tested, and implemented individually. The





emulation was constructed in segments, using the previously verified modules as a test bed for the new modules being built. Structured programming and prolific documentation were useful in developing each microprogram routine because they permitted each team member to understand the function of the program and how it could be used.

### C. EMULATION PROBLEMS

The most significant problem of the emulation was not having had any experience with an AN/UYK-20 and not having anyone readily available with prior AN/UYK-20 experience. This lack of knowledge created some anxiety when attempting to analyze the ramifications of individual opcodes.

The idiosyncrasies of certain opcodes were not made self-evident by the AN/UYK-20 software manuals. Consequently, numerous code modules were redesigned when more detailed information was provided by a UNIVAC field engineer. This proved to be very time consuming, inefficient, and frustrating.

Another emulation difficulty was the lack of working registers in the host machine as compared with the target machine. While the AN/UYK-20 has either 16 or 32 general registers, depending on whether the second stack option is incorporated, the D-machine has effectively only seven workable registers containing 16 bits or more. Therefore, all AN/UYK-20 registers had to be mapped into S-memory which



created much longer register read/write times. This created significant register manipulation problems which in some cases required main memory references for instructions intended to be strictly register-to-register operations. Consequently, increased execution times resulted in a higher emulation performance ratio (EPR), decreasing the overall emulation performance.

#### D. RESULTS

Emulating the AN/UYK-20 on a Burroughs D-machine required a considerable amount of preparation and planning before any results were realized. An in depth analysis of each computer's architecture and operating characteristics was conducted to insure that an emulation was feasible in the allotted time period. From the inception of the project, the goal of the emulation was to implement a standard AN/UYK-20 processor. This decision was based on the capability of the D-machine and an estimate of how much time would be involved in developing, debugging, and testing the final product. Although this goal was achieved, it was felt more time could have been devoted to testing and verifying emulation operation.

The AN/UYK-20 emulation was a highly complex microprogramming project involving numerous data structures and transfer protocols. A total of 205 AN/UYK-20 instructions were emulated out of nearly 290 instructions in the repertoire (including all IOC, math pac, and clock interrupt



opcodes). AN/UYK-20 diagnostic programs and user programs will establish the validity of the emulator's construction.

#### E. RECOMMENDATIONS AND FOLLOW-ON TOPICS

Although 205 opcodes have been implemented, tested, and developed into a working emulation, there are still many challenging avenues to pursue in creating the complete emulation package. First, testing is a continuous process and should be performed in conjunction with code optimization. A comprehensive code optimization effort could improve the EPR without sacrificing code readability.

Second, the floating point and 'math pac' options could be implemented. The addition of floating point arithmetic, trigonometric, and hyperbolic functions would significantly strengthen the scientific capabilities of the emulation. This would be an extremely strenuous undertaking but would permit more tactical data applications of the emulation, increasing its value to the Navy.

One area which could be examined is to perform a comprehensive timing analysis between an AN/UYK-20 and the emulation. This could consist of collecting numerous benchmark programs from Navy AN/UYK-20 installations, where performance data could be accurately obtained. These programs could then be run on the emulator, and analyzed with the benchmark results. The feasibility of replacing or substituting emulation host machines for target machines could be



addressed and supported by the timing analysis study.

An emulation of the AN/UYK-20 input/output controller could be incorporated into the emulation without serious difficulty. Since a second D-machine is available, the IOC channel processor instructions could be emulated and inserted into that D-machine's control memory. The independent processing characteristic of the AN/UYK-20 IOC would be fulfilled using this arrangement.

Finally, when the Burroughs system is linked with the computer science department's PDP 11/50, the AN/UYK-20 emulator could be connected to that system's peripheral resources. This would allow future incorporation of an AN/UYK-20 ULTRA assembler and a CMS-2M compiler into the PDP 11/50 system which could then produce machine language object code files for the AN/UYK-20 emulator to execute.





## APPENDIX A. AN/UYK-20 EMULATOR USER'S MANUAL

This description is designed to provide sufficient information to operate the AN/UYK-20 emulation program. It is assumed that the informal Burroughs D-machine manual in the Burroughs laboratory will supply adequate power-on instructions and solve any hardware operating difficulties which may arise.

The procedure for utilizing the AN/UYK-20 emulator can be divided into four phases:

- 1) selection of the necessary loader control cards (JCL).
- 2) selection of the AN/UYK-20 program instruction set.
- 3) implementation of phases one and two into the required card or CRT format.
- 4) actual hardware implementation on the Burroughs D-machine resulting in program execution.

Phase one can be achieved by selecting the desired loader control cards described in Appendix B. The card format is identical to the CRT format, except that the CRT requires the user to <carriage return> at the end of every line of input data.

Phase two is accomplished by creating the AN/UYK-20 program from a subset of the 205 emulated instructions.



Phase three consists of keypunching the desired JCL and AN/UYK-20 program in the format illustrated in Appendix C.

The resulting job deck will typically be assembled as follows:

```
?SMLOAD TED/UYK20-OBJECT      % loads the emulator into
                                micromemory

L 00004                        % load the program into
                                page 4

C 00206 FAULT INTERRUPT-EXECUTION ENDS "

C 00214 NOT IMPLEMENTED-EXECUTION ENDS "

C 00222 DIVIDE OVERFLOW - FAULT ENTERED"

*****
other desired JCL
*****

AN/UYK-20 Program

    03,0,a,00                    % priority interrupt
                                (mandatory card)

    (a = 00-17 octal)

G                                % commence program
                                execution

M (or M1)                       % machine status (reg. dump
                                at termination)

E                                % end job card
```



Finally, phase four consists of the entire program deck being loaded into the card reader. It is assumed that the IOP is at address 0015 hex, the selected interpreter is at address 0549 hex, the line printer is 'READY', and the IRQ switch is 'off'.

The IRQ switch is a three-way toggle switch mounted on the right side of the interpreter. In the up position, IRQ is 'on', horizontally it is 'off', and the downward position is used for external functions.

If either the interpreter or the IOP is not at the proper starting address, clear them by depressing the 'CLEAR' button on each unit. If this procedure does not remedy the situation, consult the user's manual in the laboratory.

Upon reading the ?SMLOAD card, the system will load the AN/UYK-20 emulator object program into the micromemory of the selected interpreter. The program address counter (on the interpreter) will be at the beginning of the emulation program, address 0000 hex. At this point, the user can select CRT input and output by placing the IRQ switch to the 'on' (upward) position. If CRT input is not desired, leave the IRQ switch in the 'off' (horizontal) position. Next, force step the interpreter by momentarily depressing the FST button (uppermost push button on side panel of the interpreter). Do not hold in the FST button. This may cause some undesirable side effects.



After depressing the FST button, the AN/UYK-20 program is loaded into S-memory. If the input is expected from the CRT, the user must enter his program from the console. Otherwise, the emulator will request cards from the card reader. Once the program has been loaded and the 'G' card read, program execution begins.

After successful program termination, the program returns to the loader and asks for more input. At this point, the user may terminate his job, or start another load sequence. It should be remembered that the AN/UYK-20 emulator has been designed for monoprogramming execution. It executes one program at a time, but can execute any number of programs in sequential order if desired. When the job is terminated, the D-machine returns to its starting address (0000 hex) and awaits further processing. When the user returns to the start address, the system is effectively 'master cleared' since S-memory will be cleared prior to executing any further jobs. It is not necessary, however, to use the ?SMLOAD card for additional programs or program re-runs because the emulator object code still resides in micromemory.

If the results of program execution are not as anticipated, use of either a 'T' or 'T1' option (trace card) is recommended to provide the user with a fetch-by-fetch program trace with the output to the printer or CRT respectively.





APPENDIX B. LOADER CONTROL CARD FORMATS

CARD COLUMNS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	-	20
B	R		decimal		addr												
	w																
	B																
C			decimal		addr		character		string		followed		by		a		"
D			decimal		addr												data
E																	
G			decimal		addr												
I	1						req#										data
	2																
L			dec.		page		num										
M																	
	1																
P																	
R			dec.		number												
S	1																
	2																
T																	
	1																

Note: All numeric fields are in decimal.



# LOADER CONTROL CARD DESCRIPTION

Control Card Identifier	Description
B ---	The 'B' card is used to implement the breakpoint feature of the emulation. This feature allows the user to specify a decimal address in columns 4-8. Column 2 must contain a R or W to breakpoint on a read or write operation respectively. The default condition is breakpoint on both read and write.
C ---	The 'C' card is used to insert character strings into memory. The character string starts in column 9 and continues until terminated by a quote symbol (") or the string reaches column 80. The decimal address where the character string will be written is given in columns 4-8. A blank or zero address field causes the character string to be inserted at the current load address.
D ---	The 'D' card is used to store decimal data from columns 16-20 into the memory address found in columns 4-8. A blank or zero address field causes the data to be inserted at the current load address.
E ---	The 'E' card is used to indicate the end-of-job and therefore is a mandatory control card for job separation.
G ---	The 'G' card or 'GO' card is used to start execution. The starting decimal address is in columns 4-8. The default value of a blank or zero address field will cause program execution to start address 01024.



- I --- The 'I' card or set index register card is used to store decimal data from columns 16-20 into the register designated in columns 7-8, into the general register stack (1 or 2) specified in column 2.
- L --- The 'L' or load card is used to partition memory into 256, 256-word (32-bit) pages and to load the program into the decimal page as referenced by columns 4-8. Pages 0-3 should not be used because they contain the required emulation register mapping and established workspace. The 'L' is a required control card, and it is recommended that it be the first JCL card.
- M --- The 'M' card or machine status card provides a register dump, wherever it is inserted. It is normally placed between the 'G' and 'E' cards in the JCL deck. If a 1 is placed in column 2, the machine status dump will be sent to the CRT. This dump will contain the current value of all AN/UYK-20 general registers, the PSW, SR2, next instruction address, the breakpoint address, and clocktime.
- P --- The 'P' card is used to implement paging.
- R --- The 'R' or reserve space card is used to reserve memory space as specified decimally in columns 4-8.
- S --- The 'S' card is used to simulate setting of the program stop switches (1 and 2) on the AN/UYK-20 maintenance panel. Column 2 must contain a 1 or a 2. Two cards are required if both switches are to be set.
- T --- The 'T' or trace card provides a fetch-by-fetch program trace, dumping the entire machine status on every fetch cycle. If a 1 is in column 2, the trace will be displayed on the CRT. This card is recommended for debugging programs.



APPENDIX C. AN/UYK-20 EMULATOR INSTRUCTION FORMAT

Format

Card Columns

\*\*\*\*\*

5 6 7 8 9 10 11 12 13 14  
 RR, RL, opcode , 'f' , ' a ' , ' m '

RI Type 2

5 6 7 8 9 10 11 12  
 RI Type 1 opcode , 'f' , ' d '

5 6 7 8 9 10 11 12 13 14 15 16 - 20  
 RK, RX opcode , 'f' , ' a ' , ' m ' , ' y '

Notes:

- 1) All fields are in octal with the exceptions of addresses and the 'y' field which are decimal
- 2) All fields must be zero-filled
- 3) The following field restrictions must be followed:

Field	Range	Base
Opcode	00-76	octal
'f'	0-3	octal
'a'	00-17	octal
'm'	00-17	octal
'd'	000-377	octal
'y'	00000-65535	decimal
addr	00000-65535	decimal





## APPENDIX D. SAMPLE DEBUGGER OUTPUT

This appendix provides a sample program output illustrating the Trace option. The debugger is called at the beginning of every instruction fetch, and at the termination of the program. Space has been provided for dumping 48 memory addresses including emulated AN/UYK-20 registers and D-machine registers. Each output line consists of eight regions printed in hexadecimal with a total of eight hex digits (32 bits) per region.

The listing is annotated to indicate the identity of each output cell. A summary of cell definitions (numbering from left to right, top to bottom) follows:

DECIMAL ADDRESS	DESCRIPTION
*****	
0 - 15	General Register Stack 1
16 - 31	General Register Stack 2
32	Program Status word (PSW)
33	Breakpoint Register (BREAKPT)
34	Status Register 2 (SR2)
35	NEXTINSTR (next load address)
36	Clocktime
37	Real-Time Clock (RTC)
38	AMPCR
39	A1
40	A2
41	A3
42	MIR
43	BR1
44 - 47	Unused







## APPENDIX E. SAMPLE TEST PROGRAMS

The programs listed in this appendix were designed to illustrate how the AN/UYK-20 emulator can be used for developing programs. The first two programs presented are the generation of prime numbers and the solution of simultaneous linear equations by Cramer's Rule. They depict several AN/UYK-20 control structures such as looping, iteration, and condition code testing as well as numerous load, store, and arithmetic operations. The last program performs the Cramer's Rule algorithm and demonstrates input/output routines.



L	00034	PRIME NUMBER GENERATOR	
11		PRIME NUMBERS RETURNED IN GEN. REGISTERS	
C		THIS CARD WILL ENVOKE PAGING	
C	00236	FAULT INTERRUPT-EXECUTION ENDS *	
C	00214	NOT IMPLEMENTED-EXECUTION ENDS *	
C	00222	DIVIDE OVERFLOW - FAULT ENTERED *	
	63,0C03,01	LITERAL LOAD, 1 INTO REG 4 (SET PRIME)	00000005
	63,0A03,02	LITERAL LOAD, 2 INTO REG 5 (2ND PRIME)	00000420
	63,0A05,02	LITERAL LOAD, 2 INTO REG 6 (COUNTER)	00000000
	63,0C07,05	LITERAL LOAD, NO. OF PRIMES INTO REG 7	00000000
	11,3A09,0C,02018	STORE A, 1 INTO ADDR 2048	00000000
	11,3A09,0C,02019	STORE A, 2 INTO ADDR 2049	00000000
	24,0C07,04	COMPARE N (NO. OF PRIMES) & 1	00000000
	44,1A07,6	LOCAL JUMP, IF EQUAL	00000000
	24,0A07,05	COMPARE H AND 2	00000000
	44,1A023	LOCAL JUMP, IF EQUAL	00000000
	65,0A11,02	LITERAL LOAD, 2 INTO REG 11 (CANDIDATE)	00000005
	62,2A11,01	LITERAL ADD, INCREMENT CANDIDATE	00000000
	65,0A13,02	LITERAL LOAD, 2 INTO REG 10 (TRIAL DIVIS)	00000000
	01,0A13,11	LOAD REG, CANDIDATE INTO REG 13	00000000
	01,0A12,00	LOAD REG 12 WITH C	00000000
	77,0A12,1C	DIVIDE REG, CANDIDATE BY TRIAL DIVISOR	00000000
	24,0C09,12	COMPARE, REMAINDER WITH 0	00000000
	44,1A371	JUMP IF EQUAL, NON-PRIME, GET NEXT CAND.	00000000
	62,2A13,01	LITERAL ADD, INCREMENT TRIAL DIVISOR	00000000
	24,0A10,11	COMPARE DIVISOR WITH CANDIDATE	00000000
	47,1A370	JUMP IF LESS THAN, TRY NEW DIVISOR	00000000
	11,3A11,06,02048	STORE FOUND PRIME INTO MEMORY	00000000
	62,2A05,01	LITERAL ADD, INCREMENT PRIME COUNTER	00000000
	24,0A05,07	COMPARE, PRIME COUNTER WITH N	00000000
	47,1A351	JUMP IF LESS THAN, GET NEXT PRIME CAND.	00000000
	05,3A03,04,02049	LOAD MULT, PRIMES FROM MEMORY INTO REGS	00000000
	03,0A17,00	PRIORITY INTERRUPT, HALT EXECUTION	00000000
	63,0A01,02	LIT LOAD, FORCE FEED 2 INTO REG 01	00000000
	63,0A03,01	LIT LOAD, FORCE FEED 1 INTO REG 00	00000000
	03,0A17,00	PRIORITY INTERRUPT, HALT EXECUTION	00000000
	03,0A17,00	GO, COMENCE EXECUTION	00000000
B		MACHINE STATUS TO THE PRINTER	
H			
01,000001	00,000005	00000007	00000002
01,000007	00,000031	00000000	00000000
01,000000	00,000000	00000000	00000000
01,000030	00,000000	00000000	00000000
01,000030	00,000000	00000000	00000000
01,000030	00,000000	00000000	00000000
01,000030	00,000000	00000000	00000000

END OF JOB

E









P	00030		
L	00236	FAULT INTERRUPT-EXECUTION ENDS *	
C	00214	NOT IMPLEMENTED-EXECUTION ENDS *	
C	00722	DIVIDE OVERFLOW - FAULT ENTERED *	
I2	30	17658	10CM FOR 20 BUFFERS FROM CARD HEADER
I2	31	04076	
I2	32	16758	10CM FOR 6 BUFFERS FROM CARD READER
I2	03	05120	
I2	04	16705	OUTPUT 10CM FOR 5 BUFFERS TO PRT
I2	35	08076	
I2	36	17655	OUTPUT 20 BUFFERS TO PRT
I2	37	10240	
I2	38	12336	REGISTER CONTAINING TWO BCL SPACE CHARACTERS
I2	11	C0040	
I2	15	C0030	
D	02048	00C30	BOTH EQUATIONS MUST BE IN STD FORM
D	02049	C0030	A (Y) PLUS B (X) EQUALS C
D	02050	00C31	Y COEFF OF 1ST EON
D	02C31	00C31	X COEFF OF 1ST EON
D	02032	00C33	CONSTANT OF 1ST EON
D	02033	00031	Y COEFF OF 2ND EON
D	02034	65545	X COEFF OF 2ND EON
D	02055	65545	CONSTANT OF 2ND EON
		63+0+15+01	LOAD 1 INTO REG. 12
		03+0+13+05	LOAD S91 WITH REG. 13
		12+1+00+17	STORE DOUBLE INTO 10CM
		35+0+07+00	INPUT 14 BUFFERS FROM CARD READER
		12+1+02+17	STORE DOUBLE INTO 10CM
		35+0+03+00	INPUT 6 BUFFERS FROM THE CARD READER
		01+2+12+00+01320	INITIALIZE BUFFER WORDS COUNT (20 PRT BUFFERS)
		01+2+11+00+10240	INITIALIZE OUTPUT BUFFER ADDR
		15+1+10+11	STORE (RA) INTO Y* AND INDEX BY 1 (STORE SPACES)
		02+0+12+11	DECREMENT BUFFER COUNTER
		45+1+375	COUNTER EQUAL ZERO
		01+2+14+00+04076	INITIALIZE BUFFER ADDRESS OF INPUT
		01+2+15+00+00C20	BUFFER COUNT
		01+2+11+00+10240	INITIALIZE DESTINATION BUFFER ADDR
		05+1+15+14	LOAD AND INDEX BY J
		15+1+15+11	STORE RA INTO Y* AND I'NDX Y*
		02+0+13+11	DECREMENT COUNTER
		45+1+374	COUNTER EQUAL ZERO
		22+2+11+00+00C26	ADD 26 TO BUFFER ADDR
		01+2+13+00+00C40	RESET - BUFFER WORD COUNT
		02+0+13+11	DECREMENT NEXT COUNTER (NO. OF BUFFERS)
		45+1+356	COUNTER EQUAL ZERO
		12+1+05+17	STORE DOUBLE INTO 10CM
		35+0+03+10	OUTPUT 14 BUFFERS TO PRT



```

63+0+15+01
03+0+15+05
LOAD SRI WITH A 1 FROM REG 13
INITIALIZE NEXT OUTPUT BUFFER ADDRESS
INITIALIZE NEXT BUFFER WORD COUNT (5 PRT BUFFERS)
BUFFER COUNT
INITIALIZE BUFFER ADDR OF SECOND INPUT BUFFER
STORE (RA) INTO Y+ AND INDEX BY 1 (STORE SPACES)
15+1+10+11
02+0+12+11
45+1+375
01+2+11+00+00C076
95+1+15+14
15+1+15+11
02+0+13+11
45+1+374
2+2+11+00+00C026
01+2+13+00+00C040
02+0+13+11
45+1+356
63+0+15+00
03+0+15+05
01+3+01+00+02C030
01+3+03+00+02031
01+3+03+00+02032
01+3+11+00+02033
01+3+13+00+02034
2+3+03+00+02035
26+0+03+03
21+0+00+10
25+3+00+17+02C040
94+1+052
12+3+07+06+00C014
01+2+02+00+00C030
01+3+01+00+02030
01+3+03+00+02031
01+3+03+00+02032
01+3+11+00+02033
01+3+13+00+02034
26+0+00+15
26+0+13+05
21+0+00+10
27+0+00+17
26+0+00+13
26+0+10+03
21+0+00+14
27+0+03+17

***RE-ENTRY POINT FOR REPETITIVE EXECUTION***
LOAD SRI WITH A 1 FROM REG 13
INITIALIZE NEXT OUTPUT BUFFER ADDRESS
INITIALIZE NEXT BUFFER WORD COUNT (5 PRT BUFFERS)
BUFFER COUNT
INITIALIZE BUFFER ADDR OF SECOND INPUT BUFFER
STORE (RA) INTO Y+ AND INDEX BY 1 (STORE SPACES)
DECREMENT BUFFER COUNTER
COUNTER EQUAL ZERO
REINITIALIZE BUFFER ADDR IN REG 9
LOAD AND INDEX BY J
STORE RA INTO Y+ AND INDEX Y+
DECREMENT COUNTER
COUNTER EQUAL ZERO
ADD 26 TO BUFFER ADDR
RESET BUFFER WORD COUNT
DECREMENT NEXT COUNTER (NO. OF BUFFERS)
COUNTER EQUAL ZERO
LOAD REG 13 WITH 0
LOAD SRI WITH 0
***CRAMER'S ROLL ALGORITHM*** STORE X OF EON 1
STORE Y COEFF, EON 1, INTO REG 03
STORE CONSTANT, EON 1, INTO REG 05
STORE X COEFF, EON 2, INTO REG 11
STORE Y COEFF, EON 2, INTO REG 13
STORE CONSTANT, EON 2, INTO REG 15
MULT RT DIAG OF DENOM, RESULT IN 00/01
SUBTRACT DOUBLE, RESULT OF DENOM, RESULT IN 10/11
COMPARE DENOM WITH ZERO
JUMP, IF EQUAL (ZERO DETERMINANT)
STORE DOUBLE, DENOM INTO 16/17
LOAD 00 INTO REG 00
RESTORE Y COEFF, EON 1, INTO REG 04
RESTORE X COEFF, EON 1, INTO REG 03
RESTORE CONSTANT OF EON 1 IN REG 05
RESTORE Y COEFF OF EON 2 IN REG 05
RESTORE X COEFF OF EON 2 IN REG 11
RESTORE CONSTANT OF EON 2 IN REG 15
X NUM LEFT DIAG HULT, RESULT IN CC/01
X NUM RT, 01AG HULT, RESULT IN 10/11
X NUM RESIDES IN REG 00/01
X NUM RESIDES IN REG 01
Y NUM LEFT DIAG HULT, RESULT REG 04/05
Y NUM RT, DIAG HULT, RESULT REG 14/15
DOUBLE SUBTRACT (EVAL NUM), RESULT 04/05
DIVIDE NUM/DENOM, Y RESIDES IN 05

```



```

01:2:07:00:16359      ***INT TO BCL CONVERSION*** TWICE BUFFER ADDR PLUS 1
63:0:03:00          LIT LOAD, C INTO REG 0
63:3:00:12          LIT DIVIDE, REG 0/1 BY 10
1C:3:03:07:00000    BYTE STORE, REG 7 MUST CONTAIN TWICE ADDR
44:1:07:31          LOCAL JUMP EQUAL (ZERO QUOTIENT)
63:0:07:00          LIT LOAD, C INTO REG 0
62:0:07:01          LIT SUBTRACT, 1 FROM REG 7
40:1:07:31          LOCAL JUMP
01:2:07:00:16633   LOAD CONSTANT, TWICE ADDR PLUS 1 IN REG. 7
53:0:04:00          LIT LOAD, C INTO REG 4
63:3:03:12          LIT DIVIDE, REC 4/5 BY 10
44:1:07:31          BYTE JUMP
63:0:04:00          JUMP EQUAL, CHECK FOR ZERO QUOTIENT
62:0:07:01          LIT LOAD, C INTO REG 4
4C:1:07:31          LIT SUBTRACT, 1 FROM REG 7
63:0:15:01          LOCAL JUMP
03:0:15:05          LOAD REG 13 WITH A 1
12:1:04:17          LOAD S61 WITH A 1
35:0:07:00          STORE DOUBLE INTO 10CM
03:0:05:00          DUMP 5 BUFFERS TO PRI
63:0:15:01          HALT
03:0:15:05          ***NO SOLUTION CASE***
2C:2:11:00:00178   LOAD SRI WITH A 1
01:2:13:00:00040   RECOMPUTE OUTPUT BUFFER ADDR FOR *NO SOLUTION*
05:1:15:14          REINITIALIZE COUNTER
02:0:13:11          LOAD AND INDEX BY 1
45:1:17:34          STORE RA INTO Y* AND INDEX Y*
12:1:04:17          DECREMENT COUNTER
03:0:04:00          COUNTER EQUAL ZERO
03:0:04:00          STORE DOUBLE INTO 10CM
03:0:04:00          DUMP 5 BUFFERS TO PRI
03:0:05:00          HALT

```





THIS IS A DEMONSTRATION PROGRAM OF THE AN/JYK20 EMULATOR.  
THE PROGRAM SOLVES TWO SIMULTANEOUS EQUATIONS BY CRAMER'S RULE.

THE INPUT COEFFICIENT VALUES AND CONSTANTS FOR EACH EQUATION MUST BE INSERTED  
USING LOADER CONTROL CARDS IN THE FOLLOWING LOCATIONS

1ST EQUATION. A1 IN LOCATION 2050 D.  
B1 IN LOCATION 2051 D.  
CONSTANT IN LOCATION 2052 D.

2ND EQUATION. A2 IN LOCATION 2053 D.  
B2 IN LOCATION 2054 D.  
CONSTANT IN LOCATION 2055 D.

THE RESULT IS.  
X >

2

1

TO CHANGE VARIABLES INSERT LOADER JCL HERE, OTHERWISE EXIT  
REINITIALIZE BUFFER WORD COUNT FOR BUFFER INIT.  
L 00C40  
L 00031  
D 02033  
D 02034  
D 02055  
G 00031  
X COEFF OF 1ST EQUATION  
Y COEFF OF 2ND EQUATION  
CONSTANT OF 1ST EQUATION  
CONSTANT OF 2ND EQUATION  
RE-EXECUTE PROGRAM AT ADDR 1055 DECIMAL

THE RESULT IS.

X >

NO SOLUTION

Y >

TO CHANGE VARIABLES INSERT LOADER JCL HERE, OTHERWISE EXIT  
END EXECUTION



## APPENDIX F. EMULATOR LISTING

This appendix provides a listing of the TRANSLANG assembler output of the AN/UUK-20 emulation. A source file copy of the emulator exists on disk as well as on cards. A microinstruction object file is also maintained on disk.

The listing is divided into four sections. The left most section contains the microinstruction address composed of four hexadecimal digits followed by a 56-bit microinstruction created from a TRANSLANG instruction. The center section contains the TRANSLANG source which includes labels, an instruction, and/or a comment field. The final number printed on the right most side of the listing is the sequence number of the TRANSLANG source statement. This number, printed in decimal, is created by a Burroughs software utility program called CARD-LIST. This number must be used when editing source programs on disk.



```

$MUDGE IED/UUK20
PROGRAM IED/UUK20-OBJECT
* * * * *
GREG1 = 0
GREG2 = 16
PSW = 32
BKPT = 33
STATUS2 = 34
NXTINSTR = 35
CLOCKTIME = 36
RTC = 37
WORKSPACE = 38
STACK = 44
I0CN = 50
HEXADDR = 120

CARD0UF = 122
CARD1X4 = 122
CARD5X6 = 122
CARD7X12 = 124
CARD7X16 = 125
CARD7X40 = 141
PRIMIBUFF = 153
CRIDUFF = 106
ERRORLIST = 206
PAGEREG = 768

* * * * *
WAIT SET GCL; WHEN GC1 THEN I L = AI;PAR2
COMP 16 = SAR
0 = MTR; SAVE
M2; AI - 1 = AI; IF SA1
M2; AI - 1 = AI; ELSE STEP
M2; AI - 1 = AI; M2; JUMP
M2; AI - 1 = AI; M2; JUMP
NEWCARD - 1 = MFCR

* * * * *
START:
* * * * *
0C00 4800 C000 0C20 C0F0
0C01 0098 00C1 401C 00F0
0C02 0000 0000 0030 C020
0C03 4812 00C3 003F 00F0
0C04 9809 A0E0 403C 1CF0
0C05 5819 0003 0030 C0FC
0C06 7628 A0C3 003C C0FC
0C07 0000 0000 003C C04F

* * * * *
CONTROL:
* * * * *
0C08 4809 20C3 0C1C C0F0
0C09 074C 00C0 0030 C0E0
0C0A C010 00C0 0030 0060
0C0B 48C9 20C1 C030 40F0

* * * * *
MAIN MEMORY ADDRESS MAPPING * * * * *
0C0C1C00 D
00002F00 D
00043C00 D
00004000 D
00005000 D
00066C00 D
00007C00 D
0C0E6000 D
0C0E9000 D
00010C00 D
00011C00 D
0C012C00 D
0C013C00 D
00014000 D
00015C00 D
00016C00 D
0C017C00 D
0C018C00 D
0C019C00 D
0C020C00 D
0C021C00 D
0C022C00 D
0C023C00 D
0C024C00 D
0C025C00 D
0C026C00 D
0C027C00 D
0C028C00 D
0C029C00 D
0C030C00 D
0C031C00 D
0C032C00 D
0C033C00 D
0C034C00 D
0C035C00 D
00036C00 D
0C037C00 D
0C038C00 D
00039C00 D
00040C00 D
00041C00 D
00042C00 D
00043C00 D
00044C00 D
00045C00 D
00046C00 D
00047C00 D
00048C00 D
0C049C00 D
0C050C00 D
0C051C00 D
00052C00 D
0C053C00 D
0C054C00 D
00055C00 D
0C056C00 D
0C057C00 D

* * * * *
ADDRESS OF GENERAL REGISTER STACK ONE
ADDRESS OF GENERAL REGISTER STACK TWO
PROGRAM STATUS WORD (PAR & SR #1)
BREAKPOINT REGISTER
STATUS REGISTER TWO
ADDRESS OF NEXT INSTRUCTION
TIME OF EXECUTION
REAL TIME CLOCK
TEMPORARY STORAGE STACK
TEMPORARY STORAGE STACK
INPUT OUTPUT COMMAND WORDS (THRU 53)
HEX ADDR TO BE PRINTED (TWO WORD VAL)
CARDBUFFER ADDRESSES
ADDRESS OF CARD BUFFER
ADDRESS OF CARD COLS 1-4
ADDRESS OF CARD COLS 5-8
ADDRESS OF CARD COLS 9-12
ADDRESS OF CARD COLS 13-16
ADDRESS OF CARD COLS 17-80. END OF CARD00004C00 D
PRINT BUFFER LOCATION
CRT BUFR (20 WORDS)
LIST OF POSSIBLE ERRORS
PAGE ADDRESS REGISTERS STACK BASE (0-25)
LOADER
BEGIN PROGRAM BY ZEROING MAIN MEMORY
RESTART RETURN POINT
IF CRT INPUT DESIRED, PUT IRO SW ON
TOGGLE EXECUTION BY SINGLE STEP
* * * * *
THIS ROUTINE WILL READ COLUMNS 1-4 AND
EXAMINE COLUMN 1 FOR A CONTROL CARD
IDENTIFIER. IF THE CARD IS A CONTROL
THE APPROPRIATE ROUTINE WILL BE CALLED.
LOAD ADDRESS OF CARD COLUMNS 1-4.
READ COLUMNS 1-4
LOAD MSR OF AI WITH 00111111

```



0005	9000	D	% FILL LSB OF R REGISTER WITH CHARACTER	00059000 D
0006	9000	D	% FROM COLUMN ONE	00069000 D
0006	1000	F		00061000 F
0006	2000	D	% BCL CODE FOR *B*	00062000 D
0006	3000	C	% CHECK FOR *B*	00063000 C
0006	4000	D	% JUMP TO PREAPPOINT ROUTINE	00064000 D
0006	5000	D		00065000 D
0006	6000	D	% BCL CODE FOR *D*	00066000 D
0006	6000	D	% CHECK FOR *D*	00066000 D
0006	6000	D	% JUMP TO DATA ROUTINE	00066000 D
0006	7000	D		00067000 D
0006	7000	D	% BCL CODE FOR *C*	00067000 D
0006	7000	D	% CHECK FOR *C*	00067000 D
0006	7000	D	% JUMP TO DATA ROUTINE	00067000 D
0006	8000	D		00068000 D
0006	8000	D	% BCL CODE FOR *G*	00068000 D
0006	8000	D	% CHECK FOR *G*	00068000 D
0006	8000	D	% JUMP TO GO ROUTINE	00068000 D
0006	8000	D		00068000 D
0006	9000	D	% BCL CODE FOR *I*	00069000 D
0006	9000	D	% CHECK FOR *I*	00069000 D
0006	9000	D	% JUMP TO THE SET INDEX REG ROUTINE	00069000 D
0006	9000	D		00069000 D
0006	9000	D	% BCL CODE FOR *L*	00069000 D
0006	9000	D	% CHECK FOR *L*	00069000 D
0006	9000	D	% JUMP TO LOAD ROUTINE	00069000 D
0006	9000	D		00069000 D
0006	9000	D	% BCL CODE FOR *P*	00069000 D
0006	9000	D	% CHECK FOR *P*	00069000 D
0006	9000	D	% JUMP TO SET PAGING BIT ROUTINE	00069000 D
0006	9000	D		00069000 D
0006	9000	D	% BCL CODE FOR *R*	00069000 D
0006	9000	D	% CHECK FOR *R*	00069000 D
0006	9000	D	% JUMP TO RESERVE SPACE ROUTINE	00069000 D
0006	9000	D		00069000 D
0006	9000	D	% BCL CODE FOR *S*	00069000 D
0006	9000	D	% CHECK FOR *S*	00069000 D
0006	9000	D	% JUMP TO SWITCHES ROUTINE	00069000 D
0006	9000	D		00069000 D
0006	9000	D	% BCL CODE FOR *T*	00069000 D
0006	9000	D	% CHECK FOR *T*	00069000 D
0006	9000	D	% JUMP TO TRACE ROUTINE	00069000 D
0006	9000	D		00069000 D
0006	9000	D	% BCL CODE FOR *C*	00069000 D
0006	9000	D	% CHECK FOR *C*	00069000 D
0006	9000	D	% JUMP TO CHARACTER STRING ROUTINE	00069000 D
0006	9000	D		00069000 D
0006	9000	D	% BCL CODE FOR BLANK	00069000 D
0006	9000	D	% CHECK FOR BLANK	00069000 D
0006	9000	D	% JUMP TO THE INSTRUCTION HANDLING	00069000 D
0006	9000	D		00069000 D
0006	9000	D	% BCL CODE FOR **	00069000 D
0006	9000	D	% CHECK FOR **	00069000 D
0006	9000	D	% JUMP TO MACHINE STATUS ROUTINE	00069000 D
0006	9000	D		00069000 D
0006	9000	D	% DEFAULT, GET NEW CARD	00069000 D
0006	9000	D		00069000 D





LOAD:

```

0C37 1809 00C0 0B30 00FC      * SET UP MEMORY INTO 256 PAGES OF 256
0C38 1809 0643 0B1C 00C0      * WORDS (32 BIT) EACH. THE PAGE NO. IN
0C39 3000 00C0 0070 00C0      * THE "L" CARD (COL 5-8) WILL RE
0C3A 07E0 00C0 0030 00E0      * TRANSLATED INTO THE BASE ADDRESS OF
0C3B 1812 00C0 00E1 00F0      * THE SELECTED PAGE AND STORED IN
                                * THE NEXTINST REG TO BE UTILIZED AS THE
                                * BASE ADDRESS TO LOAD THE PROGRAM.
                                * 7ERO B AND MIR
                                * SET UP ADDRESS OF PAGE REGISTER
0C3C 9809 00C0 0030 10F0      * SET UP CTR FOR 255 + 1 ITERATIONS
0C3D 9C08 00C0 0032 00F0      * THIS LOOP WILL INITIALIZE 256 PAGE ADDR
                                * REGISTERS TO THEIR BASE ADDRESSES.
                                * TRANSFER MIR TO B AFTER MEMORY WRITE
                                * INTO THE NEXT PAGE ADDRESS
                                * AND INCREMENT LOOP COUNTER
                                * LOAD ADDR OF COL 1-4
0C3E 9429 0F46 001C 00FC      * READ COLS 1-4
0C3F 1809 20C3 001C 00F0      * GET OCTAL VALUE OF PAGE NO. IN COL 6-8
0C40 07AC 00C0 0030 00C0      * MULT PAGE NO. BY 256 TO GET BASE ADDR
0C41 00F0 00C0 003C 00E0      * SAR % INTO NEXTINST REG WHICH WILL
0C42 0109 00C0 0030 00F0      * WRITE THE BASE ADDRESS OF SELECTED PAGE
0C43 0230 00C0 003C 00E0      * TO BE USED AS THE BASE ADDRESS TO LOAD
0C44 9809 20C3 001C 00F0      * THE PROGRAM.
0C45 0110 00C0 0030 0040      * THIS ROUTINE WILL READ THE CONTENT OF
                                * THE MEMORY ADDRESS IN MAR2.
                                * PERFORM READ
                                * READ CONTENTS OF MAR2 INTO B.
                                * THIS ROUTINE RETRIEVES THE PAR CONTENTS
                                * AND STATUS REG 1 CONTENTS AND PARKS
                                * THEM INTO A1 AND THEN JUMPS TO THE
                                * EMULATOR
                                * GET ADDRESS IN COL. 5-8 OF *60* CARD
                                * OFFSET ADDRESS BY 1024
                                * ADDRESS OF PSW
                                * RETRIEVE CONTENTS OF PSW
                                * STORE COMPLETE PSW INTO MIR AND A1
                                * LOAD PAR REG WITH START ADDRESS OF PROGRAM
                                * START EMULATION OF UYK2C
                                * START CLOCK AND FETCH FIRST INST.
                                *
                                *
                                *
                                * GET ADDRESS FIELD FROM COLUMNS 4-7
                                * OF INPUT CARD. ADDRESS WILL BE IN
                                * DECIMAL. (N & H STAND FOR CARD COLS)
                                *
                                * GET FREQUEIDING MEMORY WORD FROM SNI
                                * SAVE RETURN
                                * ISOLATE LSB OF CARD(N-3)XP
0C46 0110 00C0 0030 0040      *
0C47 8B09 00C0 003C 00C0      *
0C48 AC28 00C0 0C00 00F0      *
0C49 0120 00C0 0030 00E0      *
0C4A 8B09 00C1 4C00 00F0      *
0C4B A200 00C0 0030 00A0      *
0C4C 8B09 AC80 4070 00F0      *
0C4D 8B09 20C3 001C 00F0      *
0C4E 8B09 AC5C 4C30 00F0      *
0C4F 8B09 AC5C 4C30 00E0      *
0C50 0130 00C0 0030 00E0      *
0C51 0140 00C0 0030 0040      *
0C52 4B09 00C0 0C20 00F0      *
0C53 8B09 0640 7C20 00F0      *
0C54 8B09 0C41 0B30 40FC      *
0C55 0300 00C0 003C 0090      *

```



```

0 R = A1
00178000 0
00179000 0
00180000 0
00181000 0
00182000 0
00183000 0
00184000 0
00185000 0
00186000 0
00187000 0
00188000 0
00189000 0
00190000 0
00191000 0
00192000 0
00193000 0
00194000 0
00195000 0
00196000 0
00197000 0
00198000 0
00199000 0
00200000 0
00201000 0
00202000 0
00203000 0
00204000 0
00205000 0
00206000 0
00207000 0
00208000 0
00209000 0
00210000 0
00211000 0
00212000 0
00213000 0
00214000 0
00215000 0
00216000 0
00217000 0
00218000 0
00219000 0
00220000 0
00221000 0
00222000 0
00223000 0
00224000 0
00225000 0
00226000 0
00227000 0
00228000 0
00229000 0
00230000 0
00231000 0
00232000 0
00233000 0
00234000 0
00235000 0
00236000 0
00237000 0
00238000 0
00239000 0
00240000 0
00241000 0
00242000 0
00243000 0
00244000 0
00245000 0
00246000 0
00247000 0
00248000 0
00249000 0
00250000 0
00251000 0
00252000 0
00253000 0
00254000 0
00255000 0
00256000 0
00257000 0
00258000 0
00259000 0
00260000 0
00261000 0
00262000 0
00263000 0
00264000 0
00265000 0
00266000 0
00267000 0
00268000 0
00269000 0
00270000 0
00271000 0
00272000 0
00273000 0
00274000 0
00275000 0
00276000 0
00277000 0
00278000 0
00279000 0
00280000 0
00281000 0
00282000 0
00283000 0
00284000 0
00285000 0
00286000 0
00287000 0
00288000 0
00289000 0
00290000 0
00291000 0
00292000 0
00293000 0
00294000 0
00295000 0
00296000 0
00297000 0
00298000 0
00299000 0
00300000 0
00301000 0
00302000 0
00303000 0
00304000 0
00305000 0
00306000 0
00307000 0
00308000 0
00309000 0
00310000 0
00311000 0
00312000 0
00313000 0
00314000 0
00315000 0
00316000 0
00317000 0
00318000 0
00319000 0
00320000 0
00321000 0
00322000 0
00323000 0
00324000 0
00325000 0
00326000 0
00327000 0
00328000 0
00329000 0
00330000 0
00331000 0
00332000 0
00333000 0
00334000 0
00335000 0
00336000 0
00337000 0
00338000 0
00339000 0
00340000 0
00341000 0
00342000 0
00343000 0
00344000 0
00345000 0
00346000 0
00347000 0
00348000 0
00349000 0
00350000 0
00351000 0
00352000 0
00353000 0
00354000 0
00355000 0
00356000 0
00357000 0
00358000 0
00359000 0
00360000 0
00361000 0
00362000 0
00363000 0
00364000 0
00365000 0
00366000 0
00367000 0
00368000 0
00369000 0
00370000 0
00371000 0
00372000 0
00373000 0
00374000 0
00375000 0
00376000 0
00377000 0
00378000 0
00379000 0
00380000 0
00381000 0
00382000 0
00383000 0
00384000 0
00385000 0
00386000 0
00387000 0
00388000 0
00389000 0
00390000 0
00391000 0
00392000 0
00393000 0
00394000 0
00395000 0
00396000 0
00397000 0
00398000 0
00399000 0
00400000 0
00401000 0
00402000 0
00403000 0
00404000 0
00405000 0
00406000 0
00407000 0
00408000 0
00409000 0
00410000 0
00411000 0
00412000 0
00413000 0
00414000 0
00415000 0
00416000 0
00417000 0
00418000 0
00419000 0
00420000 0
00421000 0
00422000 0
00423000 0
00424000 0
00425000 0
00426000 0
00427000 0
00428000 0
00429000 0
00430000 0
00431000 0
00432000 0
00433000 0
00434000 0
00435000 0
00436000 0
00437000 0
00438000 0
00439000 0
00440000 0
00441000 0
00442000 0
00443000 0
00444000 0
00445000 0
00446000 0
00447000 0
00448000 0
00449000 0
00450000 0
00451000 0
00452000 0
00453000 0
00454000 0
00455000 0
00456000 0
00457000 0
00458000 0
00459000 0
00460000 0
00461000 0
00462000 0
00463000 0
00464000 0
00465000 0
00466000 0
00467000 0
00468000 0
00469000 0
00470000 0
00471000 0
00472000 0
00473000 0
00474000 0
00475000 0
00476000 0
00477000 0
00478000 0
00479000 0
00480000 0
00481000 0
00482000 0
00483000 0
00484000 0
00485000 0
00486000 0
00487000 0
00488000 0
00489000 0
00490000 0
00491000 0
00492000 0
00493000 0
00494000 0
00495000 0
00496000 0
00497000 0
00498000 0
00499000 0
00500000 0
00501000 0
00502000 0
00503000 0
00504000 0
00505000 0
00506000 0
00507000 0
00508000 0
00509000 0
00510000 0
00511000 0
00512000 0
00513000 0
00514000 0
00515000 0
00516000 0
00517000 0
00518000 0
00519000 0
00520000 0
00521000 0
00522000 0
00523000 0
00524000 0
00525000 0
00526000 0
00527000 0
00528000 0
00529000 0
00530000 0
00531000 0
00532000 0
00533000 0
00534000 0
00535000 0
00536000 0
00537000 0
00538000 0
00539000 0
00540000 0
00541000 0
00542000 0
00543000 0
00544000 0
00545000 0
00546000 0
00547000 0
00548000 0
00549000 0
00550000 0
00551000 0
00552000 0
00553000 0
00554000 0
00555000 0
00556000 0
00557000 0
00558000 0
00559000 0
00560000 0
00561000 0
00562000 0
00563000 0
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00569000 0
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00578000 0
00579000 0
00580000 0
00581000 0
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00674000 0
00675000 0
00676000 0
00677000 0
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00679000 0
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00684000 0
00685000 0
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00687000 0
00688000 0
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00690000 0
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00693000 0
00694000 0
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00696000 0
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00698000 0
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00700000 0
00701000 0
00702000 0
00703000 0
00704000 0
00705000 0
00706000 0
00707000 0
00708000 0
00709000 0
00710000 0
00711000 0
00712000 0
00713000 0
00714000 0
00715000 0
00716000 0
00717000 0
00718000 0
00719000 0
00720000 0
00721000 0
00722000 0
00723000 0
00724000 0
00725000 0
00726000 0
00727000 0
00728000 0
00729000 0
00730000 0
00731000 0
00732000 0
00733000 0
00734000 0
00735000 0
00736000 0
00737000 0
00738000 0
00739000 0
00740000 0
00741000 0
00742000 0
00743000 0
00744000 0
00745000 0
00746000 0
00747000 0
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00750000 0
00751000 0
00752000 0
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00759000 0
00760000 0
00761000 0
00762000 0
00763000 0
00764000 0
00765000 0
00766000 0
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00778000 0
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00785000 0
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00787000 0
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00789000 0
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00794000 0
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00852000 0
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00854000 0
00855000 0
00856000 0
00857000 0
00858000 0
00859000 0
00860000 0
00861000 0
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00863000 0
00864000 0
00865000 0
00866000 0
00867000 0
00868000 0
00869000 0
00870000 0
00871000 0
00872000 0
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00874000 0
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00876000 0
00877000 0
00878000 0
00879000 0
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00881000 0
00882000 0
00883000 0
00884000 0
00885000 0
00886000 0
00887000 0
00888000 0
00889000 0
00890000 0
00891000 0
00892000 0
00893000 0
00894000 0
00895000 0
00896000 0
00897000 0
00898000 0
00899000 0
00900000 0
00901000 0
00902000 0
00903000 0
00904000 0
00905000 0
00906000 0
00907000 0
00908000 0
00909000 0
00910000 0
00911000 0
00912000 0
00913000 0
00914000 0
00915000 0
00916000 0
00917000 0
00918000 0
00919000 0
00920000 0
00921000 0
00922000 0
00923000 0
00924000 0
00925000 0
00926000 0
00927000 0
00928000 0
00929000 0
00930000 0
00931000 0
00932000 0
00933000 0
00934000 0
00935000 0
00936000 0
00937000 0
00938000 0
00939000 0
00940000 0
00941000 0
00942000 0
00943000 0
00944000 0
00945000 0
00946000 0
00947000 0
00948000 0
00949000 0
00950000 0
00951000 0
00952000 0
00953000 0
00954000 0
00955000 0
00956000 0
00957000 0
00958000 0
00959000 0
00960000 0
00961000 0
00962000 0
00963000 0
00964000 0
00965000 0
00966000 0
00967000 0
00968000 0
00969000 0
00970000 0
00971000 0
00972000 0
00973000 0
00974000 0
00975000 0
00976000 0
00977000 0
00978000 0
00979000 0
00980000 0
00981000 0
00982000 0
00983000 0
00984000 0
00985000 0
00986000 0
00987000 0
00988000 0
00989000 0
00990000 0
00991000 0
00992000 0
00993000 0
00994000 0
00995000 0
00996000 0
00997000 0
00998000 0
00999000 0

```

```

% TEST FOR BLANK ADDR FIELD
% IF TRUE THEN 0 = B1 STEP ELSE SKIP % IF BLANK ADDR TREAT AS 0
% INPUT EQUAL C IN 0 REG
% PACKED-1 = MPCR
% DECODED-1 = CPCR
% THIS ROUTINE PERFORMS A MEMORY WRITE
% NEEDED FOR AMPCR ASSIGN PRIOR TO JUMP
% THIS ROUTINE PERFORMS A MEMORY WRITE
% CALL TOP TO READ NEXT CARD THEN
% JUMP TO CONTROL SPACE CARD ROUTINE.
% THIS ROUTINE INSERTS SPACES INTO
% HEXADR AND CARDBUFFER
% REMAINING 11 WORDS ARE FILLED WITH
% SPACES FOR ECHO PRINT ROUTINE.
% 133 WORDS WILL HAVE SPACES
% PUT SPACES INTO MIR
% WRITE SPACES INTO MEMORY
% IF MAR2,INC,STEP ELSE SKIP
% RETRIEVE CARD
% CARDBUF ADDRESS INTO B
% % IRC INDICATES CRT INPUT
% % CONTENTS FOR MAILBOX
% EXTOP - 1 = CPCR
% BCRO - 1 = MPCR
% IF IRC THEN STEP ELSE SKIP % IRC -> FALSE THEN ECHO PRT (PTR)
% CONTROLCD - 1 = MPCR
% JUMP TO CONTROL CARD ROUTINE
% LIT = MIR
% HEXADR = LIT
% L = BBI
% COMP 16 = SAR
% MIR CONTAINS 1/HEXADR
% ECHO CARD READ
% JUMP TO EXITOP ROUTINE
% UNSUCCESSFUL TO OPERATION
% JUMP TO CONTROL CARD ROUTINE
% THIS ROUTINE PERFORMS THE IOP INTERFACE
% BY PASSING TO THE IOP THE FUNCTION
% AND THE ADDRESSES IN THE MAILBOX. THE IOP

```



```

00239C00 D
0C2940C0 D
0C2941C0 D
0C2942C0 D
0C2943C0 D
0C2944C0 C
0C2945C0 D
0C2946C0 D
0C2947C0 D
0C2948C0 D
0C2949C0 D
0C2950C0 D
0C2951C0 D
0C2952C0 D
0C2953C0 D
0C2954C0 C
0C2955C0 D
0C2956C0 D
0C2957C0 D
0C2958C0 D
0C2959C0 D
0C2960C0 D
0C2961C0 D
0C2962C0 D
0C2963C0 D
0C2964C0 D
0C2965C0 D
0C2966C0 D
0C2967C0 D
0C2968C0 D
0C2969C0 D
0C2970C0 D
0C2971C0 D
0C2972C0 D
0C2973C0 D
0C2974C0 D
0C2975C0 D
0C2976C0 D
0C2977C0 D
0C2978C0 D
0C2979C0 D
0C2980C0 D
0C2981C0 D
0C2982C0 D
0C2983C0 D
0C2984C0 D
0C2985C0 D
0C2986C0 D
0C2987C0 D
0C2988C0 D
0C2989C0 D
0C2990C0 D
0C2991C0 C
0C2992C0 D
0C2993C0 D
0C2994C0 D
0C2995C0 D
0C2996C0 D
0C2997C0 D
0C2998C0 D
0C2999C0 D

SET GC2 WHEN GC2 THEN NOT 0 = MAR2
MH2I IF SAI
WHEN SAI THEN 0J SET INI
IF INT
WHEN INT THEN STEP
BEYI MR2I IF ROC
WHEN ROC THEN NOT 0J RESET GC2
IF ABT THEN JUMP ELSE RETN
X
X
X

OUTPUTI:
MH2I IF SAI
WHEN SAI THEN 0J JUMP
X
X
X

CRTINI:
LIT L = A2
COMP 16 = SARI 6 = LIT
OR B = B
JUMP
X
X
X

PACKEDI:
X
X THIS ROUTINE MUST BE PASSED A 32 BIT
X WORD IN UNPACKED DECIMAL FORM(4 DIGIT
X DECIMAL NUMBERS). THE NUMBER IS PASSED
X IN A1. THE PACKED DECIMAL EQUIVALENT
X OF THE NUMBER IS RETURNED IN B REGISTER.
X WHICH CONSISTS OF AN 8 DIGIT DECIMAL
X THIS STEP IS OMITTED FOR A 4 DIGIT MC.
X ZERO MIR
X SET COUNTER TO PERFORM LOOP 4 TIMES
X ELIMINATE HIGH ORDER 4 BITS OF MSB CHARACTER
X SHIFT A1 RIGHT 28 BITS AND *OR* WITH
X MIR AND PLACE IN B REGISTER
X LEFTMOST DIGIT NOW IN HIGH ORDER
X POSITION OF MIR.
X A1J STEP ELSE SKIP
X SHIFT NEXT DIGIT
X INTO *POS. FOR NEXT PASS THROUGH LOOP
X BRANCH TO TOP OF LOOP
X CHECK TO SEE IF AN 8 DIGIT NUMBER
X JOIN TO THE END OF THE ROUTINE
X PREPARE MIR TO SEND NEXT *A* INPUT.
X B NOW CONTAINS LOW ORDER 4 DIGITS
X OF AN 8 DIGIT NUMBER.
X WHEN READ COMPLETE, SET A1 EQUAL TO B
X BRANCH TO THE TOP OF THE LOOP
X RETURN TO CALLING ROUTINE WITH PACKED
X NUMBER IN B REGISTER
X
X THIS ROUTINE WILL CONVERT DECIMAL
X NUMBERS INTO THEIR OCTAL EQUIVALENTS.
X THIS ROUTINE REQUIRES A PACKED DECIMAL
X NUMBER PASSED VIA THE D REGISTER. THE

```

```

0C7A 1C86 C002 001C 00FC
0C7B 9809 00C0 0030 1CFC
0C7C 9F08 00C0 0000 00F0
0C7D 0809 00C0 00C0 00FC
0C7E 0808 00C0 0030 00FC
0C7F 8809 00C0 00C0 00FC
0C80 AC08 0C42 0000 00FC
0C81 682F 00C0 0000 00FC

0C92 9809 0003 0C30 1CFC
0C93 9C28 00C0 0030 00F0

0C94 4809 2001 200C 00F0
0C95 0800 0003 0C3C 00AC
0C96 4809 0C52 0030 00FC
0C97 482D 0003 0030 00FC

0C98 49C9 0003 0C30 00F0
0C99 4809 0003 0C30 00F0
0C9A 4809 00C0 0001 00F0
0C9B 3030 00C0 0C30 00B0

0C9C 4809 4001 4C30 00F0
0C9D 4809 40D0 8F3C 00F0
0C9E 4809 0C41 0C32 00F0

0C9F 580E 40C1 4C30 00F0

0C90 086C 00C0 0030 0040
0C91 2819 00C0 0000 00FC
0C92 01C0 00C0 0C30 004C

0C93 4809 0C45 001C 00F0
0C94 8809 00C0 0C30 00FC

0C95 AC08 0C40 4C30 00F0
0C96 0890 00C0 0C30 0040

0C97 482D 00C0 0C30 00FC

```



```

% OCTAL EQUIVALENT WILL BE RETURNED IN B. 0C294600 U
% PACKED RESULTS ARRIVE IN B REG 0C294600 D
% CLEAR B REGISTER 0C300000 D
% SET COUNTER FOR 7 ITERATIONS. 0C301000 D
% 0C302000 D
% 0C302600 D
% PLACE DECIMAL NUMBER IN A1 AND CLEAR B. 0C303000 D
% PUT HIGH ORDER 4 BITS OF A1 INTO 0C304000 D
% LOW ORDER 4 BITS OF A3. 0C305000 D
% PREPOSITION NEXT DECIMAL DIGIT IN A1. 0C306000 D
% MULT DECIMAL DIGIT BY 8 0C307000 D
% 0C308000 D
% MULT DECIMAL DIGIT BY 2, INCREMENT CTR 0C309000 D
% EFFECTIVELY MULTI BY A FACTOR OF 1C. 0C310000 D
% PARTIAL SUM OF CONVERSION 0C311000 D
% SKIP 8 GET LS DIGIT FROM A1 IF DONE 0C312000 D
% GO TO TOP OF LOOP 0C313000 D
% 0C314000 C
% ADD LS DIGIT TO P AND RETURN OCTAL 0C315000 D
% VALUE IN B REGISTER. 0C316000 D
% 0C317000 D
% 0C318000 D
% 0C319000 D
% CONVERT DECIMAL DATA IN COL 13-20 INTO 0C320000 D
% COL 4 AND STORE AT THE ADDRESS IN 0C321000 D
% COL 4-8 0C322000 D
% 0C323000 D
% RETRIEVE ADDR IN COL 4-8 IN OCTAL 0C324000 D
% TRANSFER ADDR TO A3 REG 0C325000 D
% LOAD ADDRESS OF COL 13-14 0C326000 D
% 0C327000 D
% READ IN COL 13-16 0C328000 D
% 0C329000 D
% PACK DATA IN COL 13-20 0C330000 D
% SWITCH TEMP ADDRESS STORAGE 0C331000 D
% CONVERT DECIMAL TO OCTAL 0C332000 D
% HIR CONTAINS DATA IN OCTAL 0C333000 D
% SET UP LOGICAL TEST FOR BLANK ADDR 0C334000 D
% 0C335000 D
% IF ADDR = 0 AID DATA IN NEXT ADDR 0C336000 D
% PUT MEMORY ADDR IN MAR2 FOR WRITE OP 0C337000 D
% WRITE DATA IN MEMORY AND GET NEXT CARD 0C338000 C
% 0C339000 C
% THIS ROUTINE WILL INSERT DATA INTO THE 0C340000 C
% ADDRESS CONTAINED IN THE NXTINSTR. 0C341000 C
% REGISTER DATA TO BE WRITTEN IS IN HIR. 0C342000 C
% PUT ADDR OF NEXTINST INTO MAR2, A2 0C343000 C
% 0C344000 D
% READ CONTENTS OF NXTINSTR 0C345000 D
% PLACE CONTENTS OF NXTINSTR INTO MAR2 0C346000 D
% PLACE DATA AT THAT ADDRESS(MAR2) 0C347000 D
% 0C348000 D
% CREATE NEXT ADDR FOR NXTINSTR 0C349000 D
% WRITE NEW ADDR IN NXTINSTR 0C350000 D
% REG. AND GET THE NEXT CARD 0C351000 D
% 0C352000 D
% THIS ROUTINE WILL EXAMINE COL 2 FOR 0C353000 D
% THE GENERAL REGISTER STACK NO. AND 0C354000 D
% COL 7-B FOR THE REGISTER NO. THE 0C355000 D
% CONTENTS OF COL 13-20(ONLY 16-20 USED)0C356000 D
% WILL THEN BE CONVERTED TO OCTAL AND 0C357000 D

```

```

B = A1
D = B
C = MIR, LCTR
6 = LIT

TOPDECT: A1 R = A3
COMP 4 = SAR
A1 L = A1
A3 + B L = A3, END
COMP 3 = SAR
B L = B, INC
COMP 1 = SAR
A3 + B = B
IF COV THEN A1 R = A3
TOPDEC - 1 = HPCR
A3 = SAR
A3 + B = B

JUMP

DATA:
GETADDR - 1 = CPCR
B = A3
LIT = MAR2
CARD013X16 = LIT
INPUT - 1 = CPCR
B = A1
PACKED - 1 = CPCR
A3 = A2
DECOCT - 1 = CPCR
B = HIR
A2 EOL 0
IF TRUE THEN STEP ELSE SKIP
INLINE - 1 = HPCR
A2 = MAR2
OUT - 1 = HPCR

INLINE 1
LIT = MAR2/A2
NXTINSTR = LIT
INPUT - 1 = CPCR
B = MAR2
OUTPUT1 - 1 = CPCR
R + 1 = HIR
A2 = MAR2
OUT - 1 = HPCR

SETINSTRREG:

```

```

CC98 4809 0C43 0C3C 00FC
CC99 4809 0C0C 0C0C 00FC
CC9A 4809 0C0C 0C31 00FC
CC9B 0060 00C3 0070 00E0
CC9C 4809 4000 9C3C 00FC
CC9D 0C20 00C0 0030 0030
CC9E 4809 40C1 4C70 00FC
CC9F 4809 4C41 1830 00FC
CCAA 90C0 0000 0030 0030
CCAB 4809 4C41 083C 00FC
CCAC 3000 00C0 0C30 0C30
CCAD 4809 4C43 0C70 00FC
CCAE 4809 4C43 0C70 00FC
CCAF 0870 00C0 0000 0060
CCB0 4809 4C00 2030 00FC
CCB1 097C 0000 0000 0060
CCB2 4809 0C40 0C30 00FC
CCB3 4809 0C12 003C 00FC
CCB4 4809 00C0 003C 00FC
CCB5 010C 0000 0070 0040
CCB6 4809 0C03 0C1C 00FC
CCB7 05EC 0000 0070 0040
CCB8 4809 2000 201C 00FC
CCB9 0C20 00C0 0030 00E0
CCBA 0460 00C0 0030 00E0
CCBB 4809 0C43 0C1C 00FC
CCBC 0810 00C0 0000 0060
CCBD 4809 0C45 0030 00FC
CCBE 4809 0C03 0C1C 00FC
CCBF 05E0 00C0 0C30 0040

```





```

06C0 084C 0003 0000 0020
06C1 4809 0041 0020 0030
06C2 000C 0070 0020 0030
06C3 4809 0040 0020 0040
06C4 4809 480E 0020 0040
06C5 4809 0541 0020 0040
06C6 4800 0000 0020 0030
06C7 4809 0541 0028 0040
06C8 0000 0003 0000 0030
06C9 4809 2003 001C 0040
06CA 0780 00C3 0000 00EC
06CB 046C 00C3 0070 0060
06CC 4809 0541 003C 0040
06CD 0000 0000 0020 0020
06CE 4809 0540 0000 00F0
06CF 088C 00F3 0070 0060
06D0 0070 0000 0020 0060
06D1 4809 0000 003C 20F0
06D2 4809 0F43 000C 00F0
06D3 0000 0000 003C 0040
06D4 4809 AC41 002C 00F0
06D5 0700 00C0 0030 0000
06D6 4809 20C3 001C 00F0
06D7 046C 0003 0030 0060
06D8 4809 0000 003C 20F0
06D9 4809 0000 003C 20F0
06DA 48C9 0F43 801C 00F0
06DB 0000 00C3 0070 0040
06DC 4809 0543 0030 0040
06DD 05EC 0000 0070 0040

```

```

06DE 4809 0000 00C0 00F0
06DF 4809 0C41 4C70 00F0
06E0 0000 0000 0070 0030
06E1 4809 A0F0 0030 00F0
06E2 0000 00C3 003C 003C
06E3 4809 20C3 001C 00F0
06E4 0200 0000 0070 00E0
06E5 0460 00C0 0000 0060
06E6 4809 A152 003C 00F0
06E7 0290 0000 0070 00E0
06E8 6A19 A152 003C 00F0
06E9 01E0 00C0 0000 0040
06EA 0809 00C0 0000 00E0
06EB 0809 00C0 0000 00E0
06EC 01FC 0000 0000 00E0
06ED 020C 0003 0000 0040

```

```

06EE 4809 00C1 4000 00F0
06EF 4800 00C0 0070 0010
06F0 4809 00C3 009C 0060
06F1 081C 00C3 0090 0060

```

```

* STORED IN THE DESIRED GENERAL REGISTER-00358000 C
* RELOAD COL 1 - 4 00359000 D
* ISOLATE COLUMN 2 00361000 D
00361000 D
00362000 D
00363000 D
00364000 D
00365000 D
00366000 D
00367000 D
00368000 D
00369000 D
00370000 D
00371000 D
00372000 D
00373000 D
00374000 D
00375000 D
00376000 D
00377000 D
00378000 D
00379000 D
00380000 D
00381000 D
00382000 D
00383000 D
00384000 D
00385000 D
00386000 D
00387000 D
00388000 D
00389000 D
00390000 D
00391000 D
00392000 D
00393000 D
00394000 D
00395000 D
00396000 D
00397000 D
00398000 D
00399000 D
00400000 D
00401000 D
00402000 D
00403000 D
00404000 D
00405000 D
00406000 D
00407000 D
00408000 D
00409000 D
00410000 D
00411000 D
00412000 D
00413000 D
00414000 D
00415000 D
00416000 D
00417000 D

```

```

* B IS NOW OXGEN REG. NO., 13 OR 14 (NO. 2)
* ADDRESS OF GENERAL REGISTER STACK
* MULTIPLY BY 16
* STORE BASE ADDR OF GEN REG STACK
* SHIFT TO PROPER POS. FOR BR1
* LOAD ADDR OF CAR# COL 5-F
* READ CARO COL + 5-B
* ISOLATE CARD COL 7-8
* AI CONTAINS COL 7-8 (GEN REG NO.)
* JUMP TO 2ND LINE IN ROUTINE (4 DIGIT NO)000374000 D
* B HAS OCTAL VALUE OF GEN REG NUMBER
* SET MAR1 AS POST RECENTLY REFERENCED
* MOVE BASE ADDR TO AI FROM BR1
* SHIFT OHAR TO ISOLATE BR1
* CREATE GEN REG ADDRESSBASE + OFFSET)
* ADDRESS OF DATA
* READ IN DATA
* SET MAR1 AS MOST RECENTLY REFERENCED
* LOAD GEN REG ADDR INTO MAR2
* SHIFT TO ISOLATE BR1
* B HAS OCTAL VALUE OF DATA
* WRITE DATA FROM COL + 13-2C INTO
* SPECIFIED GENERAL REGISTER
* SET UP BREAKPOINT REGISTER AND SET
* STATUS BITS
* FILL B WITH CARD COL 1-4 (FROM SW1)
* ISOLATE THE R AND B CHARACTER
* ISOLATE COLUMN 2
* WRITE PSW INTO B
* INPUT FROM MEMORY
* CHECK FOR CHARACTER 'R'

```

```

* THIS ROUTINE SETS UP THE BREAKPOINT
* REGISTER AND SETS THE READ STATUS BITS
* SET BIT # 2C OF FSW REG
* WRITE PSW INTO MEMORY

```

```

* INPUT - 1 = CPCR
* COMP 0 = SAR
* B R = 0 * AI
* AI - 1 = B
* B L = B
* COMP 4 = SAR
* B L = BR1 * MAR
* COMP 8 = SAR
* LIT = MAR2
* CAR05X8 = LIT
* INPUT - 1 = CPCR
* B L = B
* COMP 16 = SAR
* P R = AI
* PACKED = CPCR
* DECOCT - 1 = CPCR
* ASR
* BHAR R = AI
* AI * B L = BR1
* COMP 8 = SAR * CAR01316 = LIT * SHIFT FOR BR1
* LIT = MAR2
* INPUT - 1 = CPCR
* ASR ADDR - 1 = CPCR
* BHAR R = MAR2
* B = SAR
* B = MIR
* OUT - 1 = HPCR

```

```

BREAKPOINT:
BEK
B L = AI
COMP 8 = SAR
AI R = AI
24 = SAR
LIT = MAR2
PSW = LIT
INPUT - 1 = CPCR
AI EOL LIT
AI = LIT
IF FALSE THEN AI EOL LIT * SKIP
BRKREAD - 1 = HPCR
54 = LIT
IF FALSE THEN SKIP
BRKWRITE - 1 = HPCR
BRK00TH - 1 = HPCR

```

```

* THIS ROUTINE SETS UP THE BREAKPOINT
* REGISTER AND SETS THE READ STATUS BITS
* SET BIT # 2C OF FSW REG
* WRITE PSW INTO MEMORY

```

```

* INPUT - 1 = CPCR
* COMP 20 = SAR
* AI OR B = MIR
* OUTPUT - 1 = CPCR

```

```

BRKREAD:
L L = AI
COMP 20 = SAR
AI OR B = MIR
OUTPUT - 1 = CPCR

```

```

* INPUT - 1 = CPCR
* COMP 20 = SAR
* AI OR B = MIR
* OUTPUT - 1 = CPCR

```

```

* INPUT - 1 = CPCR
* COMP 20 = SAR
* AI OR B = MIR
* OUTPUT - 1 = CPCR

```



```

0072 021C 0063 0030 0040
BRKWRITE:
00E3 4809 00C1 4C30 00F0
00E4 3000 00C0 0030 0010
00E5 4809 AC5C 0030 0060
00E6 0810 0003 0030 0060
00E7 022C 00C3 0030 0040
BRKNOOTH:
00E8 4809 20C1 8C30 00F0
00E9 030C 0003 0030 0040
00EA 4809 AC5C 0030 0060
00EB 081C 00C0 0030 0060
00EC 4809 20C3 001C 00F0
00ED 0360 00C0 0030 0060
00EE 0460 0000 0030 0060
00EF 0510 0000 0030 0060
00F0 4809 20C3 001C 00F0
00F1 021C 00C0 0030 0060
00F2 4809 0C40 0030 0060
00F3 4809 0C41 0020 00F0
00F4 0000 00C0 0030 0060
00F5 081C 0000 0030 0060
00F6 060C 00C0 0030 0040
00F7 4809 E000 880C 00F0
00F8 0700 00C3 0030 0040
00F9 4809 20C3 001C 00F0
00FA 052C 0003 0030 0060
00FB 0460 0040 203C 00F0
00FC 023C 00C0 0030 0060
00FD 060C 00C3 0030 0040
00FE 4809 20C3 001C 00F0
00FF 0460 0000 0030 0060
0100 052C 0003 0030 0060
0101 0460 0040 203C 00F0
0102 023C 00C0 0030 0060
0103 4809 0C40 0030 0060
0104 0000 00C0 0030 0060
0105 081C 0000 0030 0060
0106 060C 00C0 0030 0040
0107 4809 E000 880C 00F0
0108 0700 00C3 0030 0040
0109 4809 20C3 001C 00F0
010A 052C 0003 0030 0060
010B 0460 0040 203C 00F0
010C 023C 00C0 0030 0060
010D 060C 00C3 0030 0040
010E 4809 20C3 001C 00F0
010F 0460 0000 0030 0060
0110 0460 0000 0030 0060
0111 4809 0C40 0030 0060
0112 4809 0C41 1030 00F0
0113 3000 0000 0030 0060
0114 4809 E000 9030 00F0
0115 9000 0003 0030 0030
WRITEBRKPT - 1 = MPCR
THIS ROUTINE SETS UP THE BREAKPOINT REGISTER AND SETS THE WRITE STATUS BITS
XSET BIT 21 OF PSM REG
WRITE PSM INTO MEMORY
JUMP TO WRITE BREAKPOINT REGISTER
THIS ROUTINE SETS UP THE BREAKPOINT REGISTER AND SETS THE STATUS BITS FOR BOTH READ AND WRITE
PUT BREAKPOINT CODE INTO SRI BIT POS 21/20
21 AND 20
WRITE PSM INTO MEMORY
THIS ROUTINE WRITES THE DECIMAL ADDR INTO THE BREAKPOINT REGISTER AND AND INTO REGISTER BCI
RETRIEVE CAROLUX COMMENT
INPUT INTO B
OBTAIN ADDRESS FROM COL 4-8
GET ADDRESS OF BKPT REG
R HAS BINARY ADDRESS VALUE
MINSTOR BREAKPOINT ADDR INTO BR1
WRITE OUT ADDR INTO BKPT REG
RETURN TO NEW CAFD ROUTINE
HANDLES SECOND WORD OF TWO WORD INSTR
PUT COL 16 IN LSP
REREAD ADDR OF CARD COL 13-16
XORSTI HEX STEP IN GETADDR, B CONTAINS COL 16 DIGIT IN LSB OF B
LOAD GLOBAL VALUE OF DATA INTO SECOND WORD OF DOUBLEDWORD INSTRUCTION AND
THIS ROUTINE WILL PACK AN INSTRUCTION INTO CARD INTO A 16 BIT INSTRUCTION AND PLACE IT IN THE LS 16 BITS OF A
32 BIT WORDS - BITTYPE1 INSTRUCTIONS ARE SELECTED AND HANDLED BY A SEPARATE ROUTINE.
LIT = MAR2
CARD05X8 = LIT
INPUT - 1 = CPCCR
B R = A2
B L = A3
COMP 13 = SAR
A3 R = A3
29 = SAR
DRUDLEWORD:
A3 R = B
16 = SARJ CARD13X16 = LIT
LIT = MAR2
GETADDR = CPCCR
B = A2
LOADINSTR - 1 = CPCCR
NEWCARD - 1 = MPCR
INSTRUCTION:
LIT = MAR2
CARD05X8 = LIT
INPUT - 1 = CPCCR
B R = A2
B L = A3
COMP 13 = SAR
A3 R = A3
29 = SAR

```



0114 4009 C000 003C 00FC  
 0117 4809 E641 004C 00FC  
 0116 4000 C000 0070 C030  
 0118 2700 C000 0000 0080  
 0119 2700 C000 0000 0080  
 0116 4809 E0C0 0070 00FC  
 0117 4809 E640 2020 00FC  
 0118 4809 2002 001C 00FC  
 0119 0460 0000 0070 00FC  
 0116 4809 2555 0030 00FC  
 0117 4809 00C0 0000 00FC  
 0120 0FFF 00C0 0000 00FC  
 0121 4809 A152 0030 00FC  
 0122 03AC 0000 0070 00FC  
 0123 500B 0000 0000 00FC  
 0124 024C 0000 0070 0040  
 0125 4809 0C41 0030 00FC  
 0126 1000 0000 0000 0020  
 0127 4809 0C40 0030 00FC  
 0128 8000 00C0 0070 0030  
 0129 0C40 8000 00FC  
 012A 3070 0000 0000 0040  
 012B 4809 2558 0030 00FC  
 012C 4809 AC40 0040 00FC  
 012D 4009 C0C1 2000 00FC  
 012E 3000 0000 0000 0080  
 012F 4809 2000 2010 00FC  
 0130 4809 2000 2010 00FC  
 0131 0060 0000 0070 0060  
 0132 4809 C041 0030 00FC  
 0133 1000 00C0 0070 0030  
 0134 4809 A0C0 C030 00FC  
 0135 90C0 00C0 0070 0030  
 0136 4809 0C41 1070 00FC  
 0137 2000 00C0 0070 0030  
 0138 4809 0C40 8070 00FC  
 0139 7000 00C0 0070 0030  
 013A 4809 AC40 0030 00FC  
 013B 4809 C040 2000 00FC  
 013C 0250 0000 0000 0060  
 013D 4809 E001 1070 00FC  
 013E 9000 0000 0000 0030  
 013F 4809 E000 C030 00FC  
 0140 03AC 0000 0070 0080  
 0141 4809 A152 0070 00FC  
 0142 8000 0000 0000 00FC  
 0143 1060 C000 0030 0040  
 0144 0600 0000 0000 0040  
 0145 4809 0640 0070 00FC  
 0146 4809 20C0 001C 00FC  
 0147 0230 0000 C070 00E0  
 0148 4809 00C0 0071 00FC

A2 = AMPCR  
 A3 = AMPCR L = AMPCR  
 COMP 2 = SAR  
 COMP 3 = A3 + CSAR  
 COMP 4 = SARJ  
 COMP 5 = A3 + AMPCR  
 COMP 6 = SAR  
 COMP 7 = SAR  
 COMP 8 = A1  
 COMP 9 = A1 + B  
 COMP 10 = A1 + B + A1  
 COMP 11 = A1 + B + A1 + B + A1  
 COMP 12 = A1 + B + A1 + B + A1 + B + A1  
 COMP 13 = A1 + B + A1 + B + A1 + B + A1 + B + A1  
 COMP 14 = A1 + B + A1 + B + A1 + B + A1 + B + A1 + B + A1  
 COMP 15 = SAR  
 B L = B  
 B R = A1  
 B R = A1  
 P R = B  
 23 = SARJ 7 = LIT  
 A1 + B = AMPCR  
 A1 + B + A1 = B  
 A2 L = A2  
 COMP 4 = SARJ  
 COMP 5 = A3 + AMPCR  
 L1 = A3 + AMPCR L = A2  
 L2 = A3 + AMPCR L = A2  
 INPUT MAR2 = CPFR  
 R L = A1 + B  
 COMP 7 = SAR  
 A1 R = A1  
 A1 R = A1  
 29 = SAR  
 B L = A3 + B  
 COMP 6 = SAR  
 B R = B  
 29 = SAR  
 A1 + B = B  
 A2 + B = A2  
 LOADINSTR - 1 = CPFR  
 A3 L = A3  
 COMP 3 = SAR  
 A3 R = A1  
 24 = SARJ 5B = LIT  
 A1 EOL LIT  
 IF TRUE THEN STEP ELSE SKIP  
 DOUBLEWORD - 1 = MPCR  
 NEWCARD - 1 = MPCR  
 LOADINSTR:  
 AMPCR = A1  
 MAR2 = MAR2  
 NEXTINSTR = LIT  
 LCTR









```

0174 4809 ECE5 003C 00FC
0175 4809 00F1 2C00 0050
0176 4809 004B 0030 0050
0177 4809 004B 0030 0050
0178 1440 0729 0000 C650
0179 05E0 0000 0000 C040

017A 4809 2003 001C 00F0
017B A200 0000 0000 00A0
017C 046C 0003 0000 0060
017D 4809 00C4 8030 40F0
017E 4809 2CE5 8800 00FC
017F 0010 0000 0000 C0E0
0180 4809 0C40 00A0 C0F0
0181 05E0 0000 0030 0040

0182 2809 0000 0000 00E0
0183 5809 0000 0000 00E0
0184 0510 0000 0000 0060
0185 9A09 20C3 001C 00E0
0186 0230 0000 0030 00E0
0187 0000 00C2 0030 00F0
0188 6A9E 0000 0070 C0F0
0189 0460 0000 0000 0060
018A 4809 00C4 4C30 C0F0
018B 4809 20C3 001C C0F0
018C 07C0 0000 0070 00E0
018D 046C 0000 0030 0060
018E 0030 0003 0030 00E0
018F 4812 00C3 0071 00F0
0190 4809 00C4 8032 00F0
0191 0000 0000 0000 0010
0192 4809 2C56 2730 00F0
0193 03F0 0003 0030 00E0
0194 4809 C152 0030 00F0
0195 00F0 0000 0000 0060
0196 60C9 67C3 0030 00F0
0197 0210 0000 0030 00E0
0198 0000 0000 001C 00E0
0199 5029 00C3 001C 00E0
019A 80C9 004E 1000 C0F0
019B 4809 00C3 001C 00E0
019C 001C 0000 0030 0060
019D 4809 ACC0 4C30 C0F0
019E 2808 0000 0000 0040
019F 027F 0000 0000 0040
01A0 4809 00C3 001C 00F0
01A1 4809 E159 0F30 00F0
01A2 0800 0003 000C 00E0
01A3 7008 0000 0000 00E0

```

```

A3 OR B = B
A2 L = A2
DMP B = SAR
LOADINSTR 1 = CPGR
OUT - 1 = MPGR

SETPAGING:
LIT = MAR2
PSW = LIT# 22 = SAR
INPUT - 1 = CPGR
B C = B, CSAR
LIT OR B C = B
L1 = LIT
D = MIR
OUT - 1 = MPGR

CHARSTRING:
IF LCI
IF LCI
GETADR - 1 = CPGR
LIT#MAR2 = LIT
NEXTINSTR = LIT
B EOL 0
IF TRUE THEN SET LC2:
B = A1
LIT = MAR2
CARD0#X12 = LIT
MORECHAR: INPUT - 1 = CPGR
J = LIT
LCR# SAVE
B C = B, MIR, INC
B = SAR
LIT AND B = A2
G3 = LIT
A2 EOL LIT
J5 = LIT
IF TRUE THEN SET LCI
J3 = LIT
IF LCI THEN LIT + B = B#MIR, SET LCI
IF NOT COV THEN JUMP
B#MIR = A3
LIT#MAR2 = A3
OUTPUT1 - 1 = CPGR
A1 + 1 = A1
IF LCI THEN STEP ELSE SKIP
ENDCHARSTRING - 1 = MPGR
A3 = MAR2
A3 LE0 LIT
CARD07#BC = LIT
IF TRUE THEN SIFF ELSE SKIP

```

```

X B = C000/C0+C0L* 10#11#12
X PREPARE A2 FOR ADDITION OF B
X PACK REMAINING BITS INTO A2
X INSTRUCTION WORD RITYPE 1 COMPLETED
X
X THIS ROUTINE WILL SET THE PAGING BIT
  (BIT POS. 22) OF THE PSW
X
X READ IN CONTENTS OF PSW
X MOVE PAGING BIT TO LS BIT
X PAGING BIT SET/PAGING SELECTED)
X
X CONTENTS OF PSW INTO MIR
X
X THIS ROUTINE WILL READ THE CHARACTER
  STRING STARTING IN COL. 9 UNTIL FINDING
  A QUOTE (*). THE STRING WILL THEN BE
  STORED AT THE ADDRESS IN COL. 4-8. IF
  COL. 4-8 IS BLANK, THE STORAGE ADDRESS
  WILL DEFAULT TO THE ADDRESS IN NEXTINSTR
X CLEAR CONDITION BITS
X GET ADDRESS IN COL. 4-8
X MAR2 CONTAINS ADDR OF NEXT INSTRUCTION
X CHECK FOR BLANK ADDRESS FIELD
  STEP ELSE SKIP
X READ COMMENTS OF NEXTINSTR
X A1 CONTAINS ADDR TO BE WRITTEN INTO
  SET UP READ ADDR OF COL. 9-12 IN MAR2
X READ A 4 CHARACTER BLOCK
X SET UP COUNTER FOR 4 ITERATIONS
X SHIFT 1 CHARACTER INTO B TO EE ANALYZED
X EXTRACT RIGHTMOST CHARACTER
X SET UP 6 BIT MASK
X TEST FOR * (OF)
X IF A (*) IS IN THE STRING SET LCI
X ADD VALUE TO (*) SO THAT SPACE APPEARS
X CHECK IF LOOP DONE 4 TIMES
X CHECK REMAINING ADDRESS
X WRITE WORDS BACK TO MEMORY
X INCREMENT WRITE ADDRESS
X CHECK IF (*) WAS FOUND
X A3 ADDR MAR2 HAVE READ ADDRESS
X CHECK IF YOU ARE AT THE END OF THE
  CARD0#65#LCC 0

```







```

AEOH:
C1CC 3809 0000 0000 00F0
C1CD 4809 0000 8000 00F0
C1CE 50FC 00C3 0030 00B0
C1CF 4809 2C56 0030 00FC
C1D0 4809 E1*6 2C00 00F0
C1D1 4809 CC52 0C30 00F0
C1D2 5A49 0000 0C30 00F0
C1D3 482D 00C0 0C30 00F0

C1D4 4809 A0E1 2030 00F0
C1D5 8000 00C0 0C00 002C
C1D6 4809 C0E0 A0C0 00F0
C1D7 4809 C0E0 0C3C 00F0
C1D8 7858 C0E0 4030 00F0
C1D9 429C C000 0C3C 0040
C1DA 4809 A0E0 C03C 00F0
C1DB 8000 0000 0C7C 0020
C1DC 4809 A0E1 4000 00F0
C1DD 4809 00C1 003C 00F0
C1DE 40C0 00C3 0C7C 0020
C1DF 4809 AC5C 4030 00F0
C1E0 4809 AC5C 4030 00F0
C1E1 02AC 00C0 0000 0040

C1E2 4809 0C43 0070 00F0
C1E3 5A59 00C3 0070 00F0
C1E4 3809 00C3 0C30 00FC
C1E5 4809 0C40 803C 00F0
C1E6 4000 00C0 0C3C 00C0
C1E7 482D 00C0 0C7C 00F0

C1E8 2808 0000 0C7C 00FC
C1E9 0200 C008 0C00 C040
C1EA 02C0 8008 0C3C 004C

C1EB 4809 A001 C070 00FC
C1EC 8000 0000 C07C C030
C1ED 4809 A0CE 4800 40F0
C1EE 4809 ACCL C07C 00F0
C1EF 482D 00C0 0030 00F0

C1F0 4809 A0C1 C030 00F0

```

```

IF LC2
A3 R = B
# = SARJ 15 = LIT
LIT AND B = B
A3 AND LIT = A2
A2 EOL B
IF TRUE THEN SET LC2
JUMP

A1 L = A2
C0HP 16 SAR
A2 R = A2
A2 GTR 0 = A2
IF FALSE THEN A1 + 1 = MPCR
OPCODE - 1 = MPCR
A1 R = A1
15 = SAR
A1 L = A1
C0HP 10 = SAR
A1 OR B = A1
OPCODE - 1 = MPCR

BYTETEST:
B
IF LST THEN SET LC2J SKIP % IF LSB OF B EQUALS 1 THEN SET LC2
IF LC2
B R = B
I = SAR
JUMP

***** CARRY BIT SETTING *****
CARRY: IF LC1 THEN STEP ELSE SKIP % THIS ROUTINE WILL SET THE CARRY
SETCARRY - 1 = MPCR % BIT IF LC1 IS SET UPON ENTRANCE
CLEARC - 1 = MPCR % OTHERWISE, CLEAR THE CARRY BIT

CLEARC:
A1 C = A1
28 = SAR
A1 AND B110 = A1,CSAR
A1 C = A1
JUMP

SETCARRY: A1 C = A1

```

```

% THIS ROUTINE TESTS IF THE A1 FIELD
% EQUALS THE P1 FIELD. IF EQUAL LC2
% A2 = RMJ B = RA RETURNED

% B CONTAINS *A* FIELD
% A2 CONTAINS *M* FIELD

% THIS ROUTINE WILL INCREMENT THE PAR
% YES FOR WRAPAROUND AND ALL OPCODE
% INCREMENT THE COPY OF THE PAR
% CHECK FOR WRAPAROUND
% A1 ELSE SKIP % INCREMENT PAR 3X 1
% CALL OPCODE FOR NEXT INSTRUCTION
% CLEAR OLD PAR

% 1024 INTO B
% SET PAR TO 1024
% FETCH NEXT INSTRUCTION

% THIS INSTRUCTION TEST THE LSB OF B
% WHICH CONTAINS EITHER (RMJ) OR (RXX)
% OR (RM*1) AND DIVIDES E BY TWO
% B CONTAINS RESULT
% LC2 = 1 IMPLIES LS BYTE OF Y
% LC2 = 0 IMPLIES HS BYTE

% THIS ROUTINE CLEARS THE CARRY BIT
% (POSITION 20) IN PSW

% THIS ROUTINE SETS THE CARRY BIT IN

```









```

0217 4809 46C1 8890 00F0
0218 0000 0000 0000 004C
0219 2809 0000 0000 00F0
021A 8809 AC5C 4030 00F0
021B 4820 0000 0030 00F0

021C 4809 1809 8870 00FC
021D 0000 0000 0070 0010
021E 4809 AC55 4030 00FC
021F 4820 0003 0070 00F0

0220 4809 1800 8890 00F0
0221 0000 0000 0000 0010
0222 4809 AC5C 4030 00FC
0223 4809 1819 8890 00FC
0224 3000 00E9 0030 0000
0225 4809 AC23 4030 00FC
0226 4820 0003 0070 00F0

0227 4809 40C1 C020 40F0
0228 3030 0003 0070 0040
0229 4809 A156 0870 00FC
022A 4809 4001 C070 00FC
022B 4820 0003 0000 00F0

022C 4809 0640 2000 00F0
022D 4809 0040 8890 00F0
022E 30F0 0000 0030 0080
022F 4809 2056 0890 00FC
0230 0370 0000 0030 0060
0231 4809 0000 0070 24FC
0232 4809 0040 8890 00F0
0233 4809 0000 0000 0000
0234 0000 0000 0000 0020
0235 4809 E05C 4000 00FC
0236 0380 0003 0070 0060
0237 4809 0000 0030 00F0
0238 4820 0000 0070 00F0

0239 4809 0640 2070 00FC
023A 4809 E156 0890 00F0
023B 00FC 0000 0070 00E0

SETI11 0101 C = B
      B = SAR
      IF LC1
      R OR A1 = A1
      JUMP

SFI00: 0010 C = B
      B = SAR
      B AND A1 = A1
      JUMP

SET01: 0100 R = B
      B = SAR
      B OR A1 = A1
      R SAR
      B AND A1 = A1
      JUMP

CHECKKCI:
      A1 C = A1, CSAR
      23 = SAR, J = LIT
      A1 AND LIT = B
      A1 C = A1
      JUMP

* * * * * END CONDITION CODE ROUTINES * * * * *
CONTENTSRA:
      AMPCR = A2
      B R = B
      4 = SAR, 15 = LIT
      LIT AND B = B
      REGSTACK - 1 = CFCR
      ASE = B
      B AND B = B
      COMP - 16 = SAR
      B OR A3 = A3
      EIMPUT - 1 = CPCR
      A2 = AMPCR
      JUMP

CONTENTSRRH:
      AMPCR = A2
      A3 AND LIT = B
      15 = LIT

```



```

023C 019F 000F 000F 0060 00996000 D
023D 0140 007C 007C 007C 00992000 C
023E 0140 007C 007C 007C 00992000 C
023F 180F 007C 007C 00F0 00991000 D
0240 4820 0000 0000 00F0 00902100 C
    009C2100 C
    009C3100 C
    009C4000 C
    00905000 C
    00906000 C
    00907000 C
    00908000 C
    00909000 C
    00910000 D
    00911000 D
    00912000 D
    00913000 D
    00914000 D
    00915000 D
    00916000 D
    00917000 D
    00918000 D
    00919000 D
    00920000 D
    00921000 D
    00922000 D
    00923000 C
    00924000 C
    00925000 C
    00926000 C
    00927000 D
    00928000 D
    00929000 D
    00930000 C
    00931000 D
    00932000 C
    00933000 C
    00934000 C
    00935000 C
    00936000 C
    00937000 D
    00938000 C
    00939000 D
    00940000 D
    00941000 D
    00942000 D
    00943000 D
    00944000 D
    00945000 D
    00946000 D
    00947000 D
    00948000 D
    00949000 D
    00950000 D
    00951000 D
    00952000 D
    00953000 D
    00954000 D
    00955000 D
    00956000 D
    00957000 D
    00958000 D
    00959000 D
    00960000 D
0241 4809 0C4C 0030 00F0 00996000 D
0242 4A49 0C50 0030 00FC 00992000 C
0243 4C09 0C5E 0030 00F0 00992000 C
0244 4809 0C43 8070 00F0 00991000 D
0245 4809 0C00 008F 0020 00902100 C
0246 4809 0C00 0030 00F0 009C2100 C
0247 4C0E 00C0 2080 00F0 009C3100 C
0248 4809 0C00 2030 00F0 009C4000 C
0249 2409 0C00 4000 00F0 00905000 C
024A 2809 00C0 1000 00F0 00906000 C
024B 4809 0C32 0070 00F0 00907000 C
024C 4809 0C00 007C 00F0 00908000 C
024D 4809 0C00 007C 20F0 00909000 C
024E 4809 0000 0031 20F0 00910000 D
024F 01E0 0000 0000 00E0 00911000 D
0250 4809 0000 1010 00FC 00912000 D
0251 4809 0C43 001C 00FC 00913000 D
0252 4809 00C0 0020 00F0 00914000 D
0253 4809 0F5E 0030 00FC 00915000 D
0254 740E 0000 1020 00F0 00916000 D
0255 03C0 0000 1020 0040 00917000 D
0256 4809 0C01 2080 00F0 00918000 D
0257 300C 00C0 003C 0030 00919000 D
0258 4809 0C00 0C70 00F0 00920000 D
0259 4C09 0E0C 1C3C 00FC 00921000 D
025A 4809 0C61 2C52 00FC 00922000 D
025B 300C 0000 0030 0030 00923000 C
025C 4809 0F5E 0030 00FC 00924000 C
025D 780E 0000 0000 00F0 00925000 C
025E 0300 00C0 0080 004C 00926000 C
025F 4809 0C41 0030 00FC 00927000 D
0260 300C 00C0 0030 0030 00928000 D
0261 03E0 00E0 0000 004C 00929000 D
0262 4809 0F5E 0030 00FC 00930000 C
0263 4809 0C41 003C 00FC 00931000 D
0264 4809 0C41 003C 00FC 00932000 C
0265 3010 00C0 0000 008C 00933000 C
0266 4809 2C5C 0090 00FC 00934000 C
0267 4809 E001 1030 00F0 00935000 C
0268 300B 0000 0C7C 003C 00936000 D
0269 300B 0000 0050 00F0 00937000 D
026A 2570 0000 003C 004C 00938000 D
026B 4809 E000 AC00 00F0 00939000 D
026C 1000 0000 1020 000C 00940000 D
026D 4809 0C40 1000 00F0 00941000 D
026E 4809 E000 8E0C 00F0 00942000 D
026F 00C0 0000 0030 0020 00943000 D
0270 4809 E001 1C00 00F0 00944000 D
0271 4809 E000 903C 00F0 00945000 D

```

DIV1:

DIV2:

ONE1:

ONE2:

DIV3:

DIV4:

DIV5:

DIV6:

DIV7:

DIV8:

DIV9:

DIV10:

DIV11:

DIV12:

DIV13:

DIV14:

DIV15:

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DIV97:

DIV98:

DIV99:

DIV100:







```

0245 8809 C138 0030 00FC 01649000 D
0246 809C 0000 0030 00E6 01649000 D
0247 720B C140 2C9A 00F0 01027CCC D
0248 0076 0000 0000 00E0 01027160 D
0249 8809 C041 803F 00F0 01027A00 D
0250 0000 0000 0030 0010 01027400 D
0251 8809 C040 0030 00F0 01025400 D
0252 0040 0000 0000 0080 01025600 D
0253 8809 A000 001C 00F0 01027600 D
0254 8809 7C52 0C30 00F0 01028600 D
0255 68CB 0C03 0C7C 00F0 01029600 D
0256 0460 00C0 0030 0060 0103CC00 D
0257 2F59 A0C0 4C30 00F0 01031600 D
0258 2F59 0000 0030 00F0 01032700 D
0259 2A08 0000 003C 00F0 01033700 D
0260 241C 0000 0000 004C 01034600 D
0261 800C 0000 003C 00F0 01035400 D
0262 241C C0F0 0030 0040 01036400 D
0263 8809 A003 001C 00F0 D 01037600 D
0264 8870 00C3 003C 0060 D 01038600 D
0265 8809 0000 0030 20FC D 01039600 D
0266 8809 0F40 9000 00F0 D 01040600 D
0267 0000 0000 0030 C010 D 01041600 D
0268 0000 0000 003C C010 D 01042600 D
0269 8809 E0C3 1030 00F0 D 01043600 D
0270 8809 E132 0030 00F0 D 0104400C D
0271 00C0 00C0 0000 00E0 D 0104500C D
0272 68CB E132 0C30 00F0 D 01046000 D
0273 011C 00C3 003C 00E0 D 01047600 D
0274 0480 0000 003C 0060 D 01048600 D
0275 011C 00C3 003C 00E0 D 0104900C D
0276 8809 E132 0C30 00F0 D 01050000 D
0277 011C 00C3 003C 00E0 D 01051000 D
0278 0490 0000 0030 0060 D 01052000 D
0279 0180 00C3 003C 0060 D 01053000 D
0280 0440 00C3 003C 0060 D 01054000 D
0281 020C 0000 0030 00F0 D 01055000 D
0282 68CB E132 0C30 00F0 D 01056000 D
0283 020C 0000 0030 0060 D 01057000 D
0284 0400 0000 0030 C060 D 01058000 D
0285 020C 0000 0030 00E0 D 01059000 D
0286 020C 0000 0030 00E0 D 01060000 D
0287 0400 0000 0030 C060 D 01061000 D
0288 020C 0000 0030 00E0 D 01062000 D
0289 0400 0000 0030 C060 D 01063000 D
0290 020C 0000 0030 00E0 D 01064000 D
0291 297C C000 0030 C04C D 01065000 D
0292 8809 A180 003C 00F0 D 01066000 D
0293 0020 0000 007C 00E0 D 01067000 D
0294 8809 E138 0030 00F0 D 01068000 D
0295 02FA 0000 00C0 00E0 D 01069000 D
0296 760B 00C3 0060 00F0 D 01070000 D
0297 298C 0000 0C30 0040 D 01071000 C
0298 040C 0000 0C30 0060 D 01072000 C
0299 1F4C 0000 0C30 0060 D 01073000 D
0300 04FC 00C3 0C00 0060 D 01074000 D
0301 050C 00C3 0C3C 0060 D 01075000 D
0302 0510 0000 0C30 0060 D 01076000 D
0303 8809 20C3 001C 00F0 D 01077000 D
0304 0260 0000 0030 C0E0 D

```





02E0	032C	00C0	0000	0060	0	INPUT - 1 = CPGR	X READ IN CONTENTS OF A1	01078000	0
02E1	4809	0040	0000	0060	0	BHAR * 1 = MAR2	X ADDRESS IN A1	01099000	0
02E2	0530	0000	0030	0040	0	INPUT - 1 = MAR2	X ADDRESS OF A2	01099000	0
02E3	0530	0000	0030	0040	0	INPUT - 1 = CPGR	X READ IN A2	01099000	0
02E4	4809	0040	0030	0060	0	B = A2	X RESTORE A2	01099000	0
02E5	4809	0040	0030	0060	0	BHAR * 1 = MAR2	X CONSTRUCT ADDRESS OF A3	01099000	0
02E6	0540	00C0	0030	0040	0	INPUT - 1 = CPGR	X READ IN A3	01099000	0
02E7	4809	0040	0030	0060	0	B = A3	X RESTORE A3	01099000	0
02E8	4809	0040	0030	0060	0	BHAR * 1 = MAR2	X CREATE ADDR OF MIRC(WORKSPACE + 4)	01099000	0
02E9	0550	00C0	0030	0060	0	INPUT - 1 = CPGR	X READ IN MIRC	01099000	0
02EA	4809	0040	0030	0060	0	B = MIRC	X RESTORE MIRC	01099000	0
02EB	4809	0040	0030	0060	0	BHAR * 1 = MAR2	X RESTORE ADDR OF RPI	01099000	0
02EC	0560	00C0	0000	0060	0	INPUT - 1 = CPGR	X CREATE ADDR OF RPI	01099000	0
02ED	4809	0040	0030	0060	0	R L = BR1	X RESTORE RPI	01099000	0
02EE	0260	00C0	0000	0080	0	COMP B = SAR J WORKSPACE = LIT	X THIS ROUTINE READS THE CONTENT OF THE	01099000	0
02EF	4809	0000	0030	0060	0	LIT = MAR2	X MEMORY ADDRESS IN MAR2	01100000	0
02F0	0570	00C0	0030	0060	0	INPUT - 1 = CPGR	X PERFORM READ	01100000	0
02F1	4809	0040	0030	0060	0	B = AMPCR	X READ CONTENTS OF MAR2 INTO B	01100000	0
02F2	4809	0000	0000	0060	0	STEP	X	01100000	0
02F3	4820	00C0	0000	0060	0	JUMP	X	01100000	0
02F4	4809	0000	0030	0060	0	INPUT:	MR2 J IF ROC	01100000	0
02F5	4C28	00C0	0000	0060	0		WHEN ROC THEN BEX JUMP	01100000	0
02F6	9809	0000	00C0	1C00	0	OUTPUT:	X THIS ROUTINE WRITES MIRC INTO THE	01100000	0
02F7	9C28	0000	0000	0060	0		MEMORY ADDRESS OF MAR2	01100000	0
02F8	1C88	0010	0010	0060	0	EXTIO:	X THIS ROUTINE WRITES MIRC INTO THE	01100000	0
02F9	9809	0000	00C0	1C00	0		MEMORY ADDRESS OF MAR2	01100000	0
02FA	9C08	0040	0030	0060	0		X WHEN WRITE COMPLETED JUMP	01100000	0
02FB	4809	0010	0010	0060	0		X	01110000	0
02FC	980E	00C0	0000	0060	0		X THIS ROUTINE DOES EXTERNAL I/O	01110000	0
02FD	0008	00C0	00C0	0060	0		X INTERFACE BETWEEN THE UYK20 EMULATION	01112000	0
02FE	3E08	00C0	00C0	0060	0		X AND THE IOP. B CONTAINS THE CONTENTS	01113000	0
02FF	4E08	0040	0030	0060	0		X OF MAILBOX - 1 IF REQUIRED.	01114000	0
0300	582F	00C0	0000	0060	0		X WHEN ROC THEN B111=MR2	01115000	0
0301	0580	00C0	0000	0060	0		SET GC2 J WHEN GC2 THEN B111=MR2	01116000	0
0302	4809	0040	0030	0060	0		MR2 J B111=MR2 J IF SAI	01117000	0
0303	00E0	0000	00C0	0060	0		WHEN SAI THEN B = MIRC	01118000	0
0304	00C0	0000	00C0	0030	0		B111 = MAR2 J RW2	01119000	0
0305	0590	00C0	0000	0040	0		WHEN SAI THEN SET INT	01120000	0
0306	00C0	0000	00C0	0030	0		WHEN NOT INT THEN STEP	01121000	0
0307	00C0	0000	00C0	0030	0		WHEN INT THEN BEX J MR2	01122000	0
0308	00C0	0000	00C0	0030	0		WHEN ROC THEN NOT B J RESET GC2	01123000	0
0309	00C0	0000	00C0	0030	0		IF ABT THEN JUMP ELSE RETN	01124000	0
0310	0580	00C0	0000	0060	0		X	01125000	0
0311	4809	0040	0030	0060	0		X THIS ROUTINE PRINTS OUT THE ERROR	01126000	0
0312	00C0	0000	00C0	0030	0		X MESSAGE FROM INTERRUPT	01127000	0
0313	00C0	0000	00C0	0030	0		X INSCRIBED BY LOADER JCL AND STOPS THE	01128000	0
0314	00C0	0000	00C0	0030	0		X MACHINE	01129000	0
0315	0590	00C0	0000	0040	0		X	01130000	0
0316	0580	00C0	0000	0060	0		X CREATE ERRORLIST ADDRESS IN BR1	01131000	0
0317	4809	0040	0030	0060	0		X	01132000	0
0318	00C0	0000	00C0	0030	0		X	01133000	0
0319	00C0	0000	00C0	0030	0		X	01134000	0
0320	00C0	0000	00C0	0030	0		X	01135000	0
0321	00C0	0000	00C0	0030	0		X	01136000	0
0322	00C0	0000	00C0	0030	0		X	01137000	0



COMPRESS:

```

0306 4809 0640 0C4C 00F0
0307 4809 20C3 001C 00F0
0308 02C0 00C3 001C 00F0
0309 2F5C 0000 0C4C 006C
030A 4809 0000 0000 20F0
030B 4809 0F43 001C 00F0
030C 4809 0000 9000 00F0
030D 0000 00C3 0000 002C
030E 4809 00C1 1000 00F0
030F 054C 00C0 0000 0060
0310 4809 0C41 2050 00F0
0311 000C 0000 9030 00F0
0312 4809 0F47 0030 0020
0313 0000 0000 0030 003C
0314 050C 0000 0030 003C
0315 4809 0C5E 0030 00F0
0316 4809 0F46 0B3C 00F0
0317 4809 0000 0000 20FC
0318 4809 0F43 801C 00FC
0319 000C 00C0 0050 001C
031A 4809 0C41 0020 00F0
031B 4809 0000 007C 74F0
031C 4809 0F41 001C 00F0
031D 05CC 0C73 0C70 0060
031E 4809 20C3 001C 00F0
0320 032C 0003 0C4C 00F0
0321 4809 0F46 0C1C 00F0
0322 2F30 0070 0C70 0060
0323 4809 00C0 000C 20F0
0324 4809 0F43 0C10 00F0
0325 4809 0C51 0050 00FC
0326 0000 00C0 0030 0030
0327 4809 0000 0C70 00F0
0328 4809 0000 0050 00F0
0329 021C 0000 0050 00F0
032A 4809 0C5C 4030 00F0
032B 3E59 0C52 003C 00FC
032C 4809 0C42 003C 00FC
032D 5819 0000 0000 0090
032E 0000 0000 0000 0090
032F 4809 20C3 001C 00FC
0330 02C0 0003 0070 00FC
0331 2F3C 0043 0C4C 0060
0332 4809 0C40 004C 00F0
0333 4809 0000 003C 00FC
0334 4820 00C0 0030 00FC

```

```

* * * * * INPUT OUTPUT CONTROL * * * * *
* THIS ROUTINE COMPRESSES /AVUTK00
* 16 BIT BUFFERS (LHW OF 32) INTO SUPERBLOCKS
* (5-HEMRY WORD) INTO 32 BIT WORD
* FORMAT COMPATIBLE WITH THE IOP
* UPON ENTRY, BR1 CONTAINS BUFFER ADDRESS 01194000
* NO. OF BUFFERS IN UHW OF A3
* THIS ROUTINE ACCEPTS A VARIABLE
* BUFFER LENGTH FOR CRT OUTPUT, J3 WORUS
* FOR FRT OUTPUT
* STORE AMPCR INTO STACK
* (STACK) = AMPCR
* REFERENCE BR1
* STORE BUFFER ADDRESS IN ER2
* CLEAR LHW OF A3 FOR COUNT
* GET CONTENTS OF BUFFER ADDRESS WORD
* STORE CONTENTS IN UHW OF A2
* GET ADJACENT WORD ADDR.
* B = CONTENTS OF ADJACENT WORD
* COMPLEMENT TO NEXT BIT WORD
* STORE NEXT WORD PAIR ADDR. IN B
* REFERENCE BR1
* COMPRESSED WORD DESTINATION
* STORE WORD PAIR ADDR. IN B
* REFERENCE BR2
* COMPRESSED WORD DESTINATION IN BR2
* SAVE DESTINATION ADDR. IN B
* B = BUFFER LENGTH IN 10CW + 2
* 10CW + 2 = HAR2
* B = BUFFER LENGTH
* REFERENCE BR1
* TRANSFER NEXT WORD PAIR ADDR TO ER2
* NEXT DESTINATION ADDR. IN BR1
* INCREMENT COUNTER ( < ? 16 - 1)
* ISOLATE COUNTER IN A2
* RESTORE AMPCR FROM STACK
* SEPARATE AMPCR ASSIGNMENTS AND JUMP
* * * * *

```

```

AMPCR = MIR
LIT = HAR2
STACK = LIT
EINPUT - 1 = CPCR
ASR
BHAR = BR2
A3 R = A3
15 = SAR
A3 L = A3
COMPR1: E*ULIN - 1 = CPCR
E L = A2
COMP 16 = SAR
BHAR + 1 L = BR2
COMPR 0 = SAR
A2 BR 0 = MTR CPCR
BHAR + 1 = B
ASR
BHAR R = HAR2+CSAR
B L = BR1
ASE
PHAR L = BR2
E*HULOUT - 1 = CPCR
BHAR = A2
LIT + 1 = HAR2
10CW = LIT
BHAR + 1 = HAR2
EINPUT - 1 = CPCR
ASR
BHAR = BR2
A2 + 1 L = BR1
COMP 0 = SAR
A3 + 1 = A3
A3 L = A2
COMPR 16 = SAR, J3 = LIT
IF LC2 THEN A2 EOL B; SET LC2; SKIP
A2 EOL LIT
COMPRPT - 1 = MPCR
LIT = HAR2
STACK = LIT
EINPUT - 1 = CPCR
R = AMPCR
STEP
JUMP

```



```

0335 3809 00C0 0070 20F0
0336 4809 CF40 A030 00F0
0337 0000 00C0 007C 0010
0338 48C9 E8C1 6070 C0F0
0339 0000 00C0 0030 0020
0340 0000 0040 8830 C0F0
0341 4809 C640 7000 00F0
0342 4809 C0D2 2000 00F0
0343 4809 0641 002C 00F0
0344 0000 00C0 003C 0030
0345 4809 C001 0010 00F0
0346 050C 00C3 0000 0060
0347 0000 00C0 007C 00F0
0348 4809 C8C1 8030 20F0
0349 4809 E801 2070 00F0
0350 4809 CFF0 A030 00F0
0351 4809 CF40 0010 00F0
0352 0000 00C0 0030 0030
0353 4809 00C0 00C0 C060
0354 050C 00C3 0000 0060
0355 4809 0F40 2070 00F0
0356 0000 00C0 007C 00F0
0357 050C 00C3 0000 0060
0358 4809 E8C1 6070 C0F0
0359 0000 00C0 0030 0020
0360 4809 E8C1 6070 C0F0
0361 4809 C0C3 4830 C0F0
0362 4809 C012 0070 00F0
0363 5019 0000 0020 00F0
0364 0610 C0C3 0020 C040
0365 48C5 0F40 2000 00F0
0366 4809 C559 0010 00F0
0367 0000 00C0 00C0 0030
0368 33F0 00C3 0000 C040
0369 48C9 C0C0 0030 20F0
0370 48C9 0F40 8040 C0F0
0371 0000 00C0 007C 00F0
0372 4820 C003 0030 00F0
0373 4820 C003 0030 00F0
0374 4820 C003 0030 00F0
0375 4820 C003 0030 00F0
0376 4820 C003 0030 00F0
0377 4820 C003 0030 00F0
0378 4820 C003 0030 00F0
0379 4820 C003 0030 00F0
0380 4820 C003 0030 00F0
0381 4820 C003 0030 00F0
0382 4820 C003 0030 00F0
0383 4820 C003 0030 00F0
0384 4820 C003 0030 00F0
0385 4820 C003 0030 00F0
0386 4820 C003 0030 00F0
0387 4820 C003 0030 00F0
0388 4820 C003 0030 00F0
0389 4820 C003 0030 00F0
0390 4820 C003 0030 00F0
0391 4820 C003 0030 00F0
0392 4820 C003 0030 00F0
0393 4820 C003 0030 00F0
0394 4820 C003 0030 00F0
0395 4820 C003 0030 00F0
0396 4820 C003 0030 00F0
0397 4820 C003 0030 00F0
0398 4820 C003 0030 00F0
0399 4820 C003 0030 00F0
0400 4820 C003 0030 00F0

```

EXPAND:1

```

* THIS ROUTINE WILL TAKE A WORD IN
* CONTAINING 32 BIT WORDS AND EXPAND EACH INTO 2
* INTO 2 - 32 BIT WORDS, PUTTING THE INFO INTO
* IN THE LOW OF EACH 32 BIT WORD.
* BR1 MUST CONTAIN THE BUFFER ADDRESS
* AND A3 MUST CONTAIN # OF BUFFERS/COUNT
* REFERENCE BR1
* ISOLATE THE COUNT(BUFFER EXPAND FACTOR)
* CALCULATE FIRST OUTPUT ADDRESS
* RETURN IN BR1
* BUFFER ADDR + BUF - 1 IN BR2
* COUNTS IN 1 WORD INTO C
* WORD CONTENTS INTO UNM OF A2
* ISOLATE BUFFER COUNT
* BUFFER ADDR + COUNT INTO BR2
* OUTPUT 1 EXPANDED HALFWORD
* REFERENCE #A2
* ISOLATE THE COUNT
* COUNT INTO B
* NEXT READ ADDRESS INTO BR2
* NEXT WORD INTO B
* REDUCE THE COUNT BY 1
* NEXT WRITE ADDRESS
* WRITE OUT NEXT EXPANDED WORD
* REDUCE THE COUNT
* CHECK IF ALL WORDS EXPANDED
* NEXT READ ADDRESS
* REFERENCE BR1
* RESTORE RETURN ADDRESS
* THIS ROUTINE DUMPS THE BUFFERS

```



```

0368 3809 0000 0070 24F0
0369 4809 00C0 0070 00F0
036A 4809 0F46 0010 00F0
036B 2F30 00C0 00C0 0060
036C 4809 0C41 0020 00F0
036D 4000 00C0 0030 0030
036E 4809 00C0 0030 00F0
036F 4000 0000 0020 0010
0370 4809 0C40 0070 00F0
0371 062C 0000 0030 0060
0372 4809 00C0 0030 00F0
0373 4874 0000 0030 00F0
0374 063C 0000 0030 0040
0375 0640 00C0 0030 0040
0376 0650 0000 0030 0040

SP00:
0377 4849 0000 0070 00F0
0378 305C 00C0 00C0 00F0
0379 4809 20C3 0010 00F0
037A 032C 0000 0030 0060
037B 032C 0000 0030 0060
037C 4809 00C0 0030 00F0
037D 2F30 00C0 0030 0060
037E 4809 20C1 0070 00F0
037F 007C 0000 0070 0040
0380 4809 0F45 0010 00F0
0381 2F30 0000 0070 0060
0382 48C9 0C40 2070 00F0
0383 066C 0000 0030 0060
0384 3760 0700 0000 0040
0385 4809 0000 0030 00F0
0386 4809 00C0 0030 00F0
0387 0000 0000 0000 0020
0388 4809 00C0 2070 00F0
0389 4809 0001 9030 00F0
038A 4809 0001 1000 00F0
038B 4809 0001 7070 00F0
038C 0019 0000 0030 00F0
038D 0019 0000 0030 00F0
038E 0670 0000 0030 0040
038F 4809 20C3 0010 00F0
0390 0670 0000 0030 0040
0391 2F3C 00C0 00C0 00F0
0392 4809 0C40 2070 00F0
0393 4809 00C1 0030 00F0
0394 3000 00C0 0070 0030
0395 4809 0C41 0020 00F0
0396 00C0 00C0 0030 0030
0397 4809 0C40 0090 00F0
0398 2F5C 0000 0030 0060
0399 376C 0000 0000 0040

PRTO:
039A 3050 0000 0000 0060
039B 4809 20C3 0010 00F0
039C 032C 0000 0030 0060

OUTDEV: SP00 - 1 = MPCR
PRIO - 1 = MPCR
N311HP - 1 = MPCR

SET L02
COMPRES - 1 = CPOR
LIT + 1 = HAR2
10CW = LIT
EINPOT - 1 = CPOR
P = MIR
LIT L = 6B1
7 = LITJ COMP 16 = SAR
B = MIRJ ASE
BHAR + 1 = HAR2
EINPOT - 1 = CPOR
B = A2
10C10 - 1 = CPOR
B0SP0 - 1 = MPCR
A2 = MIR
A3 R = A2
16 = SAR
A2 - 1 = A2
A3 C = A3
A3 - 1 = A3
A4 C = A3
A2 EOL 0
DECODE - 1 = MPCR
LIT + 1 = HAR2
10CW = LIT
EINPOT - 1 = CPOR
R L = B
B = A2+ B M1
COMP 1 = SAR
A2 + B L = BR1
COMP 8 = SAR
A2 + B = MIR
EOUTPUT - 1 = CPOR
SP00 - 1 = MPCR

COMPRES - 1 = CPOR
LIT + 1 = HAR2
10CW = LIT

SEI L02
COMPRES - 1 = CPOR
LIT + 1 = HAR2
10CW = LIT
EINPOT - 1 = CPOR
P = MIR
LIT L = 6B1
7 = LITJ COMP 16 = SAR
B = MIRJ ASE
BHAR + 1 = HAR2
EINPOT - 1 = CPOR
B = A2
10C10 - 1 = CPOR
B0SP0 - 1 = MPCR
A2 = MIR
A3 R = A2
16 = SAR
A2 - 1 = A2
A3 C = A3
A3 - 1 = A3
A4 C = A3
A2 EOL 0
DECODE - 1 = MPCR
LIT + 1 = HAR2
10CW = LIT
EINPOT - 1 = CPOR
R L = B
B = A2+ B M1
COMP 1 = SAR
A2 + B L = BR1
COMP 8 = SAR
A2 + B = MIR
EOUTPUT - 1 = CPOR
SP00 - 1 = MPCR

COMPRES - 1 = CPOR
LIT + 1 = HAR2
10CW = LIT

IF L02
ASE
BHAR + 1 = HAR2
EINPOT - 1 = CPOR
B L = BR1
COMP 8 = SAR
A2 R = A2
14 = SAR
A2 + AMPCR = AMPCR
03JDEV - 1 = AMPCR
STEP
EXEC

```

```

* INITIATED BY THE BUFFER ADDRESS IN C1274C00
* PRINTED, CRT, OR DISK (NOT IMPLEMENTED) C1274C00
* (10CW) = A2J HAR2 = 10CW
* REFERENCE DR2
* 10CW + 1
* B = (10CW+1)
* STORE (10CW + 1) BUFFER ADDRESS IN BR1
C1264C00
C1265C00
C1266C00
C1267C00
C1268C00
C1269C00
C1270C00
C1271C00
C1272C00
C1273C00
C1274C00
C1275C00
C1276C00
C1277C00
C1278C00
C1279C00
C1280C00
C1281C00
C1282C00
C1283C00
C1284C00
C1285C00
C1286C00
C1287C00
C1288C00
C1289C00
C1290C00
C1291C00
C1292C00
C1293C00
C1294C00
C1295C00
C1296C00
C1297C00
C1298C00
C1299C00
C1300C00
C1301C00
C1302C00
C1303C00
C1304C00
C1305C00
C1306C00
C1307C00
C1308C00
C1309C00
C1310C00
C1311C00
C1312C00
C1313C00
C1314C00
C1315C00
C1316C00
C1317C00

```

```

* WRITE SP0 FUNCTION
* CALCULATES 10CW + 1 WILL BE USED
* COMPRESS BUFFER TO 32 BIT 1/0 FORMAT
* BUFFER ADDRESSES TO PIN
* MIR CONTAINS 7/BUFFER ADDR.
* BUFFER LENGTH INTO B (HAIL00X-1)
* TRANSFER BUFFER LENGTH INTO A2
* SAVE A2 IN MIR
* ISOLATE COUNTER
* DECREMENT COUNTER
* INCREMENT COUNTER IN A3
* TEST THE COUNTER FOR ZERO
* REGENERATE BUFFER ADDRESS IN B
* R = BUFFER LENGTH+ A2 = BUFFER ADDR
* MULTIPLY B BY 2
* NEW BUFFER ADDR IN BR1
* NEW BUFFER ADDRESS IN 10CW + 1
* WRITE PRTO FUNCTION
* COMPRESS THE BUFFER
* REGENERATE BUFFER ADDRESS

```





```

0320 2630 08C0 0020 006C
032E 4809 0C40 0930 00F0
033F 4809 08C1 0F30 00F0
0340 0C00 0000 00C0 0020
0341 4809 0C43 0030 00F0
0342 0680 0000 0000 0060
0343 39AC 0000 0000 0040
0344 4809 0E00 0A00 00F0
0345 0000 0000 0000 002C
0346 4809 0E0E 2000 00F0
0347 4809 0E01 9F00 00F0
0348 4809 030E 1000 00F0
0349 4809 0F01 9000 00F0
034A 4809 0012 0030 00FC
034B 6019 0000 0030 00F0
034C 0690 0000 0000 0040
034D 4809 20C3 001C 00F0
034E 0320 0000 0000 00E0
034F 253C 0000 0000 0060
0350 4809 2041 0020 00F0
0351 4809 0000 0000 0000
0352 4809 2540 0030 00F0
0353 2F50 0000 0000 0060
0354 3990 0000 0000 0040

IN:
0285 3809 0F00 0030 00F0
0286 4809 0000 0A00 00F0
0287 4000 0000 0030 0010
0288 4809 0C40 0030 00F0
0289 06A0 0000 0F30 00C0
028A 4809 0000 0000 00F0
028B 4824 0000 0030 00F0

INDEV:
030C 0680 0000 0030 0040
030D 06CC 0000 0000 0040
030E 0600 0000 0000 0040

SP01:
02BF 4809 2000 001C 00F0
02C0 032C 0000 0000 00FC
02C1 4809 0C43 0030 00F0
02C2 4809 0C41 0020 00F0
02C3 4809 0C41 0020 00F0
02C4 0000 0000 0000 0030
02C5 4809 2001 0F00 0030
02C6 0060 0000 0000 0040
02C7 4809 0C40 0030 0040
02C8 0600 0000 0000 0060
02C9 380F 0000 0000 0040
02CA 4809 0E00 9030 00FC
02CB 0000 0000 0030 0020
02CC 4809 0000 1000 00F0
02CE 4809 0000 1000 00F0
02CF 014C 0000 0000 00E0
0300 334C 0000 0030 0060
0301 4809 0E00 0A00 00FC

INPUT - 1 = CPCR
B = MIR
L = B01
COMP 16 = SAR
B = MIR
10C10 - 1 = CPCR
PPR10 - 1 = MPCR
A3 R = A2
16 = SAR
A2 - 1 = A2
A3 C = A3
A3 - 1 = A3
A3 C = A2
A2 EOL 0
IF FALSE THEN SKIP
0PC00E - 1 = MPCR
LIT + 1 = MAR2
10C = LIT
FINPUT - 1 = CPCR
LIT + 01 COP 8 = SAR
LIT + 01 = MIR
E0U1PUT - 1 = CPCR
FR10 - 1 = MPCR

% STORE BUFFER ADDRESS IN IIR
% ISOLATE COUNTER
% DECREMENT COUNTER
% DECREMENT COUNTER IN A3
% RESTORE A3
% IS COUNTER = 0
% REGENERATE BUFFER ADDRESS
% WRITE NEW ADDRESS IN 0R1
% WRITE NEW BUFFER ADDR IN 10C4 + 1
% THIS ROUTINE INPUTS DATA FROM PERIPHERAL DEVICES TO THE DESIGNATED BUFFERS. CR0 READER, CRT, OR DISK (M1)
% CLEAR LC2
% A2 = (10C4)
% A2 CONTAINS REVISE CODE
% DISK NOT IMPLEMENTED
% READ SP0 FUNCTION:
% RETRIEVE BUFFER ADDR.
% STORE BUFFER ADDR IN MIR
% STORE ADDRESS IN 0R1
% ISOLATE COUNTER
% DECREMENT COUNTER
% RESTORE A3, LHM CLEARED
% BUFFER EXPANSION FACTOR IN LHM OF A3
% EXPAND BUFFER
% ISOLATE COUNTER

```







```

01439400 D
01440000 C
01441000 D
01442000 D
01443000 D
01444000 D
01445000 D
01446000 D
01447000 D
01448000 D
01449000 D
01450000 C
01451000 C
01452000 C
01453000 D
01454000 C
01455000 D
01456000 D
01457000 D
01458000 D
01459000 D
01460000 D
01461000 D
01462000 D
01463000 D
01464000 D
01465000 C
01466000 C
01467000 D
01468000 D
01469000 D
01470000 D
01471000 D
01472000 D
01473000 D
01474000 C
01475000 D
01476000 D
01477000 D
01478000 D
01479000 D
01480000 C
01481000 D
01482000 C
01483000 C
01484000 D
01485000 D
01486000 D
01487000 D
01488000 C
01489000 C
01490000 D
01491000 D
01492000 C
01493000 D
01494000 C
01495000 D
01496000 D
01497000 D

```

```

* IWI AT Y = IYI + (RCH)
* LC2 INDICATS BYTE INSTRUCTION
* ROUTINES RETURN P = Y
* STORE A3 WITH RETURN ADDR* IN STACK
* WRITE TO EMULATION RESERVE BUFFER
* CLEAR UHW OF A3
* UHW OF A3 CONTAINS IYI
* UHW OF A3 CONTAINS INSTRUCTION
* D = (RCH)
* A2 CONTAINS IYI
* CALCULATE ADDRESS OF Y
*
*
* INDIRECT ADDRESSING WITHOUT INDEXING
* IWI AT Y = IYI
* LC2 INDICATES BYTE INST./ ROUTINE
* RETURNS P = Y AND A2 = ((H))
* WRITE A3 WITH RETURN IN UHW
* RETRIEVE IYI: FIELD
*
* THIS ROUTINE READS IN IWI AND TESTS
* IF CASCADED OR DIRECT ADDRESSING IS
* REQUIRED.
* CLEAR UHW OF A3
* UR2 = IWI ADDRESS
* SAVE IWI ADDR IN UHW OF A3
* B = (IWI)
* TEST IF BIT 14 OF IWI IS SET
*
* IF BIT SET, CASCADED IM
* IF BIT NOT SET, FORM Y
*
* THIS ROUTINE DECIDES WHICH ADDRESSING
* FORMULA TO USE TO COMPUTE THE NEW
* LOCATION OF THE INDIRECT WORD
* A2 IS BIT MASK FOR J FIELD OF IWI

```

```

LIT = MAR2
STACK = LIT
A3 = MIR
EUIPUT - 1 = CPCR
IFETCH - 1 = CPCR
COMP 16 = SAR
A3 OR B = A3
P L = R
CONTENSIRM-1 = CPCR
A3 R = A2
16 = SAR
A2 + B = B
INDIRMD - 1 = MPCR

IANDI:
LIT = MAR2
STACK = LIT
A3 = MIR
EUIPUT - 1 = CPCR
IFETCH - 1 = CPCR
INDIRMD - 1 = MPCR

INDIRMD:
A3 L = A3
COMP 16 = SAR
A3 R = A3
P L = BR2
COMP 8 = SAR
P L = R = SAR
COMP 16 = SAR
A3 OR B = A3
EMULIN - 1 = CPCR
B R = A2
14 = SAR
IF LST THEN STEP ELSE SKIP
LASCADED - 1 = MPCR
DIRECT - 1 = MPCR

CASCADED:
R101 C = A2
19 = SAR
A2 AND B = A2
12 = SAR

C402 4809 20C3 001C 00F0
C403 02CC 0000 0000 00E0
C404 4809 E000 0086 00F0
C405 2F5C 00C3 0030 00E0
C406 072C 0003 00C0 00E0
C407 4809 0000 0000 00E0
C408 4809 0000 0000 00E0
C409 4809 0000 9C00 00F0
C40A 4809 0041 0020 00F0
C40B 4809 1C5C 1000 00F0
C40C 238C 00C3 0070 00E0
C40D 4809 E000 AC00 00F0
C40E 0000 0000 0070 0020
C40F 4809 CC40 0020 00FF
C410 0730 0000 0070 0040

C411 4809 20C3 001C 00F0
C412 02CC 0003 0030 00E0
C413 4809 E000 0030 00F0
C414 2F5C 00C3 0030 00E0
C415 074C 00C3 0000 00E0
C416 0750 00C3 00C0 0040

C417 4809 E001 1070 00C0
C418 0000 0000 0000 0020
C419 4809 E000 9000 00E0
C41A 4809 0041 001C 00E0
C41B 0000 00C0 0000 003C
C41C 4809 0041 003C 00F0
C41D 0000 0000 0000 0020
C41E 4809 EC5C 1070 00FF
C41F 076C 00C0 0070 00E0
C420 4809 CC40 AC00 00F0
C421 400C 00C0 0030 0010
C422 4809 C0C3 C070 0010
C423 580B 00C0 0000 00F0
C424 077C 0000 0000 004C
C425 0780 00C3 0070 0040

C426 4809 18C1 AC3C 00E0
C427 3000 00C3 0030 0020
C428 4809 C055 A030 00FF
C429 300C 00C0 0070 001C

```



042A	4809	C64D	00C0	00F0					0158F000	D
042B	079C	00D3	00F0	C0C0					01589F00	D
042C	4809	00D0	00F0	C0C0					01580400	D
042D	4824	00D0	00F0	C0C0					01582000	D
									01580300	D
042E	0740	00D0	00B0	00A0					01580400	D
042F	0740	00C0	00A0	00A0					01580500	D
0430	074C	00C3	00C0	00A0					01580600	D
0431	07D0	00D0	00B0	00A0					01580700	D
									01580800	D
0432	4809	E0D0	A0C0	00F0					01580900	D
0433	00C0	00D0	00F0	0020					01581000	D
0434	4809	C0D3	0640	00F0					01581200	D
0435	00D0	00F0	00C0	003C					01581300	D
0436	07EC	00D0	00F0	0060					01581400	D
0437	416C	00C0	00B0	00A0					01581500	D
									01581600	D
									01581700	D
									01581800	D
									01581900	D
									01582000	D
									01582100	D
									01582200	D
									01582300	D
									01582400	D
									01582500	D
									01582600	D
									01582700	D
									01582800	D
									01582900	D
									01583000	D
									01583100	D
									01583200	D
									01583300	D
									01583400	D
									01583500	D
									01583600	D
									01583700	D
									01583800	D
									01583900	D
									01584000	D
									01584100	D
									01584200	D
									01584300	D
									01584400	D
									01584500	D
									01584600	D
									01584700	D
									01584800	D
									01584900	D
									01585000	D
									01553000	D
									01553100	D
									01553200	D
									01553300	D
									01553400	D
									01553500	D
									01553600	D
									01553700	D
									01553800	D
									01553900	D
									01554000	D
									01554100	D
									01554200	D
									01554300	D
									01554400	D
									01554500	D
									01554600	D
									01554700	D
									01554800	D
									01554900	D
									01555000	D
									01555100	D
									01555200	D
									01555300	D
									01555400	D
									01555500	D
									01555600	D
									01555700	D

0438	4809	2C5E	0030	00F0							
0439	00F0	00C0	00F0	00E0							
043A	07F0	00C0	0030	00E0							
043B	2F3C	00D3	0030	00E0							
043C	0800	00D3	0030	00A0							
043D	2380	00D3	0030	00C0							
043E	0810	00C0	00D0	00A0							
043F	4809	E156	087C	00F0							
0440	00C0	00D0	00F0	00E0							
0441	4809	0C46	0870	00F0							
0442	0870	00D0	00F0	00E0							
0443	2F3C	00D3	0030	00E0							
0444	083C	00C0	00B0	00A0							
0445	4809	E0C9	A0D0	00F0							
0446	00C0	00D0	00F0	00E0							
0447	4809	F0D0	0610	00F0							
0448	00C0	00C0	00F0	0030							
0449	4809	0C40	20A0	00F0							
044A	084C	00D3	0030	00E0							
044B	4809	CC40	087C	00F0							
044C	416C	00C0	00D0	00A0							
044D	4809	18C1	AC20	00F0							





```

044E 3000 0000 0000 0020
0450 4800 C658 A030 00F0
0454 4809 C650 0030 00F0
0458 4809 C640 0030 00F0
0452 085C 0000 0000 00C0
0453 4809 0000 0000 00C0
0454 4824 0000 0030 00F0

DIRADDR: D10 - 1 = MPCR
0455 0860 0000 0030 0040
0456 0870 0000 0030 0040
0457 0880 0000 0030 0040
0458 0890 0000 0030 0040

D10:
A3 R = A2
16 = SAR
A2 OR 1 L = BR2
COMP B = SAR
0459 4809 E0C3 A030 00F0
045A 0000 0000 0030 0020
045B 4809 C0C3 0010 00F0
045C 0000 0000 0030 0030
045D 38A0 0000 0000 0060
045E 3809 0000 0030 00F0
045F 0860 0000 0030 0040

D11:
B AND LIT = B
15 = LIT
REGSTACK - 1 = CPCR
EIMPUT - 1 = CPCR
DIGN - 1 = MPCR
0460 4809 2C55 0E30 00F0
0461 00F0 0000 0000 0060
0462 08C0 0000 0000 0060
0463 2F30 0000 0000 0060
0464 0800 0000 0030 0040

D12:
A3 AND LIT = B
15 = LIT
REGSTACK - 1 = CPCR
EIMPUT - 1 = CPCR
DIGN - 1 = MPCR
0465 4809 E156 0E30 00F0
0466 00F0 0000 0000 0060
0467 08E0 0000 0000 0060
0468 2F30 C0C0 0000 0060
0469 08F0 0000 0030 0040

D13:
A3 AND LIT = B
15 = LIT
R + 1 = B
REGSTACK - 1 = CPCR
EIMPUT - 1 = CPCR
DIGN - 1 = MPCR
046A 4809 E155 0B30 00F0
046B 00F0 0000 0000 0060
046C 4809 0C46 0B30 00F0
046D 0F0C 0000 0000 0060
046E 2F3C 0000 0000 0060
046F 0F1C 0000 0000 0040

D1GN:
A3 R = A2
16 = SAR
A2 OR 1 L = BR2
0470 4809 E0C0 A0C0 00F0
0471 0000 0000 0000 0020
0472 4809 C0C3 0010 00C0
0473 0000 0000 0000 0030
0474 4809 0E40 2030 00F0
0475 0920 0000 0000 0060
0476 4809 C0C3 0030 00F0

```

```

01558C00 0
01559000 0
01560000 0
01561000 0
01562000 0
01563000 0
01564000 0
01565000 0
01566000 0
01567000 0
01568000 0
01569000 0
01570000 0
01571000 0
01572000 0
01573000 0
01574000 0
01575000 0
01576000 0
01577000 0
01578000 0
01579000 0
01580000 0
01581000 0
01582000 0
01583000 0
01584000 0
01585000 0
01586000 0
01587000 0
01588000 0
01589000 0
01590000 0
01591000 0
01592000 0
01593000 0
01594000 0
01595000 0
01596000 0
01597000 0
01598000 0
01599000 0
01600000 0
01601000 0
01602000 0
01603000 0
01604000 0
01605000 0
01606000 0
01607000 0
01608000 0
01609000 0
01610000 0
01611000 0
01612000 0
01613000 0
01614000 0
01615000 0
01616000 0
01617000 0

```

```

X MASK IJ1 FIELD OF IJ1
X ISOLATE BIT VALUE IN A2
X COMPUTE JUMP TABLE ADDRESSES
X FOR FORMULA DESIRED
X
X
X Y = IJ2
X SHIFT ADDR OF IJ1 INTO A2
X
X B = (IY2)
X CLEAR BYTE BIT(IF SET) LC2 = HS BYTE
X
X Y = IY2 + (RXY)
X ISOLATE RX FROM IY1
X B = (RXY)
X
X Y = IY2 + (RHM)
X MASK OFF IY1 FIELD IM: = RM
X B = (RHM)
X
X Y = IY2 + (RCH+1)
X MASK OFF RM INTO B
X B = RM + 1
X P = (RCH+1)
X
X THIS ROUTINE COMPUTES Y, TEST FOR BYTE
X INST., AND RETURNS TO CALLER OF
X RYMFIELD.
X IY1 ADDR INTO BR2 IMC, BY 1
X
X SAVE (RXY), (RHM), OR (RCH+1) IN A2
X B = (IY2)

```







04A3 4809 C240 2000 00F0  
 04A4 4809 0000 0000 20F0  
 04A5 4809 0F43 001F 00F0  
 04A6 0970 0000 0000 00F0  
 04A7 4809 0C40 0030 00F0  
 04A8 48C9 00C0 0030 00F0  
 04A9 4809 E001 F010 00F0  
 04AA 0C00 00C0 0030 00F0  
 04AB 4809 E000 9F70 00F0  
 04AC 0000 0000 0000 00F0  
 04AD 4809 E0C1 1000 00F0  
 04AE 4809 E5C0 1000 00F0  
 04AF 0900 0000 9000 00F0  
 04B0 4809 E0F1 2000 00F0  
 04B1 0000 0000 0070 00F0  
 04B2 4809 00C0 4000 00F0  
 04B3 4809 E000 9000 00F0  
 04B4 4809 E5C1 1000 00F0  
 04B5 4809 E5C0 1000 00F0  
 04B6 4809 E5C0 1000 00F0  
 04B7 4809 0E40 8070 00F0  
 04B8 0000 00C0 0070 00F0  
 04B9 4809 0E40 8070 00F0  
 04BA 4809 E001 9F30 00F0  
 04BB 0000 00C0 0000 00F0  
 04BC 4809 E30E 1030 00F0  
 04BD 4809 0C43 0000 00F0  
 04BE 4809 0C43 0000 00F0  
 04BF 4809 E0F1 9070 00F0  
 04C0 4809 0C52 0030 00F0  
 04C1 0000 00C0 0000 00F0  
 04C2 600E 0000 0000 00F0  
 04C3 4A3C 0000 0000 00F0  
 04C4 4809 C000 0040 00F0  
 04C5 48C9 C000 0000 00F0  
 04C6 482D 0000 0070 00F0

04C7 4809 0000 1000 00F0  
 04C8 2009 00C3 0070 00F0  
 04C9 0900 00C3 0070 00F0  
 04CA 0900 00C3 0070 00F0  
 04CB 4809 0C52 0070 00F0  
 04CC 5A00 C040 0000 00F0  
 04CD 4A49 C040 0000 00F0  
 04CE 4C0B C0C2 2000 00F0  
 04CF 48C9 C0C2 2000 00F0  
 04D0 4809 0C40 0070 00F0  
 04D1 4C09 0C5E 0030 00F0  
 04D2 2B19 C7C3 0070 00F0  
 04D3 09AC 0000 0000 00F0  
 04D4 48C9 C0C3 0000 00F0  
 04D5 5C09 EC40 1000 00F0  
 04D6 4809 C000 0000 00F0  
 04D7 1000 C000 0070 00F0

AMPCR = A2  
 ASR  
 BHAR = DR2  
 EMULIN - 1 = CPCR  
 R = MIR  
 A2 = B  
 A3 L = BR2  
 CDPB B = SAR  
 A3 R = A3  
 16 = SAR  
 A3 L = A3  
 A3 OR B = A3  
 EMULOUT - 1 = CPCR  
 A3 L = A2  
 COMP 16 = SAR  
 A2 R = A2  
 A3 L = A3  
 A3 L = A3  
 BWA00 B = B  
 BHAR B = A3, ASR  
 BHAR R = B, CGEAR  
 B = SAR  
 B + 1 L = PR1  
 B + C = A3  
 16 = SAR  
 A3 - 1 = A3, B  
 B L = B  
 B R = B  
 A3 C = A3  
 R EOL 0  
 COMP 8 = SAR  
 IF FALSE THEN STEP ELSE SKIP  
 HRPT - 1 = MPCR  
 A2 = AMPCR  
 STEP  
 JUMP

C = A3  
 16 = SAR  
 LCI THEN SET LCI1 SKIP  
 C EOL B = MPCR  
 IF FALSE THEN A2 XOR R1 STEP ELSE JUMP  
 A2 IF M5T THEM SET LC2  
 IF M5T THEN NOT A2 = A21  
 A2 + 1 = A2  
 P  
 IF M5T THEN C - B = R  
 IF LCI THEN SKIP  
 RREG - 1 = MPCR  
 IF L5T THEN A3 + B = A3  
 A2 R = A21, CSAR  
 1 = SAR

THIS ROUTINE WILL MULTIPLY 2 VALUES.  
 THE OPERANDS MUST BE PASSED BY A2 AND  
 LCI MUST BE SET IF 32 BIT NUMBERS ARE  
 PASSED. PRODUCT IS RETURNED IN A3.  
 HOLDS PARTIAL PRODUCT  
 DOUBLE PACK SINGLE REG VALUES  
 XOR R1 STEP ELSE JUMP CHECK FOR NEG PROD  
 STEP ELSE SKIP  
 TWO'S COMPLEMENT  
 BRING B TO THE ADDR  
 COMPLEMENT F  
 RESTORE SINGLE REG TO LS WORDS  
 BRING A2 TO THE ADDR  
 L5T THEN A3 + B = A3  
 SHIFT OFF LS BIT OF A2



```

0408 4809 0C41 0870 00F0
C409 4809 00B0 0030 00FF
040A 4809 0312 0C30 00F0
040B 4819 08E0 0090 00F0
040C 403C 00E0 0030 0040
040D 3C00 0D02 1C80 00FF
040E 4809 0D03 1000 00F0
040F 4820 0709 0030 00F0
0410 4809 0C41 0830 00F0
0411 4809 0011 2030 00F0
0412 4809 0010 400C 00F0
0413 4809 0010 400C 00F0
0414 4809 0C40 8830 00F0
0415 403C 00E0 0030 0040

C4E6 09B0 00A3 0000 0060
04E7 4809 0540 0870 00F0
04E8 0CE0 0000 0030 00C0
04E9 4809 7C41 0C20 00F0
04EA 008F 00C0 00C0 00B0
04EB 09C0 00E0 0C30 0040

C4EC 0900 00B0 0030 0060
04ED 48E9 0540 0830 00F0
04EE 4809 0C41 0C30 00C0
04EF 010C 00D0 0030 00B0
04F0 010C 00D0 0030 00B0
04F1 09E0 0C00 0030 0040

C4F2 360B 00C3 0070 00FC
04F3 4809 0C5E 0890 00F0
04F4 4809 0700 0070 00C0
04F5 48C9 00E0 00E0 00FF
04F6 4809 0C40 0C30 00FF
04F7 480B 00C0 0C30 00F0
04F8 09FC 00C0 00C0 0040
04F9 4809 00A3 0030 00F0
04FA 4809 0C40 0070 00F0
04FB 480B 00C3 0030 008C
04FC 0A00 00E0 0030 00FF
04FD 2600 00E0 0030 00FF
04FE 0A2C 00E0 0030 0040
04FF 0A2C 00E0 0030 0040
0500 260B 00E0 0C30 00FC
0501 0A3C 00E0 0C30 0040

B L = 0
A2
A2 EOL 0
IF TRUE THEN SKIP
MULTI - 1 = MPCR
IF LC2 THEN NOT A3 = A3
A3 + 1 = A3
JUMP
B L = B
A2 L = A2
MULTI - 1 = MPCR
A2 R = A2
B R = B
MULTI - 1 = MPCR

SAVEREG - 1 = CPCR
AMPCR = B
ERRORLIST = AMPCR
LIT + 0 L = BRI
B = LIT, COMP B = SAR
PTRERR - 1 = MPCR

SAVEREG - 1 = CPCR
AMPCR = B
ERRORLIST = AMPCR
LIT + 0 L = BRI
B = LIT, COMP B = SAR
PTRERR - 1 = MPCR

NOTIMP:
OVERFLOW:
CHECKOFF:
IF LC2 THEN STEP ELSE SKIP
A2 - B = E
A2
IF HST THEN SET LC1
A2 XOR B
IF HST THEN STEP ELSE SKIP
CLEAROV - 1 = MPCR
BMI
IF HST THEN STEP ELSE SKIP
SNEG - 1 = MPCR
IF LC1 THEN STEP ELSE SKIP
SETOVBIT - 1 = MPCR
CLEAROV - 1 = MPCR
IF LC1 THEN STEP ELSE SKIP
CLEAROV - 1 = MPCR

MULTIPLIER BY 2
CHECK TO SEE IF ENTIRE MULTIPLIER
HAS BEEN REAL
IF MULTIPLICAND = 0, THEN DONE
A3 STEP ELSE JUMP
MOVE B TO UHM
MOVE A2 TO UHM, 16 = SAR
CONTINUE MULTIPLY
RESTORE REG TO LHM
RESTORE REG TO LHM

THIS ROUTINE SETS UP AN ERROR MESSAGE
*NOT IMPLEMENTED* INSERTIO VIA LOADER
JCL

THIS ROUTINE WILL PRINT OUT AN ERROR
DIAGNOSTIC INSERTED VIA LOADER JCL AND
ABORTS MACHINE EXECUTION.

TRANSFER ERRORLIST ADDR TO B
CREATE ERRORLIST ADDR IN BRI
PRINT THE ERROR MESSAGE AND STOP
OVERFLOW BIT SETTING

THIS ROUTINE WILL SET THE OVERFLOW BIT
IF REQUIRED, OTHERWISE CLEAR IT
A2 HOLDS ***, B HOLDS ***, AND MIR
HOLDS THE ALG SUM (IN MS WORDS)
IF LC2 IS SET, IT IMPLIES A NEGATIVE
SKIP
TEST FOR A SUBTRACTION OP CODE
A2 TO THE ADDR
IMPLIES X IS NEGATIVE
CHECK FOR *LIKE* SIGNS
CLEAR THE 0V BIT, UNLIKE SIGNS

IF HST THEN STEP ELSE SKIP
CHECK FOR NEG SUM
NEG SUM, LIKE SIGNS
IF LC1 THEN STEP ELSE SKIP
POS SUM, LIKE SIGNS, NEG X
POS SUM, LIKE SIGNS, POS X
IF LC1 THEN STEP ELSE SKIP
NEG SUM, NEG X, LIKE SIGNS

```





OY01T: IF LCI THEN STEP ELSE SKIP \* THIS ROUTINE WILL SET THE  
SETIOVBIT - 1 = MPCR \* OVERFLOW BIT IN SR01 IF LCI IS SET  
CLEAROV - 1 = MPCR \* OTHERWISE, CLEAR THE OVERFLOW BIT

CLEAROV: A1 C = A1 \* THIS ROUTINE WILL CLEAR THE OVERFLOW  
27 = SAR \* BIT IN SR01  
A1 AND R110 = A1,CSAR \*  
A1 C = A1J IF LCI \* CLEAR LCI FROM CHECKOV  
JUMP

01804000 0  
01805000 0  
01806000 0  
01807000 0  
01808000 0  
01809000 0  
01810000 0  
01811000 0  
01812000 0  
01813000 0  
01814000 0  
01815000 0  
01816000 0  
01817000 0  
01818000 0  
01819000 0  
01820000 0

SETIOVBIT: \* THIS ROUTINE SETS THE OVERFLOW BIT IN  
\* POSITION 27 OF PSW

01821000 0  
01822000 0  
01823000 0  
01824000 0  
01825000 0  
01826000 0  
01827000 0  
01828000 0  
01829000 0  
01830000 0  
01831000 0  
01832000 0  
01833000 0  
01834000 0  
01835000 0  
01836000 0  
01837000 0  
01838000 0  
01839000 0  
01840000 0

\* \*\*\*\*\* END OF  
PRTERR: \* THIS ROUTINE IS CALLED WHENEVER AN  
\* ERROR PRINTOUT IS GENERATED.  
\* B HAS THE ERRORLIST NUMBER.  
\*  
\* WRITE A BLANK LINE  
\* WRITE PRINTBUFF ADDRESS INTO A3  
\* LOAD COUNT IN UHW OF A3  
\* 8 WORDS WILL BE MOVED  
\* MOVE ERROR DIAGNOSTIC INTO PRINTBUFF  
\* WRITE ERROR LIST MESSAGE  
\* RESTORE LU REGISTERS  
\*  
\* THIS ROUTINE CHECKS THE STACK  
\* DESIGNATION BIT IN SR01 TO DETERMINE  
\* WHICH STACK THE PROGRAMMER IS USING.  
\* THE REGISTER IS ASSUMED TO HAVE THE  
\* WRAPAROUND IS ALLOWED.  
\* STORE THE REGISTER  
\* POSITION STACK DESIGNATOR BIT IN LS  
\* POSITION REG BIT. IN LS FIT  
\* SEND A1 TO THE ADDR  
\*  
\* RESTORE A1 TO NORMAL SR01/PAR FORMAT

01841000 0  
01842000 0  
01843000 0  
01844000 0  
01845000 0  
01846000 0  
01847000 0  
01848000 0  
01849000 0  
01850000 0  
01851000 0  
01852000 0  
01853000 0  
01854000 0  
01855000 0  
01856000 0  
01857000 0  
01858000 0  
01859000 0  
01860000 0

CLEARBUFF - 1 = CPCR  
WRITEBUFF - 1 = CPCR  
AMPCR = A3  
PRINTBUFF = AMPCR  
LIT L = B  
8 = LITJ COMP 16 = SAR  
A3 OR B = A3  
MOVE - 1 = CPCR  
WRITEBUFF - 1 = CPCR  
CLEARBUFF - 1 = CPCR  
WRITEBUFF - 1 = CPCR  
RESREG - 1 = CPCR  
STOPTIME - 1 = MPCR

01861000 0  
01862000 0  
01863000 0  
01864000 0  
01865000 0  
01866000 0  
01867000 0  
01868000 0  
01869000 0  
01870000 0  
01871000 0  
01872000 0  
01873000 0  
01874000 0  
01875000 0  
01876000 0  
01877000 0  
01878000 0  
01879000 0  
01880000 0

REGSTACK: B = MAR2  
A1 C = A1  
16 = SAR  
A1  
IF LAST THEN STEP ELSE SKIP  
STACK2 - 1 = MPCR  
LIT EOL D  
16 = LIT  
IF TRUE THEN STEP ELSE SKIP  
0 = MAR2  
A1 C = A1J JUMP

01881000 0  
01882000 0  
01883000 0  
01884000 0  
01885000 0  
01886000 0  
01887000 0  
01888000 0  
01889000 0  
01890000 0  
01891000 0  
01892000 0  
01893000 0  
01894000 0  
01895000 0  
01896000 0  
01897000 0  
01898000 0  
01899000 0  
01900000 0

0500 4809 4001 0030 0000  
0506 4809 4001 0070 0000  
0507 3000 0000 0030 0000  
0508 4809 400E 4010 4000  
0509 2809 40C1 0070 0000  
050A 4820 0000 0070 0000  
050B 4809 4001 0030 0000  
050C 3000 0000 0030 0000  
050D 4809 40C0 0000 0000  
050E 4820 0000 0030 0000  
0510 1F40 0000 0070 0000  
0511 0A7C 00C0 0000 0000  
0512 4809 0640 1070 0000  
0513 059F 0000 0070 0000  
0514 4809 20C1 0000 0000  
0515 0080 0000 0000 00A0  
0516 4809 05C0 1000 0000  
0517 4A2C 0000 0030 0000  
0518 0A80 0000 0000 0060  
0519 1F4C 00C0 0000 0060  
051A 0A90 00C0 0000 0060  
051B 0A4C 0000 0070 0060  
051C 0A80 0000 0000 00A0  
051D 4809 0C40 001C 0000  
051E 4809 4001 0000 0000  
051F 0000 0000 0070 0020  
0520 4809 0000 0000 0000  
0521 5800 00C0 0000 0000  
0522 0A0C 00C0 0070 00A0  
0523 4809 2C52 0000 0000  
0524 0100 00C0 0070 0000  
0525 5800 0000 0000 0000  
0526 4809 00C0 001C 0000  
0527 4820 40C1 0030 0000



```

0524 8809 2C8J 001C 001C
0529 0100 0000 0030 00E0
052A 8809 2C8J 0000 00E0
052B 0200 0000 0030 00E0
052C 6819 0000 0030 00F0
052D 8820 ACC1 0000 00F0
052E 8809 20C7 001C 00F0
052F 0100 0000 0000 00E0
0530 8820 ACC1 0000 00F0

0531 8809 0680 0030 00F0
0532 8809 20C3 001C 00F0
0533 0260 0000 0000 00E0
0534 2F30 0000 0000 006C
0535 8809 0C40 0030 00F0
0536 2F30 0000 005C 00F0
0537 8809 0C40 2000 00F0
0538 8809 0F45 001C 00FC
0539 2F30 0000 0000 0060
053A 8809 20C3 1000 00F0
053B 8809 20C7 001C 00F0
053C 8809 20C7 001C 00F0
053D 2F30 0000 0030 006C
053E 8809 0C40 0030 00F0
053F 8809 0C40 0030 00F0
0540 8809 0000 0030 00F0
0541 8820 0000 0000 00F0

0542 8809 0680 0030 00FC
0543 8809 2003 001C 00F0
0544 0200 0000 0000 00E0
0545 2F30 0000 0000 0060
0546 8809 0C40 2030 00F0
0547 0000 0000 0000 0000
0548 0020 0000 0000 0000
0549 8809 0000 0030 00F0
054A 8809 0191 2070 00F0
054B 8809 0000 0000 00F0
054C 8809 0000 0000 00F0
054D 8809 0001 4030 00FC
054E 8809 0001 4030 00FC
054F 8809 880E 4000 00FC
0550 0A00 0000 0030 0060
0551 8809 0C40 0030 00F0
0552 8809 0000 0000 00E0
0553 0000 0000 0030 0020
0554 8809 0001 4030 00F0
0555 8809 0000 8870 00F0
0556 8809 0000 4000 00F0
0557 8809 0000 0030 00F0
0558 8809 0000 0000 00F0
0559 883F 0000 0000 00F0

```

RESREG:

```

AMPCR = MIR
LIT + 1 = MAR2
WORKSPACE = LIT
EINPUT - 1 = CPGR
B = A1
EINPUT + 1 = MAR2
EINPUT - 1 = CPGR
EINPUT + 1 = CPGR
EINPUT - 1 = CPGR
R = A3
LIT = MAR2
EINPUT - 1 = CPGR
E = MIR+BHI
B = AMPCR+BHI
STEP
JUMP

```

RTSPSM:

```

AMPCR = MIR
LIT = MAR2
PSM = LIT
B = MIR+BHI
E = A2
EINPUT + 1 = CPGR
A2 + R = A2
A2 + LIT = A2
A2 OR B = A3
A1 R = A1
A1 L = A1, BHI
A1 OR B = A1
A1 AND B011 = A1
IFETCH - 1 = CPGR
B = MIR
A1 R = A1
16 = SAR
A1 L = A1
A3 R = B
A1 OR B = A1+BHI
A3 = AMPCR
STEP
RETN

```

THIS ROUTINE RESTORES THE REGISTERS

```

% OF THE LU IN WORKSPACE
% SAVE RETURN IN MIR
% MAR2 = WORKSPACE + 1

% RESTORE A1
% INCREMENT WORKSPACE ADDR
% RESTORE A2
% INCREMENT WORKSPACE ADDR
% RESTORE A3
% SELECT WORKSPACE BASE ADDR
% SWAP B AND MIR
% RESTORE AMPCR AND B

% THIS ROUTINE WILL PLACE THE CONTENTS
% OF PSM INTO THE PAR, THEN RESTORE
% THE PAR TO (PAR) + 2.
% SAVE RETURN ADDR TO OPCCOE IN MIR
% ADDRESS OF PSM

% (PSM) INTO B
% (PSM) INTO MIR, RETURN ADDR INTO 9
% PAR INTO A2
% RIGHT JUSTIFY (PAR)
% (PAR) + 2 = A2
% (PAR)+2/RETURN ADDR = A3
% CLEAR PAR

% (PSM) INTO PAR
% CLEAR BIASED FETCH BIT
% INSTRUCTION AT Y INTO B
% CLEAR PAR

% (PAR) + 2 = F
% RESTORE RETURN ADDR, INSTR IN B

```



R111

055A 4809 0000 0000 0000  
 055B 4809 EC01 1C0C 40F0  
 055C 0000 0000 0C7C C010  
 055D 4809 E0C3 0030 00FC  
 055E 4C09 0019 0B7C 00FC  
 055F 4809 0000 9000 00F0  
 0560 48C9 EC53 08C0 00F0  
 0561 0000 0000 0000 0020  
 0562 4809 A0C1 1C00 00F0  
 0563 4809 EC4D 8B00 00F0  
 0564 4809 A0C3 C000 00F0  
 0565 4809 A0D1 4C00 00FC  
 0566 4809 AC5C 4070 00F0  
 0567 0AEC 00C9 0C70 0040

RH1

0568 4809 0000 0000 24F0  
 0569 4809 064D 2C00 00F0  
 056A 0000 0000 0000 0000  
 056B 51C0 0000 0000 0060  
 056C 2F30 C0C9 0000 0060  
 056D 48C9 C0C3 0030 00FC  
 056E 4809 0C43 0C7C 00FC  
 056F 4800 00C3 0C7C 00FC  
 0570 482D 00C3 0070 00FC

C = B  
 A3 L = A3, CSAR  
 COMP 24 = SAR  
 A3  
 IF HST THEN B111 L = B  
 A3 R = A3  
 A3 OR B L = E  
 COMP 16 = SAR  
 A1 L = A3  
 A3 + B R = B  
 A1 R = A1  
 A1 L = A1  
 A1 OR B = A1  
 OPCODE - 1 = MPCR

REGSTACK - 1 = CPCR  
 EINPUT - 1 = CPCR  
 A2 = AMPCR  
 B = M1R  
 WAIT  
 JUMP

RXF1ELD:

0571 4809 E0E1 9000 00F0  
 0572 0000 0000 0000 0020  
 0573 4809 E65C 1030 00FC  
 0574 4809 E5E1 057C 00FC  
 0575 4809 E5E1 057C 00FC  
 0576 0E60 0000 0070 00E0  
 0577 4809 0052 0000 00FC  
 0578 6A08 0000 0000 00FC  
 0579 0AFC 00C0 002C 004F  
 057A 4809 2E53 0020 00FC  
 057B 0080 00C0 0000 00E0  
 057C 7800 0000 0C30 00FC  
 057D 0000 00C0 0C30 00FC  
 057E 4809 0C4D 2030 00FC  
 057F 500E 0000 0000 00FC  
 0580 3B1C 00C0 0C20 0040

THIS ROUTINE COMPUTES (P)\*D = P  
 AND JUMPS TO NEXT INSTRUCTION  
 EXAMINE SIGN BIT OF \*D\*  
 A3 TO THE ADDR  
 IF SIGN=1, FILL UPPER BYTE WITH 115  
 RESTORE \*D\* FIELD TO LS BYTE  
 B = SIGN/\*D\*, IN MS WORD  
 SAVE THE OLD PAR IN MS WORD OF A3  
 ALGEBRAICALLY ADD (P) + D  
 CLEAR OLD PAR  
 CREATE NEW PAR  
 1935:0000 D  
 1936:0000 D  
 1937:0000 D  
 1938:0000 D  
 1939:0000 D  
 1940:0000 D  
 1941:0000 D  
 1942:0000 D  
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 1968:0000 D  
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 1970:0000 D  
 1971:0000 D  
 1972:0000 D  
 1973:0000 D  
 1974:0000 D  
 1975:0000 D  
 1976:0000 D  
 1977:0000 D

THIS ROUTINE GETS THE CONTENTS OF RCM  
 THAT INDICATED IN MAR AND RETURNS  
 IN RCM  
 REFERENCE MAR  
 SAVE RETURN ADDRESS  
 SELECT REGISTER STACK TO BE USED  
 ADDR OF REG BEG STACK RETURNED IN MAR2  
 GET CONTENTS OF RCM  
 RESTORE RETURN ADDRESS  
 M1R IS USED AS TEMP STORAGE  
 FOR TEST PURPOSES  
 1950:0000 D  
 1951:0000 D  
 1952:0000 D  
 1953:0000 D  
 1954:0000 D  
 1955:0000 D  
 1956:0000 D  
 1957:0000 D  
 1958:0000 D  
 1959:0000 D  
 1960:0000 D  
 1961:0000 D  
 1962:0000 D  
 1963:0000 D  
 1964:0000 D  
 1965:0000 D  
 1966:0000 D  
 1967:0000 D  
 1968:0000 D  
 1969:0000 D  
 1970:0000 D  
 1971:0000 D  
 1972:0000 D  
 1973:0000 D  
 1974:0000 D  
 1975:0000 D  
 1976:0000 D  
 1977:0000 D

THIS ROUTINE ANALYZES THE \*M\* FIELD OF  
 A TYPE R INSTRUCTION. UPON ENTRANCE  
 A3 CONTAINS THE MOST SIGNIF. WORD OF  
 THE DOUBLEWORD INSTRUCTION. LC2  
 INDICATES BYTE INSTRUCTION. UPON EXIT  
 OF DAWI, DAWCI, OR INDIRACTION  
 A3 CONTAINS Y1. LC2 PASSES MSC0,LS(1)  
 PREPARE PS 2 BYTES OF A3 TO HOLD RETURN  
 ADDRESS FROM ADDR IN A3(UPPER HALF)  
 RESTORE A3 RETURN\_ADDR/INSTRUCTION  
 MASK OFF \*M\* FIELD  
 IS M = 07  
 JUMP TO DIRECT ADDRESS W/O INDEXING  
 TEST FOR H = 14XX  
 IF FALSE THEN STEP ELSC SKIP  
 JUMP TO DIRECT ADDR WITH INDEXING  
 FAV B IN A2  
 IF NOT LST THEN STEP ELSC SKIP  
 IF H = 10,12,14,16 THEN INDIRACTION  
 INDIR - 1 = MPCR









```

05A7 4809 18C1 A0D0 00F0 0
05A8 9000 0000 0030 002C 0
05A9 4809 00C5 889C 0010 0
05AA 2000 0000 0090 0010 0
05AB 08AC 00C0 0030 0040 0

SRM14:
05AC 4809 18C1 A0D0 00F0 0
05AD 3000 00C3 C070 002C 0
05AE 4809 00C5 889C 00F0 0
05AF 8000 00C0 0070 0010 0
05B0 08AC 00C0 0030 0040 0

SRM16:
05B1 4809 18C1 A0D0 00F0 0
05B2 1C00 00C0 0030 0020 0
05B3 4809 00C5 889C 00F0 0
05B4 A000 00C0 0070 0010 0
05B5 08CC 00D0 009C 0040 0

SRM18:
05B6 4809 205E 0030 00F0 0
05B7 0010 00C0 0000 00E0 0
05B8 7419 2052 0090 00F0 0
05B9 386C 00D3 009C 0040 0
05BA 0020 0000 0030 00E0 0
05BB 0000 0000 0000 0000 0
05BC 481C 0000 003C 0040 0
05BD 4400 00C0 0030 0040 0

SAVEREG:
05BE 4809 00D3 0030 24F0 0
05BF 4809 0C40 008C 00F0 0
05C0 4809 0640 089C 00F0 0
05C1 4809 20D3 0C1C 00F0 0
05C2 026C 00C0 003C 00E0 0
05C3 2F5C 00C3 0070 0060 0
05C4 4809 0F45 001C 00F0 0
05C5 4809 A0C0 0080 00F0 0
05C6 2F50 00C0 0000 0060 0
05C7 4809 0F46 001C 00F0 0
05C8 4809 00D0 0030 00F0 0
05C9 2F50 00C3 0070 0060 0
05CA 4809 0F46 001C 00F0 0
05CB 4809 00D0 0030 00F0 0
05CC 2F50 00C3 0070 0060 0
05CD 4809 0C43 008C 00F0 0
05CE 4809 00C3 0070 0060 0

02C397C00 0
0204C000 0
02041C00 0
02042C00 0
02043C00 0
02044C00 0
02045C00 0
02046C00 0
02047C00 0
02048C00 0
02049C00 0
02050C00 0
02051C00 0
02052C00 0
02053C00 0
02054C00 0
02055C00 0
02056C00 0
02057C00 0
02058C00 0
02059C00 0
02060C00 0
02061C00 0
02062C00 0
02063C00 0
02064C00 0
02065C00 0
02066C00 0
02067C00 0
02068C00 0
02069C00 0
02070C00 0
02071C00 0
02072C00 0
02073C00 0
02074C00 0
02075C00 0
02076C00 0
02077C00 0
02078C00 0
02079C00 0
02080C00 0
02081C00 0
02082C00 0
02083C00 0
02084C00 0
02085C00 0
02086C00 0
02087C00 0
02088C00 0
02089C00 0
02090C00 0
02091C00 0
02092C00 0
02093C00 0
02094C00 0
02095C00 0
02096C00 0
02097C00 0

X FROM SR02 AND CALL THE APPROPRIATE
X ISOLATE I:M FIELD = 12
X B CONTAINS STATUS REC 2
X P CONTAINS CONTENTS OF I:P FIELD
X JUMP TO TEST CONTENTS ROUTINE
X THIS ROUTINE WILL REMOVE THE I:M FIELD
X FROM SR02 AND CALL THE APPROPRIATE
X INDIRECT ADDRESSING ROUTINE
X ISOLATE I:M FIELD = 14
X B CONTAINS STATUS REC 2
X P CONTAINS CONTENTS OF I:P FIELD
X JUMP TO TEST CONTENTS ROUTINE
X THIS ROUTINE WILL REMOVE THE I:M FIELD
X FROM SR02 AND CALL THE APPROPRIATE
X INDIRECT ADDRESSING ROUTINE
X ISOLATE I:M FIELD = 16
X B CONTAINS STATUS REC 2
X P CONTAINS CONTENTS OF I:P FIELD
X JUMP TO TEST CONTENTS ROUTINE
X THIS ROUTINE ANALYSES THE I:P FIELD
X CONTENTS M = 0:112:3
X DIRECT ADDRESSING WITH INDEXING
X TEST IF M* = 2
X JUMP TO INDIRECT ADDR WITH INDEXING
X INDIRECT ADDR WITHOUT INDEXING
X THIS ROUTINE SAVES LOGIC UNIT REG.
X STORE B IN MIR
X SAVE RETURN IN B
X WRITE B INTO WORKSPACE
X WRITE A1 INTO WORKSPACE +1
X WRITE A2 INTO WORKSPACE + 2
X WRITE A3 INTO WORKSPACE + 3
X RESTORE ADDRESS
STEP

```











```

061F 4959 0000 003C 00F0
0620 4859 0000 904C 00F0
0621 4859 0000 0000 00F0
0622 4859 0000 8500 00F0
0623 4800 0000 0000 0020
0624 4800 0000 0000 00F0
0625 5808 0000 0000 00F0
0626 901C 0000 0170 004C
0627 4809 0000 8100 00FC
0628 900F 0000 0170 0020
0629 4809 0000 0000 00F0
062A 5805 0000 0076 00F0
062B 5FFC 0000 0000 0040
062C 4809 0000 0000 24F0
062D 4809 0000 801C 00FC
062E 0000 0000 0000 0010
062F 4809 0000 0900 00F0
0630 9009 0000 0A70 10F0
0631 9008 0000 0000 00F0
0632 2809 0000 0000 00FC
0633 4820 0000 0000 00FC

```

```

IFETCH:
0634 4809 0640 2020 00F0
0635 4809 2003 061C 00F0
0636 022C 0000 0000 00E0
0637 2F30 0000 0000 0060
0638 4809 0000 0000 00FC
0639 480F 0000 0000 00FC
063A 27EC 0000 0000 0060
063B 4809 0000 0B30 00F0
063C 0000 0000 0000 0020
063D 4809 0000 880F 00F0
063E 4809 0000 0000 00FC
063F 0000 0000 0000 0030
0640 50E0 0000 0000 0060
0641 4809 0000 0000 00FC
0642 4809 0001 2000 00FC
0643 0000 0000 0000 0020
0644 4809 0000 0000 00F0
0645 4809 0000 0000 00F0
0646 4809 0000 0000 00F0
0647 4829 0000 0000 00F0
0648 4809 0000 0000 00F0
0649 4809 0000 0000 00F0
064A 4809 0000 0000 00F0
064B 4809 0000 0000 00F0
064C 0000 0000 0000 0020
064D 4809 0000 4F00 00F0
064E 4809 0000 4000 00F0
064F 4820 0000 0000 00F0

```

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SET LCI
061 42
062 1
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X FLAG USED TO IDENTIFY THIS ROUTINE
X TRANSFER MIR TO P
X TRANSFER MIR TO A2
X SEND B TO THE ADDR
X CHECK IF PAGING SELECTED
X JUMP TO PAGING ROUTINE
X TEST IF BRACKPOINT SELECTED
X JUMP TO BKPT ANALYSIS ROUTINE
X REFERENCE MAR2
X PAR2 CONTAINS ADDRESS
X RESTORE MIR
X PERFORM WRITE INTO MEMORY
X CLEAR LCI
X THIS ROUTINE WILL FETCH AN INSTRUCTION
X AND TRACE ALL REGISTERS IF
X PRESELECTED VIA TRACE CONTROL CARD
X STORE RETURN ADDRESS
X READ IN SR #2
X SR # 2 TO THE ADDR
X TRACE IF TRUE
X JUMP TO REGISTER DUMPING ROUTINE
X ISOLATE ADDRESS IN PAR FIELD OF FSM
X INSERT ADDRESS INTO BR2
X PR2 IS FILLED FROM 2ND LEB OF SOURCE
X RETRIEVE INSTRUCTION AT ADDRESS IN BF2
X RESTORE RETURN ADDRESS
X ISOLATE PAR INTO A2
X TEST FOR UPPER MEMORY BOUNDARY
X A1 JUMP % NCHRAL INCREMENT
X CREATE 1024 IN B
X CLEAR PAR
X RESTORE B AND SET PAR TO 1024
X THIS ROUTINE WILL CALCULATE AN ACTUAL
X ADDRESS WHEN PASSED A PAGE NUMBER
X REFERENCE AND AN OFFSET IN THE BR2 REG.
X A1,A2,A3,AMPQR MUST BE SAVED TO EE USED?27700 D

```









U S AIR FORCE AIRCRAFT MAINTENANCE INSTRUCTIONS

02339100 0  
02340000 0  
02341000 0  
02342000 0  
02343000 0  
02344000 0  
02345000 0  
02346000 0  
02347000 0  
02348000 0  
02349000 0  
02350000 0  
02351000 0  
02352000 0  
02353000 0  
02354000 0  
02355000 0  
02356000 0  
02357000 0  
02358000 0  
02359000 0  
02360000 0  
02361000 0  
02362000 0  
02363000 0  
02364000 0  
02365000 0  
02366000 0  
02367000 0  
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02369000 0  
02370000 0  
02371000 0  
02372000 0  
02373000 0  
02374000 0  
02375000 0  
02376000 0  
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02396000 0  
02397000 0

\* A1 CONTAINS THE FSM  
\* A2 SERVES AS A TEMPORARY REGISTER  
\* P FOR RETURNS, ETC.  
\* P IS THE WORKING REGISTER  
\* A3 CONTAINS THE INSTRUCTION

067C 0630 087C 0000 0040  
067D 0630 087C 0000 0040  
067E 0630 087C 0000 0040  
067F 0660 0000 0000 0040  
0680 067C 0000 0000 0040  
0681 068C 0000 0000 0040  
0682 069C 0000 0000 0040  
0683 06A0 0000 0000 0040  
0684 06B0 0000 0000 0040  
0685 06C0 0000 0000 0040  
0686 06D0 0000 0000 0040  
0687 06E0 0000 0000 0040  
0688 06F0 0000 0000 0040  
0689 0000 0000 0000 0040  
068A 0010 0000 0000 0040  
068B 0020 0000 0000 0040  
068C 0030 0000 0000 0040  
068D 0040 0000 0000 0040  
068E 0050 0000 0000 0040  
068F 0060 0000 0000 0040  
0690 0070 0000 0000 0040  
0691 0080 0000 0000 0040  
0692 0090 0000 0000 0040  
0693 00A0 0000 0000 0040  
0694 00B0 0000 0000 0040  
0695 00C0 0000 0000 0040  
0696 00D0 0000 0000 0040  
0697 00E0 0000 0000 0040  
0698 00F0 0000 0000 0040  
0699 0000 0000 0000 0040  
069A 0010 0000 0000 0040  
069B 0020 0000 0000 0040  
069C 0030 0000 0000 0040  
069D 0040 0000 0000 0040  
069E 0050 0000 0000 0040  
069F 0060 0000 0000 0040  
06A0 0070 0000 0000 0040  
06A1 0080 0000 0000 0040  
06A2 0090 0000 0000 0040  
06A3 00A0 0000 0000 0040  
06A4 00B0 0000 0000 0040  
06A5 00C0 0000 0000 0040  
06A6 00D0 0000 0000 0040  
06A7 00E0 0000 0000 0040  
06A8 00F0 0000 0000 0040  
06A9 0000 0000 0000 0040  
06AA 0010 0000 0000 0040  
06AB 0020 0000 0000 0040  
06AC 0030 0000 0000 0040  
06AD 0040 0000 0000 0040  
06AE 0050 0000 0000 0040  
06AF 0060 0000 0000 0040  
06B0 0070 0000 0000 0040  
06B1 0080 0000 0000 0040







040C 1080 0000 0000 0040  
040D 1090 0000 0030 0040

0F012 - 1 = MPCR  
0F013 - 1 = MPCR

0F0101:

060E 4809 2C55 0B30 00FC  
060F 00F0 0000 0070 00FC  
0610 31CC 0FC3 0C00 0060  
  
061E 2F30 0000 0000 0060  
061F 4809 0C41 0C10 00F0  
0620 200C 0000 0030 0060  
0621 4809 00C0 0030 0060  
0622 80FC 0000 0000 0080  
0623 4809 E155 0E30 00FC  
0624 51CC 0000 0070 0060  
  
062E 2F50 0000 0000 0060  
062F 56E0 0000 0030 0060

0F0111:

065A 4809 2C55 0E30 00FC  
065B 00F0 0000 0030 00FC  
065C 51CC 0000 0000 0060  
  
065E 2F30 0000 0070 0060  
065F 4809 0C41 0C10 00FC  
0660 00C0 0000 0000 0030  
0661 60E0 0000 0070 0060  
0662 4809 0C40 0030 00F0  
0663 200C 0000 0000 0060  
0664 4809 EDC0 8B00 00FC  
0665 80F0 0000 0000 0080  
0666 4809 2C55 0E30 00FC  
0667 51CC 0000 0000 0060

0F0121:

066E 2F50 0000 0000 0060  
066F 56E0 0000 0030 0060  
  
0669 6330 00C0 0030 0060  
066A 4809 EDC1 1030 00FC  
066B 00F0 00C0 0030 00A0  
066C 4809 EC5C 1030 00FC  
066D 4809 00C0 0030 00F0  
066E 4809 EDC0 8A00 00FC  
066F 4809 C156 001C 00FC  
0700 4809 0F52 0000 00FC  
0701 600B 0000 0070 00FC  
0702 5670 0000 0000 0060  
0703 4809 EDC1 2C00 00FC  
0704 000C 0000 0000 0020  
0705 4809 C000 0000 00FC  
0706 4809 C000 0030 00FC  
0707 200C 0000 0000 0060

02439000 0  
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02461000 0  
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02500000 0  
02501000 0  
02502000 0  
02503000 0  
02504000 0  
02505000 0  
02506000 0  
02507000 0  
02508000 0  
02509000 0  
02510000 0  
02511000 0  
02512000 0  
02513000 0  
02514000 0  
02515000 0  
02516000 0  
02517000 0

X RR TYPE INSTRUCTION  
X CONTENTS OF R(CH) STORED INTO R(A)  
X SELECT LS 4 BITS OF B (\*P\* FIELD)  
X SELECT REGISTER STACK TO BE USED  
X ADDR OF GEN REG STACK RETURNED IN MAR2  
X PUT CONTENTS OF R(CH) IN B  
X CONTENTS OF P(CH) IN MIR  
X ARITHMETIC CC SETTING (CENTER WITH B)  
X OBTAIN \*A\* FIELD  
X SELECT REGISTER STACK TO BE USED  
X ADDR OF GEN REG STACK RETURNED IN PAR2  
X CONTENTS OF P(CH) INTO R(A)  
X OBTAIN \*A\* FIELD  
X ADDR OF GEN REG STACK RETURNED IN PAR2  
X CONTENTS OF P(CH) INTO R(A)  
X SET UP ADDRESS OF Y\* IN ER2  
X READ (Y\*) INTO B  
X (Y\*) IN MIR  
X ARITHMETIC CC SETTING (CENTER WITH B)  
X EXTRACT \*A\* FIELD  
X SELECT REGISTER STACK TO BE USED  
X ADDR OF GEN REG STACK RETURNED IN MAR2  
X WRITE OUT CONTENTS OF Y\* INTO R(A)  
X RR TYPE INSTRUCTION  
X (Y) INTO R(A) IF \*M\* = 0  
X (Y) (R(CH) = R(A) IF \*M\* = 0  
X GET CONTENTS OF Y1 FIELD  
X PREPARE A3 FOR STORAGE OF Y1 FIELD  
X CLEAR MIR, BR2  
X PLACE Y1 FIELD IN LS 4 BITS OF A2  
X PUT Y1 FIELD INTO MAR  
X CHECK IF \*M\* FIELD 0  
X SKIP  
X ANALYZE R(CH) AND RETURN VALUE IN MIR  
X ISOLATE Y INTO A2  
X PUT Y INTO A2 AND R(CH) INTO B  
X B, MIR CONTAINS FUTURE CONTENTS OF R(A)  
X ARITHMETIC CC SETTING (CENTER WITH B)













```

0765 119F 00C0 003C 004F
RPOS - 1 = MPCR
RNEG1
NOT B = B
E R = B
15 = SAR
COMP = 0
GMP = 0
GMP - 3 = SAR
15 = SAR
A2 - B = MIR; SET LC2
IF ADV THEN SET LC1
CARRY - 1 = CPGR
CHECKOV - 1 = CPGR
END02002 - 1 = MPCR
RPOS1
D L = B
COMP 1 = SAR
A2 + B = MIR
IF ADV THEN SET LC1
CARRY - 1 = CPGR
CHECKOV - 1 = CPGR
END02002+ASE
BHAR = A2
A2 AND B110 = MAR2; PMI
B R = B;MIR
16 = SAR
SETCCA - 1 = CPGR
COUTPUT - 1 = CPGR
OPCODE - 1 = MPCR
0F02004:
B L = A2+B;SAR
COMP 16;A2;SAR
A2 EOL B10;SAR
IF TRUE THEN SET LC1
OVB1T - 1 = CPGR
16 = SAR
- B R = B;MIR
IF ADV THEN SET LC1
CARRY - 1 = CPGR
SETCCA - 1 = CPGR
COUTPUT - 1 = CPGR
OPCODE - 1 = MPCR
0F02005:
ASE
BHAR L = BR1
COMP B = SAR
R L = A2
COMP 16 = SAR ; I = LIT
LIT OR BHAR = MAP2
FINDUP - 1 = CPGR
A2 EOL B = A2; B
IF TRUE THEN SET LC1
OVB1T - 1 = CPGR
- B = B
IF ADV THEN SET LC1
CARRY - 1 = CPGR
0766 4809 0C42 60C0 00FC
0767 4809 00C3 60C0 00FD
0768 300F 00C3 60C0 0010
0769 480F 00C1 60C0 00C0
0770 4809 0C40 00C0 00E0
0771 4809 0C40 00C0 00F0
0772 3000 00C0 00C0 0010
0773 4809 C05E 00C0 0010
0774 78C9 00C0 00C0 00F0
0775 1E70 00C0 00C0 0060
0776 4F10 00C0 00C0 0060
0777 4809 00C3 00C0 24F0
0778 4809 0F40 20C0 00F0
0779 4809 C0CE 00C0 00F0
0780 4809 C0C4 00C0 00F0
0781 4809 C0C4 80C0 0020
0782 2E00 00C0 00C0 0060
0783 2F50 00C0 00C0 0060
0784 56E0 00C0 00C0 0040
0785 4809 0C41 20C0 00E0
0786 4809 0812 00C0 00F0
0787 4809 0812 00C0 00FD
0788 1E70 00C3 00C0 0060
0789 20C0 C0C3 00C0 0060
0790 2F50 00C3 00C0 0060
0791 66EC 00C3 00C0 004C
0792 4809 00C0 00C0 24F0
0793 4809 0F41 00C0 00FD
0794 00C0 00C0 00C0 003C
0795 4809 0C41 20C0 00F0
0796 001C 00C0 00C0 0040
0797 2E10 2F50 00C0 0060
0798 4809 C0C3 20C0 0060
0799 4809 0812 00C0 00FD
0800 5020 00C3 00C0 0060
0801 4809 0C5E 00C0 00FC
0802 78C9 00C3 00C0 00FD
0803 1E70 00C3 00C0 0060

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02638000 0
02639000 0
02640000 0
02641000 0
02642000 0
02643000 0
02644000 0
02645000 0
02646000 0
02647000 0
02648000 0
02649000 0
02650000 0
02651000 0
02652000 0
02653000 0
02654000 0
02655000 0
02656000 0
02657000 0
02658000 0
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02696000 0
02697000 0

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X COMPLEMENT B (15)
X ISOLATE BIT 15 IN D
X CLEAN OUT B REGISTER
X PLACE BIT 15 IN BIT 16
X CHECK FOR CARRY
X OVERFLOW CHECK
X SHIF1 BIT P0E 15 OF RA+1 INTO BIT 16
X CHECK FOR CARRY
X CHECK FOR OVERFLOW
X SET UP RCA INTO MAR2
X RESULT (RCA) STORE INTO LNK OF B;MIR
X 2'S COMPLEMENT; TYPE RR
X A2+B HAVE (RCA) IN UHW; MAR2 = RA
X CHECK FOR MAX NEG. NUM.
X SET/CLEAR OVB1T
X TWO'S COMPLEMENT (RCA)
X CHECK FOR CARRY
X B = (RCA)
X TWO'S COMPLEMENT DOUBLE; TYPE RR
X (RA+RA+1); -> RA;RA+1
X REF PR2
X TEMP STORAGE OF R(CA)
X B = (RCA); MAR2 = RA
X (RA+1)
X B = (RA+1); MAR2 = RA + 1
X A2 = (RA;RA+1)
X TEST FOR MAX NEG NUM
X TWO'S COMPLEMENT OF (RCA);R(A+1)
X CHECK FOR CARRY

```









07C6 4809 2001 0820 00F0  
 07C7 4809 C40 0E30 00F0  
 07C8 78C9 00C0 0E90 00F0  
 07C9 1E7C 00C0 0E90 0060  
 07CA 4F1C 00C0 0C70 0060  
 07CB 4809 00C0 0D90 00F0  
 07CC 4809 0C40 8B30 00F0  
 07CD 00C0 00C0 0D90 0020  
 07CE 200C 00C0 0E70 0060  
 07CF 2F5F 00C0 0000 0060  
 07D0 66EC 00C0 0030 0040

0P02013:

07D1 4809 0C40 2E40 00F0  
 07D2 0020 00C0 00C0 0040  
 07D3 4849 2001 0E20 00F0  
 07D4 4809 CE5E 0030 00F0  
 07D5 78C9 00C0 0F00 00F0  
 07D6 1E7C 00C0 0E00 0060  
 07D7 4F10 00C0 0C70 0060  
 07D8 4809 00C0 0D90 00F0  
 07D9 4809 0C40 8B30 00F0  
 07DA 00C0 00C0 0D90 0020  
 07DB 2000 00C0 0E70 0060  
 07DC 2F50 00C0 0000 0060  
 07DD 66ED 00C0 0070 0040

0P021:

07DE 4809 2E55 0830 00F0  
 07DF 00F0 00C0 00C0 00E0  
 07E0 51CC 00C0 0000 0060  
 07E1 2F3C 00C0 0000 0060  
 07E2 482C 00C0 0070 0060  
 07E3 66EC 00C0 0000 0040

0P023:

07E4 570C 00C0 0000 0060  
 07E5 4820 00C0 0020 0060  
 07E6 66E0 00C0 0C70 0040

0P020E03:

07E7 5F9C 00C0 0000 0060  
 07E8 4809 C640 0040 00FC  
 07E9 118C 00C0 0030 00CC  
 07EA 4809 00C0 0000 00F0  
 07EB 4824 00C0 0030 00F0

0P03F:

07EC 11CC 00C0 0000 0040  
 07ED 300C 00C0 0C70 0040  
 07EE 3000 00C0 0E90 0040  
 07EF 11D0 C003 0C70 0040

0P030:

07F0 4809 2E56 2030 00F0  
 07F1 00FC 00C0 00C0 00E0  
 07F2 48C9 C640 0040 00CC  
 07F3 11E0 00C0 0030 00CC

02759C00 0  
 02760C00 0  
 02761C00 0  
 02762C00 0  
 02763C00 0  
 02764C00 0  
 02765C00 0  
 02766C00 0  
 02767C00 0  
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 02793C00 0  
 02794C00 0  
 02795C00 0  
 02796C00 0  
 02797C00 0  
 02798C00 0  
 02799C00 0  
 02800C00 0  
 02801C00 0  
 02802C00 0  
 02803C00 0  
 02804C00 0  
 02805C00 0  
 02806C00 0  
 02807C00 0  
 02808C00 0  
 02809C00 0  
 02810C00 0  
 02811C00 0  
 02812C00 0  
 02813C00 0  
 02814C00 0  
 02815C00 0  
 02816C00 0

%% DECREASE RA BY TWO TYPE RR  
 %% (RA) - 2 -> RA  
 %% B = (RA) MAR2 = RA  
 %%  
 %% CHECK FOR CARRY  
 %% CHECK FOR OVERFLOW  
 %% RESULT IN LHM OF B+MIR  
 %%  
 %% (RA) - 2 -> RA  
 %% B = (RA) MAR2 = RA  
 %%  
 %% (RA) IN LHM OF A2  
 %% LC2 IS SUBTRACTION FLAG  
 %%  
 %% SET/CLEAR CARRY BIT  
 %% CHECK FOR OVERFLOW  
 %% RESULT IN LHM OF B AND MIR  
 %%  
 %% (Y\*Y + I) -> RA+RA+I SET CC  
 %% ISOLATE IM: FIELD  
 %%  
 %% B = (RCH) = Y\*  
 %% CALL LOAD DOUBLE ROUTINE  
 %%  
 %% LOAD DOUBLE TYPE RX  
 %% (Y\*Y + I) -> RA+RA+I  
 %% B = Y  
 %% CALL LOAD DOUBLE ROUTINE  
 %%  
 %% THIS ROUTINE ANALYZES THE 03 OP CODE

%% XFCODE - I = CPCR  
 %% A2 + AMPCR = AMPCR  
 %% OP03F - J = AMPCR  
 %% STEP  
 %% EXEC  
 %%  
 %% OP030 - I = MPCR  
 %% FAULT - I = MPCR  
 %% FAULT - I = MPCR  
 %% OP033 - I = MPCR  
 %%  
 %% B AND LIT = A2  
 %% I5 = LIT  
 %% A2 + AMPCR = AMPCR  
 %% OP030H - I = AMPCR



```

0769 0769 0000 0000 0000
0770 0070 0000 0000 0000
0771 7800 0000 0000 0000
0772 4E50 0000 0000 0000
0773 4A24 0000 0000 0000
0774 0000 0000 0000 0000
0775 11F0 0000 0000 0000
0776 1200 0000 0000 0000
0777 1210 0000 0000 0000
0778 4E50 0000 0000 0000
0779 0000 0000 0000 0000
0780 0000 0000 0000 0000
0781 1230 0000 0000 0000
0782 1240 0000 0000 0000
0783 4809 E800 8B00 0000
0784 30F0 0000 0000 0000
0785 2E56 0000 0000 0000
0786 4809 48C1 0000 0000
0787 0000 0000 0000 0000
0788 4809 0E43 8B90 0000
0789 2000 0000 0000 0000
0790 2F50 0000 0000 0000
0791 5060 0000 0000 0000
0792 4809 E0C3 9000 0000
0793 30F0 0000 0000 0000
0794 4809 E155 0B30 0000
0795 5100 0000 0000 0000
0796 4809 0000 0000 0000
0797 4809 0E40 2070 0000
0798 2000 0000 0000 0000
0799 2F50 0000 0000 0000
0800 56EC 0000 0000 0000
0801 4809 E8C0 9020 0000
0802 30F0 0000 0000 0000
0803 4809 E155 0B30 0000
0804 5100 0000 0000 0000
0805 4809 0000 0000 0000
0806 4809 0E40 2070 0000
0807 2000 0000 0000 0000
0808 2F50 0000 0000 0000
0809 56EC 0000 0000 0000
0810 4809 E0C3 9000 0000
0811 30F0 0000 0000 0000
0812 4809 E155 0B30 0000
0813 5100 0000 0000 0000
0814 4809 0000 0000 0000
0815 4809 0E40 2070 0000
0816 2000 0000 0000 0000
0817 2F50 0000 0000 0000
0818 56EC 0000 0000 0000
0819 4809 E8C0 9020 0000
0820 30F0 0000 0000 0000
0821 4809 E155 0B30 0000
0822 5100 0000 0000 0000
0823 4809 0000 0000 0000
0824 4809 0E40 2070 0000
0825 2000 0000 0000 0000
0826 2F50 0000 0000 0000
0827 56EC 0000 0000 0000
0828 4809 E8C0 9020 0000
0829 30F0 0000 0000 0000
0830 4809 E155 0B30 0000
0831 5100 0000 0000 0000
0832 4809 0000 0000 0000
0833 4809 0E40 2070 0000
0834 2000 0000 0000 0000
0835 2F50 0000 0000 0000
0836 56EC 0000 0000 0000
0837 4809 E8C0 9020 0000
0838 30F0 0000 0000 0000
0839 4809 E155 0B30 0000
0840 5100 0000 0000 0000
0841 4809 0000 0000 0000
0842 4809 0E40 2070 0000
0843 2000 0000 0000 0000
0844 2F50 0000 0000 0000
0845 56EC 0000 0000 0000
0846 4809 E8C0 9020 0000
0847 30F0 0000 0000 0000
0848 4809 E155 0B30 0000
0849 5100 0000 0000 0000
0850 4809 0000 0000 0000
0851 4809 0E40 2070 0000
0852 2000 0000 0000 0000
0853 2F50 0000 0000 0000
0854 56EC 0000 0000 0000
0855 4809 E8C0 9020 0000
0856 30F0 0000 0000 0000
0857 4809 E155 0B30 0000
0858 5100 0000 0000 0000
0859 4809 0000 0000 0000
0860 4809 0E40 2070 0000
0861 2000 0000 0000 0000
0862 2F50 0000 0000 0000
0863 56EC 0000 0000 0000
0864 4809 E8C0 9020 0000
0865 30F0 0000 0000 0000
0866 4809 E155 0B30 0000
0867 5100 0000 0000 0000
0868 4809 0000 0000 0000
0869 4809 0E40 2070 0000
0870 2000 0000 0000 0000
0871 2F50 0000 0000 0000
0872 56EC 0000 0000 0000
0873 4809 E8C0 9020 0000
0874 30F0 0000 0000 0000
0875 4809 E155 0B30 0000
0876 5100 0000 0000 0000
0877 4809 0000 0000 0000
0878 4809 0E40 2070 0000
0879 2000 0000 0000 0000
0880 2F50 0000 0000 0000
0881 56EC 0000 0000 0000
0882 4809 E8C0 9020 0000
0883 30F0 0000 0000 0000
0884 4809 E155 0B30 0000
0885 5100 0000 0000 0000
0886 4809 0000 0000 0000
0887 4809 0E40 2070 0000
0888 2000 0000 0000 0000
0889 2F50 0000 0000 0000
0890 56EC 0000 0000 0000
0891 4809 E8C0 9020 0000
0892 30F0 0000 0000 0000
0893 4809 E155 0B30 0000
0894 5100 0000 0000 0000
0895 4809 0000 0000 0000
0896 4809 0E40 2070 0000
0897 2000 0000 0000 0000
0898 2F50 0000 0000 0000
0899 56EC 0000 0000 0000
0900 4809 E8C0 9020 0000
0901 30F0 0000 0000 0000
0902 4809 E155 0B30 0000
0903 5100 0000 0000 0000
0904 4809 0000 0000 0000
0905 4809 0E40 2070 0000
0906 2000 0000 0000 0000
0907 2F50 0000 0000 0000
0908 56EC 0000 0000 0000
0909 4809 E8C0 9020 0000
0910 30F0 0000 0000 0000
0911 4809 E155 0B30 0000
0912 5100 0000 0000 0000
0913 4809 0000 0000 0000
0914 4809 0E40 2070 0000
0915 2000 0000 0000 0000
0916 2F50 0000 0000 0000
0917 56EC 0000 0000 0000
0918 4809 E8C0 9020 0000
0919 30F0 0000 0000 0000
0920 4809 E155 0B30 0000
0921 5100 0000 0000 0000
0922 4809 0000 0000 0000
0923 4809 0E40 2070 0000
0924 2000 0000 0000 0000
0925 2F50 0000 0000 0000
0926 56EC 0000 0000 0000
0927 4809 E8C0 9020 0000
0928 30F0 0000 0000 0000
0929 4809 E155 0B30 0000
0930 5100 0000 0000 0000
0931 4809 0000 0000 0000
0932 4809 0E40 2070 0000
0933 2000 0000 0000 0000
0934 2F50 0000 0000 0000
0935 56EC 0000 0000 0000
0936 4809 E8C0 9020 0000
0937 30F0 0000 0000 0000
0938 4809 E155 0B30 0000
0939 5100 0000 0000 0000
0940 4809 0000 0000 0000
0941 4809 0E40 2070 0000
0942 2000 0000 0000 0000
0943 2F50 0000 0000 0000
0944 56EC 0000 0000 0000
0945 4809 E8C0 9020 0000
0946 30F0 0000 0000 0000
0947 4809 E155 0B30 0000
0948 5100 0000 0000 0000
0949 4809 0000 0000 0000
0950 4809 0E40 2070 0000
0951 2000 0000 0000 0000
0952 2F50 0000 0000 0000
0953 56EC 0000 0000 0000
0954 4809 E8C0 9020 0000
0955 30F0 0000 0000 0000
0956 4809 E155 0B30 0000
0957 5100 0000 0000 0000
0958 4809 0000 0000 0000
0959 4809 0E40 2070 0000
0960 2000 0000 0000 0000
0961 2F50 0000 0000 0000
0962 56EC 0000 0000 0000
0963 4809 E8C0 9020 0000
0964 30F0 0000 0000 0000
0965 4809 E155 0B30 0000
0966 5100 0000 0000 0000
0967 4809 0000 0000 0000
0968 4809 0E40 2070 0000
0969 2000 0000 0000 0000
0970 2F50 0000 0000 0000
0971 56EC 0000 0000 0000
0972 4809 E8C0 9020 0000
0973 30F0 0000 0000 0000
0974 4809 E155 0B30 0000
0975 5100 0000 0000 0000
0976 4809 0000 0000 0000
0977 4809 0E40 2070 0000
0978 2000 0000 0000 0000
0979 2F50 0000 0000 0000
0980 56EC 0000 0000 0000
0981 4809 E8C0 9020 0000
0982 30F0 0000 0000 0000
0983 4809 E155 0B30 0000
0984 5100 0000 0000 0000
0985 4809 0000 0000 0000
0986 4809 0E40 2070 0000
0987 2000 0000 0000 0000
0988 2F50 0000 0000 0000
0989 56EC 0000 0000 0000
0990 4809 E8C0 9020 0000
0991 30F0 0000 0000 0000
0992 4809 E155 0B30 0000
0993 5100 0000 0000 0000
0994 4809 0000 0000 0000
0995 4809 0E40 2070 0000
0996 2000 0000 0000 0000
0997 2F50 0000 0000 0000
0998 56EC 0000 0000 0000
0999 4809 E8C0 9020 0000
1000 30F0 0000 0000 0000

```

```

A2 GEO LIT
7 = LIT
IF TRUE THEN STEP ELSE SKIP
NOTIMP - 1 = MPCR
EXEC
X
X
X EXECUTIVE RETURN (P) + 1 -> RAJ HALT
X B = RAJ FIELD
X ISOLATE PAR INTO B INCREMENTED BY 1
X (P) + 1 INTO B AND MIR
X SET CONDITION CODE
X (P) + 1 -> RA
X STOP MACHINE EXECUTION
X STORE (SR1) INTO RA
X STORE (SR2) INTO RA
X RA = MAR2
X RA INTO A2
X D = SR2
X ISOLATE UYK2C SR2
X TRANSFER RA INTO MAR2
X (SR2) INTO RA
X
X LOAD P.J. (RKA)) INTO P

```



```

0823 4809 E000 9000 0000
0824 4050 0000 0000 0000
0825 4809 E156 0030 0000
0826 5100 0000 0030 0000
0827 2F30 0000 0030 0000
0828 4809 A000 C030 0000
0829 0000 0000 0030 0000
082A 4809 A001 4000 0000
082B 4809 AC5C 4030 0000
082C 56E0 0000 0030 C040

082D 4809 E000 9000 0000
082E 4050 0000 0000 0000
082F 4809 E156 0030 0000
0830 5100 0000 0030 0000
0831 2F30 0000 0030 0000
0832 4809 0C91 0090 0000
0833 0000 0000 0030 0000
0834 4809 2001 2000 0000
0835 307C 0000 0000 0000
0836 4809 2001 0000 C0F0
0837 0700 0000 C030 00A0
0838 4809 C05C 0030 C0F0
0839 4809 0C42 2000 C0F0
083A 4809 C056 0090 C0F0
083B 4809 C002 0030 C0F0
083C 4809 A056 2000 0000
083D 4809 C05C C000 0000
083E 4809 A0C1 4000 C0F0
083F 0000 0000 0030 C020
0840 4809 A0D0 C030 0000
0841 4809 A05C 4030 0000
0842 66EC C000 0030 C040

0843 4809 E000 9000 0000
0844 30E0 0000 0000 0000
0845 4809 E156 0030 0000
0846 5100 0000 0030 0000
0847 2F30 0000 0030 0000
0848 4809 0C91 0090 0000
0849 0000 0000 0030 0000
084A 022C 0000 0000 0000
084B 023C 0000 0000 0000
084C 4809 0C40 8030 0000
084D 0000 0000 0000 0020
084E 4809 0C41 0000 0000
084F 4809 C05C C000 C0F0
0850 2F50 0000 0030 C060
0851 56E0 0000 0030 C040

0852 5330 0000 0030 0000
0853 4809 0C91 0090 C0F0
0854 0000 0000 0000 00A0
0855 4809 EC5C 1000 0000

```

A3 M = A3

4 = SARI 15 = LIT  
A3 AND LIT = B  
REGSTACK - 1 = CPCR  
EINPUT - 1 = CPCR  
A1 R = A1  
16 = SAR  
A1 L = A1  
A1 OR B = A1  
OPCODE - 1 = MPCR

0P030065:

A3 R = A3  
4 = SARI 15 = LIT  
A1 AND LIT = B  
REGSTACK - 1 = CPCR  
EINPUT - 1 = CPCR  
B L = MIR 1 = CPCR  
COMP 16 = SAR  
LIT L = A2  
7 = LIT/ COMP 29 = SAR  
LIT L = B  
112 = LIT/ COMP 16 = SAR  
A2 OR B = B  
NOT R = A2, BHI  
A2 AND B = MIR  
NOT A2 = B  
A1 AND B = A2, BHI  
A2 OR B = B  
A1 L = A1  
COMP 16 = SAR  
A1 R = A1  
A1 OR B = A1  
OPCODE - 1 = MPCR

0P030061:

A3 R = A3  
4 = SARI 15 = LIT  
A3 AND LIT = B  
REGSTACK - 1 = CPCR  
EINPUT - 1 = CPCR  
B L = A2, BHI  
LIT L = A2, BHI  
STATUS2 = LIT  
EINPUT - 1 = CPCR  
B R = B  
16 = SAR  
B L = B  
A2 OR B = MIR  
EOUTPUT - 1 = CPCR  
OPCODE - 1 = MPCR

0P033:

IFETCH - 1 = CPCR  
B L = B  
COMP 16 = SAR 15 = LIT  
A3 OR B = A3

02879000 U  
02880000 D  
02881000 D  
02882000 D  
02883000 D  
02884000 D  
02885000 U  
02886000 D  
02887000 D  
02888000 U  
02889000 U  
02890000 D  
02891000 D  
02892000 C  
02893000 D  
02894000 U  
02895000 D  
02896000 D  
02897000 D  
02898000 U  
02899000 U  
02900000 U  
02901000 U  
02902000 U  
02903000 D  
02904000 D  
02905000 U  
02906000 U  
02907000 D  
02908000 D  
02909000 U  
02910000 U  
02911000 D  
02912000 U  
02913000 D  
02914000 D  
02915000 D  
02916000 D  
02917000 D  
02918000 U  
02919000 D  
02920000 D  
02921000 D  
02922000 U  
02923000 D  
02924000 D  
02925000 D  
02926000 D  
02927000 D  
02928000 D  
02929000 D  
02930000 D  
02931000 D  
02932000 D  
02933000 D  
02934000 D  
02935000 D  
02936000 D  
02937000 D

\* RA IN MAR2  
\* B = (R(A))  
\* ZERO PAR  
\* (R(A)) INTO P UPPER 16 BITS UNTOUCHED  
\* LOAD SRI ; (R(A)) INTO SRI  
\* RA IN MAR2  
\* B = (R(A))  
\* STORE (R(A)) IN UHW OF MIR  
\* CREATE BIT MASK FOR LOADER 106GLES  
\* LOWER MASK OF SRI  
\* CREATE MASK ONES IN UHW GF B  
\* MASK OFF (RA), STORE IN MIR  
\* MASK FOR A1 (PEM)  
\* MASK OFF SAVED PART OF A1 INTO A2  
\* CLEAR UHW OF A1  
\* RESTORE A1  
\* RESTORE A1 (ACTIVE PSM)  
\* UNTOUCHED  
\* (LOAD SR2) (R(A)) INTO SR2  
\* PA = MAR2  
\* B = (R(A))  
\* (R(A)) = A2  
\* B = (STATUS2)  
\* ISOLATE UPPER 16 BITS OF STATUS2  
\* NEW STATUS2 CREATED  
\* (R(A)) INTO STATUS2  
\* LOAD MULTIPLE, TYPE RX  
\* (Y \*\*\* Y + H - A + 1) INTO RA \*\*\* RH  
\* B = !Y: = Y  
\* STORE Y IN UHW OF A3































```

0988 130C 0009 0030 C040
0989 13CC 00C0 0080 C040
098A 3000 00C0 0030 C040
098B 1300 00C0 0000 C040

0F0701
0F070 0F070 - 1 = MPCR
0F071 - 1 = MPCR
FAULT - 1 = MPCR
0F073 - 1 = MPCR

R R = 0
R = SARI 15 = LIT
LIT AND B = 0
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B = A2
A3 AND LIT = B
15 = LIT
R = SAR
A2 R = A2
IF LIT THEN STEP ELSE SKIP X TEST BIT
TEST11 - 1 = MPCR
LIT EOL B = MPCR
IF TRUE THEN B010 C = B SKIP X SET 00 INTO CC LITS
R11 C = B
B = SAR
A1 AND B = A1
OPCODE - 1 = MPCR

LIT EOL B
IF TRUE THEN B101 C = B SKIP X SET 11 IN BOTH LC BITS
B10 C = B
A1 OR B = A1
OPCODE - 1 = MPCR

YES11:
LIT AND B = 0
15 = LIT
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B = A2
B L = BR2
COMP B = SAR
EYULIN - 1 = CPCR
A1 R = A1
16 = SAR
A1 L = A1
A1 OR B = A1
A2 + 1 = A2
A2 L = BR2
COMP B = SAR
ENULIN - 1 = CPCR
B L = HIR
COMP 16 = SAR
LIT L = A3
LIT B COMP 29 = SAR
112 = LIT COMP 16 = SAR
A3 OR B = B

098C 4809 0C40 8B00 C0FC
098D 40C0 00C0 0000 C0FC
098E 4809 2C55 0B30 C050
098F 51C0 00C0 0000 C060
0990 2F30 00C0 0000 C060
0991 4809 0C40 2070 C060
0992 4809 E155 0B70 C0F0
0993 00FC 00C0 00C0 00E0
0994 4809 0C40 007C 80F0
0995 4809 00C0 007C F0FC
0996 4809 00C0 00C0 00F0
0997 5800 00C0 007C 00F0
0998 13E0 00C0 007C 0040
0999 4809 2C52 0000 00F0
099A 5C19 4809 8P70 00FC
099B 4809 1813 8B00 00FC
099C 00C0 00C0 007C 001F
099D 4809 AC56 4000 00F0
099E 66EC 00C0 007C 0040

099F 4809 2C52 0000 00E0
09A0 5C19 18C1 8B00 00FC
09A1 4809 00C0 007C 00FC
09A2 00C0 00C0 007C 00FC
09A3 4809 AC5C 4000 00E0
09A4 66EF 00C0 0000 0040

09A5 4809 2C55 0B00 00F0
09A6 00C0 00C0 007C 00E0
09A7 51C0 00C0 007C 0060
09A8 2F30 00C0 007C 0060
09A9 4809 0C40 207C 00FC
09AA 4809 0C41 001C 00FC
09AB 00C0 00C0 007C 0030
09AC 50EC 00C0 00C0 006E
09AD 4809 40C0 0000 00FC
09AE 00C0 00C0 007C 0020
09AF 4809 40C1 4C00 00F0
09B0 4809 AC5C 4070 00FC
09B1 4809 00C0 2F70 00F0
09B2 4809 00C0 00C0 00F0
09B3 00C0 00C0 007C 0030
09B4 50E1 00C0 007C 0060
09B5 4809 0C41 0C9C 00E0
09B6 00C0 00C0 008C 0020
09B7 407C 00C0 007C 00FC
09B8 4809 20C1 0000 00FC
09B9 4809 20C1 0000 00FC
09BA 0700 00C0 0030 0040
09BB 4809 EC5C 0B00 00E0

```

```

03259600 0
03360600 0
03361600 0
03302600 0
03303600 0
03304600 0
03305600 0
03366600 0
03307600 0
03368600 0
03319600 0
03311600 0
03312600 0
03313600 0
03314600 0
03315600 0
03316600 0
03317600 0
03318600 0
03319600 0
03320600 0
03321600 0
03322600 0
03323600 0
03324600 0
03325600 0
03326600 0
03327600 0
03328600 0
03329600 0
03330600 0
03331600 0
03332600 0
03333600 0
03334600 0
03335600 0
03336600 0
03337600 0
03338600 0
03339600 0
03340600 0
03341600 0
03342600 0
03343600 0
03344600 0
03345600 0
03346600 0
03347600 0
03348600 0
03349600 0
03350600 0
03351600 0
03352600 0
03353600 0
03354600 0
03355600 0
03356600 0
03357600 0

X 09A1 COMPARE BIT1 TEST BIT H OF RA FCR
X ZERO
X ISOLATE INH FIELD
X SHIFT COMPARE BIT TO LS POSITION
X BIT POSITION 15?
X SET 11 IN BOTH LC BITS
X SET 1 INTO LS BIT OF CC
X SET 1 OR 11 INTO CC BIT
X LPI1 LOAD_PSW (INDIRECT)
X (Y*,Y**1,Y**2) -> P*,SRI,SRI2
X RM = MAR2
X E = (R(M)) = Y*
X STORE B IN A2
X Y* = BR2 OR Y = ER2
X B = (Y*) OR (Y)
X PAR = (Y) OR (Y*)
X NEXT SEQ Y OR Y*
X (Y**1) OR (Y*1) = B
X STORE B INTO UNW OF HIR
X CREATE BIT MASK FOR LOADLR TOGGLELS
X STORE MASK FOR LOWER SRI INTO B
X STORE MASK FOR LOWER SRI INTO B
X CREATE FULL WORD MASK OF 11S

```



```

0900 4809 0C42 1000 00F0  X MASK FOR (RA)
0901 4809 EC56 0650 00F0  X MASK FOR (RA), STORE IN RIR
0902 4809 0E02 0E20 09F0  X MASK FOR A1 (PSW)
0903 4809 E902 0E20 09F0  X MASK OFF SAVED PART OF A1 INTO A2
0904 4809 AE56 1000 00F0  X CREATE NEW A1 VALUE FROM (RCA)
0905 4809 EC56 0650 00F0  X CLEAR UNW OF A1
0906 4809 0E02 0E20 09F0  X RESTORE A1
0907 4809 0E02 0E20 09F0  X NEXT SEQ Y OR Y=
0908 4809 AE56 1000 00F0  X (Y+2) OR (Y+2) = B
0909 4809 EC56 0650 00F0  X SR2 = HAR2
0910 4809 0E02 0E20 09F0  X B = (STATUS2)
0911 4809 AE56 1000 00F0  X ISOLATE UPPER 16 BITS OF STATUS2
0912 4809 EC56 0650 00F0  X CREATE NEW STATUS?
0913 4809 0E02 0E20 09F0  X LPJ LOAD PSW
0914 4809 AE56 1000 00F0  X (Y+1+Y+2) -> P;SR1;SR2
0915 4809 EC56 0650 00F0  X B = Y
0916 4809 0E02 0E20 09F0  X
0917 4809 AE56 1000 00F0  X LOGICAL RIGHT SHIFT
0918 4809 EC56 0650 00F0  X RETURNS *F= IN A2
0919 4809 0E02 0E20 09F0  X
0920 4809 AE56 1000 00F0  X
0921 4809 EC56 0650 00F0  X
0922 4809 0E02 0E20 09F0  X
0923 4809 AE56 1000 00F0  X
0924 4809 EC56 0650 00F0  X
0925 4809 0E02 0E20 09F0  X
0926 4809 AE56 1000 00F0  X
0927 4809 EC56 0650 00F0  X
0928 4809 0E02 0E20 09F0  X
0929 4809 AE56 1000 00F0  X
0930 4809 EC56 0650 00F0  X
0931 4809 0E02 0E20 09F0  X
0932 4809 AE56 1000 00F0  X
0933 4809 EC56 0650 00F0  X
0934 4809 0E02 0E20 09F0  X
0935 4809 AE56 1000 00F0  X
0936 4809 EC56 0650 00F0  X
0937 4809 0E02 0E20 09F0  X
0938 4809 AE56 1000 00F0  X
0939 4809 EC56 0650 00F0  X
0940 4809 0E02 0E20 09F0  X
0941 4809 AE56 1000 00F0  X
0942 4809 EC56 0650 00F0  X
0943 4809 0E02 0E20 09F0  X
0944 4809 AE56 1000 00F0  X
0945 4809 EC56 0650 00F0  X
0946 4809 0E02 0E20 09F0  X
0947 4809 AE56 1000 00F0  X
0948 4809 EC56 0650 00F0  X
0949 4809 0E02 0E20 09F0  X
0950 4809 AE56 1000 00F0  X
0951 4809 EC56 0650 00F0  X
0952 4809 0E02 0E20 09F0  X
0953 4809 AE56 1000 00F0  X
0954 4809 EC56 0650 00F0  X
0955 4809 0E02 0E20 09F0  X
0956 4809 AE56 1000 00F0  X
0957 4809 EC56 0650 00F0  X
0958 4809 0E02 0E20 09F0  X
0959 4809 AE56 1000 00F0  X
0960 4809 EC56 0650 00F0  X
0961 4809 0E02 0E20 09F0  X
0962 4809 AE56 1000 00F0  X
0963 4809 EC56 0650 00F0  X
0964 4809 0E02 0E20 09F0  X
0965 4809 AE56 1000 00F0  X
0966 4809 EC56 0650 00F0  X
0967 4809 0E02 0E20 09F0  X
0968 4809 AE56 1000 00F0  X
0969 4809 EC56 0650 00F0  X
0970 4809 0E02 0E20 09F0  X
0971 4809 AE56 1000 00F0  X
0972 4809 EC56 0650 00F0  X
0973 4809 0E02 0E20 09F0  X
0974 4809 AE56 1000 00F0  X
0975 4809 EC56 0650 00F0  X
0976 4809 0E02 0E20 09F0  X
0977 4809 AE56 1000 00F0  X
0978 4809 EC56 0650 00F0  X
0979 4809 0E02 0E20 09F0  X
0980 4809 AE56 1000 00F0  X
0981 4809 EC56 0650 00F0  X
0982 4809 0E02 0E20 09F0  X
0983 4809 AE56 1000 00F0  X
0984 4809 EC56 0650 00F0  X
0985 4809 0E02 0E20 09F0  X
0986 4809 AE56 1000 00F0  X
0987 4809 EC56 0650 00F0  X
0988 4809 0E02 0E20 09F0  X
0989 4809 AE56 1000 00F0  X
0990 4809 EC56 0650 00F0  X
0991 4809 0E02 0E20 09F0  X
0992 4809 AE56 1000 00F0  X
0993 4809 EC56 0650 00F0  X
0994 4809 0E02 0E20 09F0  X
0995 4809 AE56 1000 00F0  X
0996 4809 EC56 0650 00F0  X
0997 4809 0E02 0E20 09F0  X
0998 4809 AE56 1000 00F0  X
0999 4809 EC56 0650 00F0  X

```

```

NOT D = A3, BHI
A3 AND B = MIR
NOT A3 = 0
A1 AND B = A3, BHI
A3 OR D = B
A1 L = A1
CDHP 16 = SAR
A1 R = A1
A1 OR P = A1
A2 + 1 = A2
A2 L = BR2
COMP B = SAR
EOLIN - 1 = CPCR
B = A2
LII = HAR2
STATUS2 = LIT
INPUT - 1 = CPCR
L R = B
B L = SR
A2 OR B = MIR
EDUTPUT - 1 = CPCR
OPCODE - 1 = MPCR

```

```

0P073:
RKHFIELD - 1 = CPCR
LPSW - 1 = MPCR

```

```

OPCODE10:
XFCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP10F - 1 = AMPCR
STEP
EXEC

```

```

OP10F:
OP100 - 1 = MPCR
FAULT - 1 = MPCR
OP102 - 1 = MPCR
OP103 - 1 = MPCR

```

```

OP100:
CONTENISRM - 1 = CPCR
E = MIR
A3 = B
CONTENISRA - 1 = CPCR
B = A3, BHI
B = SAR
A3 R = MIR, B
SETCCA - 1 = CPCR
EDUTPUT - 1 = CPCR
OPCODE - 1 = MPCR

```

```

OP102:
X PK TYPE LOGICAL RIGHT SINGLE SHIFT

```



```

09E8 6330 0000 0000 0060
09E9 4809 0640 0030 00F0
09EA 4809 E156 0830 C0E0
09EB 00F0 0000 00C0 00E0
09EC 4809 0C52 00C0 00F0
09ED 6C19 C000 0800 00F0
09EE 238C 0040 2000 C06C
09EF 4809 0C50 0000 00F0
09F0 4809 0C40 0C40 00F0
09F1 4809 EC00 0800 C0F0
09F2 228C 09C0 0000 006C
09F3 4809 0C40 1030 00F0
09F4 4809 0E00 0030 00F0
09F5 4809 E0C0 0830 C0F0
09F6 2F50 0000 00C0 0060
09F7 200C 0000 0030 C060
09F8 58E0 0800 0030 0040

0PF03:
0CF9 4849 08C0 0030 C060
0CFE 5700 07C0 0030 006C
0CFB 4809 0C41 00C0 0030
0CF8 0000 0000 00C0 0030
0CFD 4809 0F40 0070 00F0
0CFE 50EC 00C0 0000 0060
09FF 4809 0C40 0C50 00F0
0A00 4809 E000 E07C C0F0
0A01 228C 0800 0070 C060
0A02 4809 2E57 100C C0F0
0A03 0FFC 0000 0000 00BC
0A04 380B 0800 0000 C0F0
0A05 143C 0000 0030 0040
0A06 4809 0C41 0000 00F0
0A07 0000 0000 0070 0010
0A08 4809 0C40 0800 00F0
0A09 4809 E000 7000 001C
0A0A 4809 EC00 0030 001C
0A0B 4809 EC50 0030 00F0
0A0C 4809 EC50 0030 00F0
0A0D 1440 0000 0030 0040

LS1C3:
0A0E 4809 0C40 0800 40F0
0A0F 0000 00C0 0030 001C
0A10 4809 0C41 0830 40FC
0A11 4809 E000 7000 00F0
0A12 4809 EC50 0030 00F0
0A13 4809 0000 0070 20F0
0A14 4809 0F40 0010 00F0
0A15 51EC 0800 C000 0060
0A16 56E0 C0C0 0C00 004C

OPCODE11:
0A17 5F90 0000 0070 C060
0A18 4809 C640 0030 00F0
0A19 145C 00C0 0070 00C0

SHIFT (RCA) MUSHI 1 BITS 0-5 REAVIS
ZERO FILL AND SET CC
Y INTO B
ISOLATE *M* FIELD
(RCA) INTO B
TRANSFER (RCA) INTO A2
Y INTO MIR
INSTRUCTION INTO B
(RCA) INTO B
(RCA) INTO A3
YCO-5) INTO SAR
PERFORM SHIFT
SET APPROPRIATE CONDITION BITS
RX TYPE EYIF STORE
(RCA) BITS 7) INTO Y BYTE
LC2 USE AS A BYTE OPERATION FLAG
Y ADDR INTO B
Y INTO BE2
STORE Y
(Y) INTO B
(Y) INTO MIR
(RCA) INTO B
RESTORE INSTRUCTION INTO B
(RCA) INTO B
LIT AND B = A3, BHI
255 = LIT) COMP 8 = SAR
(Y) INTO B
IF LC2 THEN STEP ELSE SKIP
IF LC2 SET, PUT BYTE INTO
LS103 - 1 = MPCCR
B L = B, CSAR
COMP 24 = SAR
A3 R = A3, CSAR
B = SAR
B = A3
A3 DR B = MIR
CNT103 - 1 = MPCCR
B R = B, CSAR
B = SAR, CSAR
B L = B, CSAR
A3 DR B = MIR
CNT103: ASR
EVAR = BR2
EHULOUT - 1 = MPCCR
OPCODE - 1 = MPCCR

R(AX) - BITS 0-7 INTO 2ND LS BYTE
IN A3
MIR CONTAINS NEW (Y)
USED AS A WORD
(RCA) BITS 0-7 INTO LS EYIE OF A3
CLEAR LS BYTE OF B
(RCA) BITS 0-7 INTO LS EYIE OF A3
MIR CONTAINS NEW (Y)
REFERENCE BR1
Y INTO BR2
WRITE INTO R(A)
RIGHT SHIFT AND STORE
R = F INTO A2

```





0A14 4809 0000 0030 0060  
0A10 4824 0000 0030 0060

STEP  
EXEC

OP1101 - 1 = MPCR  
OP1111 - 1 = MPCR  
OP1121 - 1 = MPCR  
OP1131 - 1 = MPCR

OP1101

CONTENTS - 1 = CPCR  
B = MIR  
A3 = B  
CONTENTS - 1 = CPCR  
B = A3, BHI  
A3 C = A3, CSAR  
15 = SAR  
IF LST THEN SET LCI  
A3 C = A3  
B = A2  
ROT 0 = B  
Z L = B  
16 = SAR  
IF LCI THEN A3 OR B = A3  
A2 = SAR  
A3 R = B  
COMP 16 = SAR  
D R = B, MIR  
EQUIPUT - 1 = CPCR  
SETCCA - 1 = CPCR  
OPCODE - 1 = MPCR

OP1111

CONTENTS - 1 = CPCR  
B = MIR  
CONTENTS - 1 = CPCR  
B L = BR2  
COMP 0 = SAR  
EMULOUT - 1 = CPCR  
OPCODE - 1 = MPCR

OP1121

LIT AND B = E  
15 = LIT  
B EOL 0  
IF TRUE THEN SKIF  
CONTENTS - 1 = CPCR  
B L = B  
COMP 16 = SAR  
A3 OR 0 = A3  
IFEITCH - 1 = CPCR

0A3E 4809 2C56 0070 00E0  
0A3F 00F0 0000 0070 00E0  
0A40 4809 0C52 0070 00E0  
0A41 6819 0000 0000 00F0  
0A42 2380 0000 0070 00E0  
0A43 4809 0C41 0070 00E0  
0A44 0C00 00C0 0070 00E0  
0A45 4809 EC5C 1000 00F0  
0A46 633C 0000 0000 0060

03478000 0  
03479000 0  
03480000 0  
03481000 0  
03482000 0  
03483000 0  
03484000 0  
03485000 0  
03486000 0  
03487000 0  
03488000 0  
03489000 0  
03490000 0  
03491000 0  
03492000 0  
03493000 0  
03494000 0  
03495000 0  
03496000 0  
03497000 0  
03498000 0  
03499000 0  
03500000 0  
03501000 0  
03502000 0  
03503000 0  
03504000 0  
03505000 0  
03506000 0  
03507000 0  
03508000 0  
03509000 0  
03510000 0  
03511000 0  
03512000 0  
03513000 0  
03514000 0  
03515000 0  
03516000 0  
03517000 0  
03518000 0  
03519000 0  
03520000 0  
03521000 0  
03522000 0  
03523000 0  
03524000 0  
03525000 0  
03526000 0  
03527000 0  
03528000 0  
03529000 0  
03530000 0  
03531000 0  
03532000 0  
03533000 0  
03534000 0  
03535000 0  
03536000 0  
03537000 0







0A76 51C0 0F43 0030 006C  
 0A77 4809 0F43 0070 00F0  
 0A78 0000 0000 0000 0030  
 0A79 2F30 0070 0000 0060  
 0A7A 4809 0C41 2070 00F0  
 0A7B 0010 0000 0000 004C  
 0A7C 4809 2F5C 0010 00F0  
 0A7D 2F30 0070 0000 006C  
 0A7E 4809 0C5C 2050 00F0  
 0A7F 4809 0E15 0030 00F0  
 0A80 0070 0000 0000 00CC  
 0A81 51C0 0000 0000 0060  
 0A82 0000 0000 0000 0000  
 0A83 4809 0C40 0070 00F0  
 0A84 4809 0C00 4870 00F0  
 0A85 2000 0000 0000 0060  
 0A86 4809 0000 0000 00F0  
 0A87 4809 0F43 0010 00F0  
 0A88 0000 0F7C 0070 0010  
 0A89 4609 0C00 8030 00F0  
 0A8A 0000 0000 0000 0020  
 0A8B 2F5C 0000 0C70 0060  
 0A8C 4809 0061 2030 00F0  
 0A8D 0010 0000 0000 004C  
 0A8E 4809 0C00 8030 00F0  
 0A8F 4809 2F5C 0010 00F0  
 0A90 2F5C 0070 0030 0060  
 0A91 660E 0000 0000 0040

0P121)

0A92 2280 00C3 0070 0060  
 0A93 4809 0C43 0030 00F0  
 0A94 238C 0003 0030 0060  
 0A95 4809 0C41 0F10 00F0  
 0A96 0000 0000 0000 0030  
 0A97 4809 0F12 0000 0060  
 0A98 4809 0C00 9000 00F0  
 0A9A 0C00 0000 0000 0040  
 0A9B 4809 0C0C 0010 00F0  
 0A9C 2F3C 0000 0000 0060  
 0A9D 4809 0C49 1000 00F0  
 0A9E 4809 0000 0000 00F0  
 0A9F 4809 0000 0000 00F0  
 0AA0 4809 0C41 0010 00F0  
 0AA1 0000 0000 0000 0030  
 0AA2 610C 0000 0C70 0060  
 0AA3 660E 0000 0000 0040

0P122)

0AA4 633C 0000 0000 0060  
 0AA5 4809 0C41 0030 00F0  
 0AA6 0000 0000 0000 004C  
 0AA7 4809 0C5C 1000 00F0  
 0AA8 4809 0E15 0000 00F0

REUSIACK - 1 = CPCR  
 BMAR L = BR1  
 COMP B = SAR  
 INPUT - 1 = CPCR  
 B L = A2  
 COMP 16 = SARJ 1 = LIT  
 LIT OR BHAR = MAR2  
 INPUT - 1 = CPCR  
 A2 OR B = A2  
 A3 AND LIT = B  
 A3 = LIT  
 REGSTACK - 1 = CPCR  
 INPUT - 1 = CPCR  
 B SAR - 1 = CPCR  
 A2 R SAR A2-BJ SET LCI  
 SETCCA - 1 = CPCR  
 ASR  
 BMAR R = MAR2  
 B = SAR  
 A2 R = MIR  
 16 = SAR  
 EINPUT - 1 = CPCR  
 A2 L = A2  
 COMP 16 = SARJ 1 = LIT  
 LIT OR BHAR = MAR2  
 INPUT - 1 = CPCR  
 OPCODE - 1 = MPCR  
 CONTENTSRA - 1 = UPCR  
 B = MIR  
 CONTENTSRM - 1 = CPCR  
 COMP B = SAR  
 EMLOUT - 1 = CPCR  
 BQAR + 1 = MIR  
 A2 = SARJ CSAR  
 A3 OR = MAR2  
 EINPUT - 1 = CPCR  
 B = A3  
 BHI  
 A3 = MIR  
 B L = BR2  
 COMP B = SAR  
 EMLOUT - 1 = CPCR  
 OPCODE - 1 = MPCR  
 X SAVE R(A)  
 X (R(A)) INTO B  
 X TEMP STORAGE OF (R(A))  
 X (R(A+1))  
 X (R(A+1)) INTO B  
 X A2 = (R(A))/(R(A+1))  
 X ISOLATE \*H\* FIELD  
 X (R(B)) INTO MAR2  
 X (R(C)) INTO P  
 X (R(C)) INTO P INTO SAR  
 X (R(C)) INTO P INTO SAR  
 X SET LINE CONDITION BITS  
 X REFERENCE BR1  
 X ADDR OF R(A) INTO MAR2  
 X (R(A)) INTO MIR  
 X WRITE OUT SHIFTD (R(A))  
 02621100 D  
 03621100 D  
 03623400 C  
 03624600 C  
 03625000 D  
 03626600 D  
 03627000 D  
 03628000 D  
 03629000 C  
 03630000 C  
 03621000 C  
 03633000 D  
 02634000 D  
 02635000 D  
 02636000 C  
 03637000 D  
 02638000 D  
 03640000 C  
 03641000 D  
 03642000 C  
 03643000 D  
 03644000 D  
 02645000 D  
 03646000 D  
 03647000 D  
 03648000 D  
 03649000 D  
 02650000 C  
 03651000 D  
 03652000 C  
 03653000 D  
 03654000 D  
 03655000 D  
 02656000 D  
 03657000 D  
 X RI TYPE ? STORE DOUBLE  
 X (R(A)/R(A+1)) INTO Y\*, Y\*\*  
 X (R(A)) INTO B, R(A) INTO MS WORD A3  
 X TEMP STORAGE FOR (R(A))  
 X (R(P)) INTO B  
 X (R(A)) INTO Y\*  
 X TEMP HOLDER FOR Y\* + 1  
 X (R(A+1)) INTO B  
 X (R(A+1)) INTO B  
 X TEMP STORAGE OF (R(A))  
 X ADDR OF Y\* + 1  
 X  
 X RK TYPE LOGICAL RIGHT DOUBLE SHIFT  
 X SHIFT (R(A), R(A+1)) RIGHT Y(0-5)  
 X ZEROFILL AND SET CC  
 X \*Y\* INTO B  
 X A3 HOLDS \*Y\*/INSTRUCTION  
 X ISOLATE \*H\* FIELD









```

OPCODE13:
0AE1 5F90 0800 0000 0060
0AE2 4809 C640 0030 C0F0
0AE3 14FC 0C00 00C0 0040
0AE4 4809 00C0 0030 00F0
0AE5 4824 0000 0030 00F0

04E6 1500 0000 0000 0040
04E7 3000 0000 0070 0040
CAE8 151C 0000 0030 0040
CAE9 157C 0000 0030 0040

04EA 4809 0C40 0830 00E0
04EB 80FC 00C0 0070 0080
04EC 4809 2C56 080C C0F0
CAED 51CC 00C0 0070 0060
04EE 2F30 0000 0030 0060
04EF 4809 0041 2030 0060
04F0 0010 0093 0000 C0A0
04F1 4809 0F41 0020 00F0
04F2 0000 0093 0000 C030
04F3 4809 2F5C 001C 00F0
04F4 2F30 00C0 000C C060
04F5 4809 0C5C 2070 00F0
CAFE 4809 0000 0030 C0FC
04F7 4409 00C0 0070 00F0
04F8 4809 0E15 0830 00F0
04F9 00F0 0000 000C 00E0
04FA 51CC 00C0 0070 C060
04FB 2F30 00C0 0030 0060
04FC 4809 0040 0030 80F0
04FD 43C9 0000 0000 0060
04FE 200C 0000 0000 C060
04FF 0010 0013 000C 00F0
0500 4809 0000 0000 00F0
0501 4809 C25C 2070 20F0
0502 4809 0F43 801C 00F0
CE03 0000 00C0 0030 0040
CE04 4809 C0F0 8030 C0F0
0505 0000 0000 0000 C020
0506 2F50 00C0 0030 0060
0507 4809 C001 2030 00F0
0508 001C 0093 000C 004C
0509 4809 C0C0 8830 00F0
050A 4809 2F5C 001C 00F0
050B 2F50 00C0 0070 0060
050C 66E0 00C0 0000 0040

0500 4809 2C56 0830 00F0

OP13F:
0F13F1 0F130 - 1 = MPCR
FAULT - 1 = MPCR
0F132 - 1 = MPCR
0F133 - 1 = MPCR

OP130:
B R = B
W = SAR, 15 = LIT
LIT AND B = E
REGSTACK - 1 = CPCR
FINPUT - 1 = CPCR
E L = A2
COMP 16 = SAR, 1 = LIT
BMAR L = BR, 1
BMAR L = SAR
LIT OR BMAR = MAR2
FINPUT - 1 = CPCR
A2 OR B = A2
IF MST THEN SET IC2
A3 AND LIT = B
15 = LIT
REGSTACK - 1 = CPCR
FINPUT - 1 = CPCR
B = SAR
A2 R = A2, B J SET LC1
SEICCA - 1 = CPCR
IF LC2 THEN PIII L = B J SKIP
A2 OR B = A2 J ASR
BMAR R = MAR2
B = SAR
A2 R = MAR
15 = SAR
OUTPUT - 1 = CPCR
A2 L = A2
COMP 16 = SAR, 1 = LIT
A2 R = MIR, B
LIT OR BMAR = MAR2
OUTPUT - 1 = CPCR
OPCODE - 1 = MPCR

LIT AND B = B

```

```

% SHIFT
% *F INTO A2
% OR TYPE ALG RIGHT DOUBLE SHIFT
% SHIFT ((R(A)),R(A+1)) RIGHT R(H) (0-5)
% SIGN FILL AND SET CC
% ISOLATE *A* FIELD
% ADDR OF R(A) INTO MAR2
% R(A) INTO B
% TEMP STORAGE OF R(A)
% TEMP STORAGE OF R(A)
% R(A+1) INTO MAR2
% R(A+1) INTO B
% A2 = (R(A))/(R(A+1))
% ISOLATE *M*
% R(H) INTO E
% R(H) (0-5) INTO SAR
% A2 HAS RIGHT SHIFTED (R(A))/(R(A+1))
% SET CONDITION BITS
% SKIP
% ADDR OF R(A) INTO MAR2
% R(A) INTO MIR
% WRITE OUT SHIFTED (R(A))
% SHIFTED (R(A+1)) INTO MIR
% R(A+1)
% PK TYPE ALG RIGHT DOUBLE SHIFT
% SHIFT (R(A),R(A+1)) RIGHT Y(0-5)
% SIGN FILL AND SET CC

```







```

0846 51CC 0000 0000 0060
0847 2F3C 0000 0000 0060
0848 4809 0F46 0F1C 00F0
0849 4809 00C0 9000 00F0
084A 0000 0000 0070 0020
084B 4809 00C0 1000 00F0
084C 4809 00C0 1000 00F0
084D 4809 0F40 0090 20FC
084E 4809 0F43 0010 00F0
084F 51EC 0000 0070 0060
0850 4809 0F46 0010 00F0
0851 4809 0F41 0020 00FC
0852 0000 0000 0030 0030
0853 4809 00C1 0000 00F0
0854 0000 0000 0000 0020
0855 4809 0040 1000 00F0
0856 4809 0F46 0000 00F0
0857 0100 0000 0000 00E0
0858 4809 00C0 0070 00F0
0859 4809 0000 0000 00FC
085A 4809 0000 0000 004C
085B 56CC 0000 0000 0040

085C 5F9C 0000 0000 0060
085D 4809 0040 0000 00FC
085E 153C 0000 0000 00C0
085F 4809 00C0 0070 00F0
0860 4824 0000 0000 00F0

0861 1540 0000 0000 0040
0862 3000 0000 0000 004C
0863 1550 0000 0000 0040
0864 156C 0000 0000 004C

0865 2380 0000 0000 0060
0866 4809 0040 0000 00FC
0867 4809 00C0 0000 00FC
0868 4809 0040 2000 0060
0869 4809 0040 2000 0060
086A 4809 2050 0000 00FC
086B 4809 0000 0000 00FC
086C 4809 2050 0000 00FC
086D 0100 0000 0000 00E0
086E 7819 0000 0000 00F0
086F 1570 0000 0070 0040
0870 4809 00CE 0000 00FC
0871 4809 00C1 2000 00FC
0872 4809 0000 9000 00FC
0873 0000 0000 0000 0020
0874 4809 0001 2000 00FC
0875 4809 0000 8800 00FC
0876 4809 0002 0000 00FC
0877 63C9 0000 0000 00FC

0878 0000 0000 0000 0000
0879 0000 0000 0000 0000
087A 0000 0000 0000 0000
087B 0000 0000 0000 0000
087C 0000 0000 0000 0000
087D 0000 0000 0000 0000
087E 0000 0000 0000 0000
087F 0000 0000 0000 0000
0880 0000 0000 0000 0000
0881 0000 0000 0000 0000
0882 0000 0000 0000 0000
0883 0000 0000 0000 0000
0884 0000 0000 0000 0000
0885 0000 0000 0000 0000
0886 0000 0000 0000 0000
0887 0000 0000 0000 0000
0888 0000 0000 0000 0000
0889 0000 0000 0000 0000
088A 0000 0000 0000 0000
088B 0000 0000 0000 0000
088C 0000 0000 0000 0000
088D 0000 0000 0000 0000
088E 0000 0000 0000 0000
088F 0000 0000 0000 0000
0890 0000 0000 0000 0000
0891 0000 0000 0000 0000
0892 0000 0000 0000 0000
0893 0000 0000 0000 0000
0894 0000 0000 0000 0000
0895 0000 0000 0000 0000
0896 0000 0000 0000 0000
0897 0000 0000 0000 0000
0898 0000 0000 0000 0000
0899 0000 0000 0000 0000
089A 0000 0000 0000 0000
089B 0000 0000 0000 0000
089C 0000 0000 0000 0000
089D 0000 0000 0000 0000
089E 0000 0000 0000 0000
089F 0000 0000 0000 0000
0900 0000 0000 0000 0000

% ADDR OF R(A), INTO MAR2
% INCREMENT R(A)
% INCREMENT R(A)
% CLEAR LHM OF A3
% A3 = -C(R)/R(A*X)
% LOAD BR2 WITH Y
% WRITE OUT NEW Y VALUE
% NEXT Y ADDRESS
% SAVE NEXT Y IN BR1
% 1 IN BIT 16 OF B
% INCREMENT NEGATIVE COUNTER
% ISOLATE ADDR OF NEXT R(A*X)
% A3 TO THE ADDR
% RETURN TO TOP OF LOOP
% ALGEBRAIC LEFT SHIFT
% *P* INTO A2
% RR TYPE ALG LEFT SHIFT (REGISTER)
% SHIFT (R(A)) LEFT (R(M)) (-5) PLACES
% ZERO FILL, SET CC AND SET OVERFLOW BIT
% (R(M)) INTO B
% TEMP STORAGE
% PUT INSTR BACK INTO B
% (R(A)) INTO B
% MASK BITS 0-5
% CHECK FOR SHIFT >= 16
% SHIFT >= 16
% PERFORM LEFT SHIFT
% PUT DIGITS SHIFTED OUT IN A3
% CLEAR UHW (A)
% SHIFTED (R(A)) INTO MIR
% FLAG FOR SETTING OV OIT

```



```

0F75 5020 08C0 0020 0060
0F76 2000 08C0 0000 0060
0F77 2F50 08C0 0000 0060
0F78 66E0 08C0 0030 0060
0F79 66E0 08C0 0030 0060
0F7A 2F50 08C0 0000 0060
0F7B 66E0 08C0 0030 0060
0F7C 4809 C012 0020 0060
0F7D 63C9 08C0 0000 0060
0F7E 5020 0000 0000 0060
0F7F 4809 08C0 0050 0060
0F80 218C 08C0 0070 0060
0F81 2F50 08C0 0030 0060
0F82 66E0 08C0 0000 0060

0F83 6330 0000 0020 0060
0F84 4809 08C0 0050 0060
0F85 4809 0E55 0020 0060
0F86 00FC 00C0 0000 0060
0F87 4809 0E52 0000 0060
0F88 6819 08C0 0070 0060
0F89 2380 0000 0000 0060
0F8A 4809 C043 203C 0060
0F8B 4809 C043 083C 0060
0F8C 4809 E000 9020 0060
0F8D 80FC 0000 0070 0060
0F8E 4809 E155 800C 0060
0F8F 51C0 00C3 0000 0060
0F90 2F30 C0C0 0000 0060
0F91 4809 0040 20C0 0060
0F92 4809 2E56 C00C 0060
0F93 03F0 00C0 0000 0060
0F94 4809 2E55 0000 0060
0F95 9100 00C0 0070 0060
0F96 158C 0003 0000 0060
0F97 4809 0E55 0000 0060
0F98 4809 0E55 0000 0060
0F99 4809 C001 9020 0060
0F9A 4809 C001 9020 0060
0F9B 00C0 0000 0000 0060
0F9C 4809 C001 2070 0060
0F9D 4809 C001 8E90 0060
0F9E 4809 E002 0020 0060
0F9F 63C9 00C0 0000 0060
0FA0 5020 08C0 CFC0 0060
0FA1 2000 08C0 0000 0060
0FA2 2F50 08C0 0020 0060
0FA3 66E0 0000 C00C 0060
0FA4 4809 0000 0000 0060
0FA5 53C9 0000 0000 0060
0FA6 502C C000 0070 0060
0FA7 4809 0000 0050 0060
0FA8 218C 0000 0030 0060
0FA9 2F50 0000 0030 0060
0BAA 66E0 0000 0000 0060

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0049 5700 0000 0030 0060 00 03966000 0
0050 4809 0041 0020 00F0 00 03964000 0
0051 00AE 0000 00C3 000C 0030 00 03962000 0
0052 40AF 4809 0000 0000 00F0 00 03964000 0
0053 0000 2200 00C0 0070 0060 00 03964000 0
0054 00B1 4809 2055 0030 00F0 00 03965000 0
0055 0000 2550 0000 0000 00E0 00 03966000 0
0056 00B2 2180 0000 0020 0060 00 03967000 0
0057 00B4 4809 0045 0030 0060 00 03968000 0
0058 00B6 4809 0040 0030 0060 00 03969000 0
0059 01F5 2F50 00C0 0000 0060 00 03970000 0
0060 00B7 4809 0040 1030 00FC 00 03971000 0
0061 00B8 4809 0040 1030 00FC 00 03972000 0
0062 00B9 4809 0040 0010 00FC 00 03973000 0
0063 00BA 4809 0040 0070 00FC 00 03974000 0
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0065 00BC 159C 00C3 0000 0060 00 03976000 0
0066 00BD 4809 0041 0030 00F0 00 03977000 0
0067 00BE 0000 00C0 0070 0010 00 03978000 0
0068 00BF 4809 0040 0000 00F0 00 03979000 0
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0073 00C4 4809 0041 0010 00F0 00 03984000 0
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0082 00CC 5A00 0000 0000 0060 00 03993000 0
0083 00CD 5F90 0000 0000 0060 00 03994000 0
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0085 00CF 15AC 00C3 0070 00C0 00 03996000 0
0086 00D0 4809 00C0 0000 00FC 00 03997000 0
0087 00D1 4824 0000 0000 00FC 00 03998000 0
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0091 00D5 15E0 0000 0070 0040 00 04003000 0
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0097 00DB 0000 0000 0000 0060 00 04009000 0
0098 00DC 03F0 00C3 2000 00F0 00 04010000 0
0099 00DD 4809 00C0 2000 00F0 00 04011000 0
0100 00DE 4809 00C0 2000 00F0 00 04012000 0
0101 00DF 4809 00C0 2000 00F0 00 04013000 0
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0109 00E7 4809 00C0 2000 00F0 00 04021000 0
0110 00E8 4809 00C0 2000 00F0 00 04022000 0
0111 00E9 4809 00C0 2000 00F0 00 04023000 0
0112 00EA 4809 00C0 2000 00F0 00 04024000 0
0113 00EB 4809 00C0 2000 00F0 00 04025000 0
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0115 00ED 4809 00C0 2000 00F0 00 04027000 0
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0118 00F0 4809 00C0 2000 00F0 00 04030000 0
0119 00F1 4809 00C0 2000 00F0 00 04031000 0
0120 00F2 4809 00C0 2000 00F0 00 04032000 0
0121 00F3 4809 00C0 2000 00F0 00 04033000 0
0122 00F4 4809 00C0 2000 00F0 00 04034000 0
0123 00F5 4809 00C0 2000 00F0 00 04035000 0
0124 00F6 4809 00C0 2000 00F0 00 04036000 0
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0126 00F8 4809 00C0 2000 00F0 00 04038000 0
0127 00F9 4809 00C0 2000 00F0 00 04039000 0
0128 00FA 4809 00C0 2000 00F0 00 04040000 0
0129 00FB 4809 00C0 2000 00F0 00 04041000 0
0130 00FC 4809 00C0 2000 00F0 00 04042000 0
0131 00FD 4809 00C0 2000 00F0 00 04043000 0
0132 00FE 4809 00C0 2000 00F0 00 04044000 0
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0136 0102 4809 00C0 2000 00F0 00 04048000 0
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0162 011C 4809 00C0 2000 00F0 00 04074000 0
0163 011D 4809 00C0 2000 00F0 00 04075000 0
0164 011E 4809 00C0 2000 00F0 00 04076000 0
0165 011F 4809 00C0 2000 00F0 00 04077000 0
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0169 0123 4809 00C0 2000 00F0 00 04081000 0
0170 0124 4809 00C0 2000 00F0 00 04082000 0
0171 0125 4809 00C0 2000 00F0 00 04083000 0
0172 0126 4809 00C0 2000 00F0 00 04084000 0
0173 0127 4809 00C0 2000 00F0 00 04085000 0
0174 0128 4809 00C0 2000 00F0 00 04086000 0
0175 0129 4809 00C0 2000 00F0 00 04087000 0
0176 012A 4809 00C0 2000 00F0 00 04088000 0
0177 012B 4809 00C0 2000 00F0 00 04089000 0
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0197 013F 4809 00C0 2000 00F0 00 04109000 0
0198 0140 4809 00C0 2000 00F0 00 04110000 0
0199 0141 4809 00C0 2000 00F0 00 04111000 0
0200 0142 4809 00C0 2000 00F0 00 04112000 0

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CC12 4812 0000 0020 00F0  
 CC13 4809 0E5E 0E00 06F0  
 CC14 7C29 045E 1000 00F0  
 CC15 4809 0300 0870 00F0  
 CC16 4809 2F5E 0830 06F0  
 CC17 4809 00F1 0800 00F0  
 CC18 4809 0F41 0850 00F0  
 CC19 0000 0000 0000 0020  
 CC1A 4809 0640 0850 00F0  
 CC1B 2F50 0000 0800 0060  
 CC1C 2000 0000 0690 0060  
 CC1D 56E0 0000 0690 0060

OP1531

CC1E 5700 00C0 0070 0060  
 CC1F 4809 0F41 0820 00F0  
 CC20 0000 0000 0070 0030  
 CC21 48C9 0E03 0800 00F0  
 CC22 2200 00F0 0700 0060  
 CC23 4809 0C40 0630 20F0  
 CC24 4809 0F43 0C10 00F0  
 CC25 51E0 0000 0000 0060  
 CC26 2380 0000 0030 0060  
 CC27 4809 0F46 0630 00F0  
 CC28 2F50 0000 0670 0060  
 CC29 56E0 0003 0000 0040

CC2A 5F50 0003 0070 0060  
 CC2B 4809 0640 0000 00F0  
 CC2C 15F0 0000 0C70 00C0  
 CC2D 4809 0000 0000 00F0  
 CC2E 4824 0003 0030 00F0  
 CC2F 1600 0003 0030 0040  
 CC30 1630 0000 0000 0040  
 CC31 1620 0003 0000 0040  
 CC32 1630 0000 0030 0040

CC33 4809 0C40 5800 00F0  
 CC34 80FC 0000 0000 0080  
 CC35 48C9 2F5E 0830 00F0  
 CC36 51C0 0000 0C70 0060  
 CC37 2F30 0003 0000 0060  
 CC38 4809 0F41 2030 00F0  
 CC39 0010 00C0 0070 0040  
 CC3A 4809 0F41 0670 00F0  
 CC3B 0000 0000 0000 0030  
 CC3C 4809 2F5C 0010 00F0  
 CC3D 2F30 0000 0000 0060  
 CC3E 4809 0F5E 2070 00F0  
 CC3F 4809 0F5E 0630 00F0  
 CC40 00C0 0000 0000 0060  
 CC41 51C0 0000 0000 0060

A3 GE0 LIT  
 IF TRUE THEN A3 + NOT LIT + 1 = A3J JUMP  
 A3 = B  
 LIT - B = SAR  
 A2 C = B  
 B L = B  
 B L = B  
 B L = SAR  
 D R = MIR, B  
 D R = MIR, B  
 D R = MIR, B  
 SETICKA - 1 = CPCR  
 SETICKA - 1 = CPCR  
 OPFCODE - 1 = MPFC

X SET THE CONDITION BITS

X RX TYPE STORE AND INDEX BY 1  
 X (R(A)) INTO Y, R(M) + 1 -> R(M)  
 X ADDR OF Y INTO B

X R(A) INTO B  
 X Y ADDR INTO R2  
 X R(P) INTO B

X \*F\* INTO A2

XFCODE - 1 = CPCR  
 A2 + AMPCR = AMPCR  
 OPI6F - 1 = AMPCR  
 STEP  
 EXLC  
 OPI60 - 1 = MPFC  
 OPI61 - 1 = MPFC  
 OPI62 - 1 = MPFC  
 OPI63 - 1 = MPFC

OP160:

B R = B  
 Q = SAR, 15 = LIT  
 LIT AND P = B  
 REGSTACK - 1 = CPCR  
 EINPUT - 1 = EFCR  
 B L = A2  
 COMP 16 = SAR, 1 = LIT  
 BHAR L = B R1  
 COMP 8 = SAR  
 LIT OR BHAR = MPFC  
 EINPUT - 1 = CPCR  
 A2 OR B = A2  
 AS AND LIT = B  
 15 = LIT  
 REGSTACK - 1 = CPCR

04079C00 0  
 04080C00 0  
 04081C00 0  
 04082C00 0  
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 04132C00 0  
 04133C00 0  
 04134C00 0  
 04135C00 0  
 04136C00 0  
 04137C00 0

X RR TYPE ALGEBRAIC LEFT DOUBLE SHIFT  
 X SHIFT R(A), R(A+1), LEFT (R(M)) (0-5)  
 X ZERO FILL AND SET CC, SET OVERFLOW

X ISOLATE THE "A" FIELD  
 X ADDR OF R(A) INTO MAR2  
 X (R(A)) INTO B  
 X TEMP STORAGE OF (R(A))  
 X TEMP STORAGE OF (R(A))  
 X (R(A+1)) INTO B  
 X A2 = (R(A))/(R(A+1))  
 X ISOLATE "H" FIELD

X \*F\* INTO A2

XFCODE - 1 = CPCR  
 A2 + AMPCR = AMPCR  
 OPI6F - 1 = AMPCR  
 STEP  
 EXLC  
 OPI60 - 1 = MPFC  
 OPI61 - 1 = MPFC  
 OPI62 - 1 = MPFC  
 OPI63 - 1 = MPFC

OP160:

B R = B  
 Q = SAR, 15 = LIT  
 LIT AND P = B  
 REGSTACK - 1 = CPCR  
 EINPUT - 1 = EFCR  
 B L = A2  
 COMP 16 = SAR, 1 = LIT  
 BHAR L = B R1  
 COMP 8 = SAR  
 LIT OR BHAR = MPFC  
 EINPUT - 1 = CPCR  
 A2 OR B = A2  
 AS AND LIT = B  
 15 = LIT  
 REGSTACK - 1 = CPCR



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01611
- B = SAR
A2 R = A3
M01 A3
IF NOT APT THEN SET LCL
0BIT 1 = CPCR
A2 L = A2, B1 SET LCL
SEICCA - 1 = CPCR
ASR
BMAR R = MAR2
B = SAR
A2 R = MIR
16 = SAR
FOIUTPUT - 1 = CPCR
COMP 16 = SAR, 1 = LIT
A2 L = A2
LIT OR BMAR = MAR2
EINPUT - 1 = CPCR
OPCODE - 1 = MPCR

CONTENISGH - 1 = CPCR
C = BRI SAR 2 = LIT
COMP 8 = SAR, 1 = MIR
BMAR L = BR2
EMULOUT - 1 = CPCR
A3 R = B, 1 = CPCR
15 = LIT, 4 = SAR
LIT AND P = B
A3 = B
CONTENISFA - 1 = CPCR
B = MIR
BMAR = BR2
EMULOUT - 1 = CPCR
BMAR + 1 L = BRI
COMP 8 = SAR
A3 R = MAR2
16 = SAR, 1 = LIT
LIT OR BMAR = MAR2
EINPUT - 1 = CPCR
B = MIR
BMAR = BR2
[EMULOUT - 1 = CPCR
OPCODE - 1 = MPCR

% FOR OVERFLOW TEST
% SET OVERFLOW BIT
% REFERENCE BRI
% PI TYPE 2 STORE AND INDEX BY 2
% (R(A),R(A+1)) INTO Y*, Y+1
% (R(M)) + 2 INTO R(H)
% (R(M)) INTO B
% Y* INTO ERI
% REFERENCE BR1
% (R(A)) INTO Y*
% ADDP OF Y* + 1
% ADDR OF R(A)
% (R(A+1)) INTO B
% (R(A+1)) INTO B
% REFERENCE BRI
% (R(A+1)) INTO Y* + 1
% PK TYPE ALS LEFT DOUBLE SHIFT
% SHIFT (R(A),R(A+1)) LEFT Y (0-5) PLACES
% ZERO FILL, SET CC AND SET OVERFLOW BIT
% ISOLATE "M"

04139600 0
04140000 0
04141000 0
04142000 0
04143000 0
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04190000 0
04191000 0
04192000 0
04193000 0
04194000 0
04195000 0
04196000 0
04197000 0

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0657 336C 0000 007C 0060
0658 4809 0000 007C 0060
0659 002C 0070 0050 0060
065A 4809 2C80 0F3C 00F0
065B 51E0 0070 0030 0060
065C 51E0 0070 0030 0060
065D 4809 E000 8800 00F0
065E 80FC 0000 0070 0080
065F 4809 2C56 0B30 00F0
0660 51C0 0000 0030 0060
0661 4809 E0C0 CE30 00F0
0662 2280 0000 009F 0060
0663 4809 0C40 003C 00F0
0664 4809 0000 007C 20F0
0665 4809 0F43 0010 00F0
0666 61E0 00C3 0000 0060
0667 4809 0F47 0030 00F0
0668 0000 0000 0000 0030
0669 4809 E0C3 801C 00F0
066A 0010 0050 0000 00A0
066B 4809 2F5C 001C 00F0
066C 2F3C 0000 0030 0060
066D 4809 0C40 003C 00F0
066E 4809 0000 0030 20F0
066F 4809 0F43 0010 00F0
0670 61E0 00C3 0000 0060
0671 56E0 0000 0030 00A0

0672 4809 2C56 0E7C 00F0
0673 00FC 0000 0000 00EC

```





0 EOL B  
 1 TRUE THEN SKIP  
 2 UNTERSPH - 1 = CPGR % (R(M)) INTO B  
 3 = SAR  
 4 = SAR, 15 = LIT  
 5 AND LIT = B  
 6 REGSTACK - 1 = CPGR  
 7 BHAR L = B RI  
 8 COMP B = SAR  
 9 INPUT - 1 = CPGR  
 10 B L = A3  
 11 COMP 16 = SAR, 1 = LIT  
 12 LIT OR BHAR = MAR2  
 13 INPUT - 1 = CPGR  
 14 A3 OR B = A2, B RI  
 15 - B = SAR  
 16 A2 R = A3  
 17 NOT A3  
 18 NOT ABT THEN SET LCI  
 19 - B = SAR  
 20 A2 L = A3, B, SET LCI  
 21 SETCCA - 1 = CPGR  
 22 A3 L = A2  
 23 COMP 16 = SAR  
 24 A2 R = MIR  
 25 A3 R = MIR  
 26 ASR  
 27 BHAR R = MAR2  
 28 B = SAR  
 29 EUIPUT - 1 = CPGR  
 30 OPCODE - 1 = MPCR  
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OP1631



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CC4B 4809 00C0 0000 20F0
CC4C 4809 0F43 001C 00F0
CC4D 61E0 0000 0000 0060
CF4E 4809 0F47 0020 00F0
CC4F 0000 00C3 0070 0530
CFD0 4809 0003 001C 00F0
CF91 2F3C 0003 0000 006C
CFB2 4809 0C4C 0030 00F0
CFB3 4809 0000 0000 20F0
CFB4 4809 0F43 001C 00F0
CFB5 61E0 0000 0000 006C
CFB6 66E0 0000 0070 0040

0CB7 5F9C 0003 0000 0060
0CB8 4809 0C40 0030 00F0
0CB9 1640 00C0 0000 00C0
0CBA 4809 0000 0000 00F0
0CBB 4824 00C0 00C0 00FC

0CBC 1650 00C0 0000 004C
0CBD 0000 0000 0000 004C
0CBE 165C 00C0 0030 004C
0CBF 166C 00C0 0070 0040

0CC0 2380 0003 0000 0060
0CC1 4809 0C40 2000 00F0
0CC2 4809 0000 0000 00F0
0CC3 80F0 0000 0000 0080
0CC4 4809 2556 0090 00F0
0CC5 51C0 0000 00C0 0060
0CC6 4809 0F41 0020 00F0
0CC7 001C 0000 0070 0080
0CC8 4809 2F5C 001C 00F0
0CC9 2F3C 0000 0000 0060
0CCA 4809 0F45 001C 00FC
0CCB 0000 00C1 0000 00FC
0CCD 2F3C 0000 0000 0060
0CCE 4809 0C5C 1020 00F0
0CCF 4809 0002 0000 00FC
0CD0 4809 00C0 0000 00F0
0CD1 4C99 0001 9870 00F0
0CD2 2000 0000 0000 0060
0CD3 4809 00C1 0070 00F0
0CD4 0000 00C0 0070 0020
0CD5 4809 0C40 0030 00F0
0CD6 2F50 00C3 00C0 0060
0CD7 4809 00C3 0000 20F0
0CD8 4809 0F43 801C 00F0
0CD9 0000 00C0 0000 0010
0CDA 4809 00C0 8030 00FC
0CDB 0000 0000 0000 002C
0CCD 2F5C 0000 0000 006C
0CDD 66E0 0000 0000 004C

ASB
DMAR = DR2
EMULOUT - 1 = CPCR
EMHAR + 1 L = RR1
COMP 0 = SAR
A3 = HAR2
EINPUT - 1 = CPCR
B = MIR
ASR
DMAR = DR2
EMULOUT - 1 = CPCR
OPCODE - 1 = HPCR

OPCODE17: XFCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP17F - 1 = AMPCR
STEP
EXEC

OP17F: OP17C - 1 = HPCR
OP17I - 1 = HPCR
OP17Z - 1 = HPCR
OP17S - 1 = HPCR

OP170:
CONTENISRM - 1 = CPCR
B = A2
A3 R = B
4 = SARJ 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR
EMHAR L = BR1
COMP 0 = SARJ 1 = LIT
LIT OR EMHAR = HAR2
EINPUT - 1 = CPCR
EMHAR + 1 = HAR2
B L = A3
COMP 16 = SAR
EINPUT - 1 = CPCR
A3 OR B = A3
NOT A2 = A2
A2 + 1 = SAR
A3 C = A3 B1 SET LC1
SETCCA - 1 = CPCR
A3 L = B
COMP 16 = SAR
B R = MIR
FOUTPUT - 1 = CPCR
ASR
EMHAR R = HAR2
B = SAR
A3 R = MIR
16 = SAR
EINPUT - 1 = CPCR
OPCODE - 1 = HPCR

REFERENCE BR1
% ADDR OF Y INTO BR2
% (R(A)) INTO Y
% ADDR OF Y + 1
% (R(A+1)) INTO B
% REFERENCE BR1
% (R(A+1)) INTO Y+1
% *F* INTO A2
% REFERENCE BR1
% (R(A+1)) INTO Y+1
%
%
% RR TYPE CIRCULAR DOUBLE LEFT SHIFT
% SHIFT (R(A),R(A+1)) LEFT CIRCULARLY
% (R(H)) (0-5) PLACES AND SET CC
% (R(P)) INTO B
%
%
CONTENISRM - 1 = CPCR
B = A2
A3 R = B
4 = SARJ 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR
EMHAR L = BR1
COMP 0 = SARJ 1 = LIT
LIT OR EMHAR = HAR2
EINPUT - 1 = CPCR
EMHAR + 1 = HAR2
B L = A3
COMP 16 = SAR
EINPUT - 1 = CPCR
A3 OR B = A3
NOT A2 = A2
A2 + 1 = SAR
A3 C = A3 B1 SET LC1
SETCCA - 1 = CPCR
A3 L = B
COMP 16 = SAR
B R = MIR
FOUTPUT - 1 = CPCR
ASR
EMHAR R = HAR2
B = SAR
A3 R = MIR
16 = SAR
EINPUT - 1 = CPCR
OPCODE - 1 = HPCR

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04258000 0
04258000 0
04258000 0
04261000 0
04261000 0
04262000 0
04263000 0
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04269000 0
04270000 0
04271000 0
04272000 0
04273000 0
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04319000 0  
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 04321000 0  
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 04376000 0

RI TYPE I STORE ZERO, 0 INTO Y\*  
 (RCH) INTO B  
 PK TYPE CIRCULAR LEFT DOUBLE SHIFT  
 SHIFT (R(A),RCA+J) LEFT CIR. Y (0-5)  
 AND SET LC

A3 = (R(H))/INSTRUCTION  
 Y\* INTO B  
 (R(H)) INTO A2  
 Y INTO A2  
 ISOLATE \*A\*  
 TEMP STORAGE OF R(A)  
 (R(A)) INTO E  
 (R(A)) INTO IS WORD OF A3  
 (R(A+1)) INTO B  
 A3 = (R(A))/R(A+1)  
 COMP OF Y (0-5)  
 PERFORM SHIFT  
 SET THE CONDITION BITS  
 SHIFTED (R(A+1)) INTO HI  
 REFERENCE BR1

PK TYPE STORE ZERO, 0 INTO Y  
 ADDR OF Y INTO D

CONTENTS R - 1 = CPCR  
 B L = BR2  
 COMP 8 = SAR  
 0 = MIR  
 FULOUT - 1 = CPCR  
 OPCODE - 1 = HPCR

LIT AND 0 = B  
 15 = LIT  
 EOL B  
 IF TRUE THEN SKIP  
 CONTENTS R - 1 = CPCR  
 B L = B  
 COMP 16 = SAR  
 A3 OR 0 = A3  
 IFETCH - 1 = CPCR  
 A3 R = A2  
 16 = SAR  
 A2 + B = A2  
 A3 R = A3  
 4 = SAR; 15 = LIT  
 A3 AND LIT = B  
 REGSTACK - 1 = CPCR  
 BHAR L = BR1  
 COMP 8 = SAR; 1 = LIT  
 LIT OR BHAR = HAR2  
 P L = A3  
 COMP 16 = SAR  
 EINPUT - 1 = CPCR  
 A3 OR 0 = A3  
 NBT A2 = A2  
 A3 C = SAR  
 A3 C = A3B1 SET LC1  
 SETPCA - 1 = CPCR  
 A3 L = A2  
 COMP 16 = SAR  
 A2 R = MIR  
 EINPUT - 1 = CPCR  
 ASR  
 BHAR R = HAR2  
 8 = SAR  
 A3 R = MIR  
 16 = SAR  
 EINPUT - 1 = CPCR  
 OPCODE - 1 = HPCR

RXNFIELD - 1 = CPCR  
 B L = BR2  
 COMP 8 = SAR  
 C = MIR

0P171:  
 0P172:  
 0P173:

PCDE 2380 00C3 0070 0060  
 0CDF 4809 0C41 0010 00F0  
 0CE0 0000 0000 0000 0030  
 0CE1 4809 00C0 0090 00F0  
 0CE2 61E0 00C0 0070 0060  
 0CE3 66E0 0000 0000 0040  
 CCEH 4809 2C56 0B3C 00F0  
 0CE5 00FC 0C00 0070 00F0  
 0CE6 4809 0C52 0020 00F0  
 0CE7 6819 0000 0000 00F0  
 0CE8 234C 0000 0070 0060  
 0CE9 4809 0C41 0B30 00F0  
 0CEA 0000 0070 0070 0020  
 0CEB 4809 EC5C 1C30 00F0  
 0CEC 6330 00C0 0000 0060  
 0CED 4809 E0C0 0000 00F0  
 0CEE 0000 00C0 0070 0020  
 0CEF 4809 CC40 2770 00F0  
 0CE0 4809 EC00 9000 00F0  
 0CF1 50FC 00C3 0020 008C  
 0CF2 4809 E155 0B30 00FC  
 0CF3 51CC 00C0 0070 0060  
 0CF4 4809 0F41 0C20 00F0  
 0CF5 001C 00C3 0000 0080  
 0CF6 2F3C 0000 0000 0060  
 0CF7 4809 2F5C 001C 00FC  
 0CF8 4809 0C41 1C00 00F0  
 0CF9 0000 00C0 0070 0020  
 0CEA 2F30 00C3 0020 0060  
 0CEB EC05 3070 00F0  
 0CEC 4809 C0C3 0000 00F0  
 0CEE 4809 E0C1 9B30 00F0  
 0CFE 2000 00C0 00C0 0060  
 0CE0 4809 E0C1 2C30 00F0  
 0CE1 0000 00C0 0030 0020  
 0CE2 4809 C0C0 8030 00F0  
 0CE3 2F5C 00C7 0070 0060  
 0CE4 4809 0000 0020 00F0  
 0CE5 4809 0F43 801C 00FC  
 0CE6 0000 00C0 0070 0010  
 0CE7 4809 E000 803C 00F0  
 0CE8 0000 00C0 0000 0020  
 0CE9 2F50 00C3 0000 006C  
 0CEA 66E0 00C0 0000 0040  
 0000 57C0 0000 0020 0060  
 000C 4809 0C41 0010 00FC  
 0000 0000 00C0 0000 0030  
 000E 4809 00C0 0050 00F0



```

0010 66E0 0F00 0030 0040
0011 5F5C 0000 0000 0060
0012 4809 0640 0040 00F0
0013 165F 0000 0000 00C0
0014 4809 0000 0000 00F0
0015 4824 0000 0030 00F0
0016 1640 00C0 0000 0040
0017 168C 0000 0030 0040
0018 165C 00C0 0000 0040
0019 160F 0000 0030 0040
0020 22B0 00C0 0000 0060
0021 28F9 0E41 2030 00F0
0022 0D1C 0000 0000 0040
0023 4859 E155 0070 00F0
0024 51C0 0000 0020 006C
0025 2F30 0000 0000 0060
0026 4849 0E41 0000 00F0
0027 4809 0E5E 0030 00F0
0028 78C9 0000 0030 00F0
0029 1E7C 0000 0000 0060
0030 4F16 0000 0030 0060
0031 4809 0E40 0030 00F0
0032 4809 0E40 0030 00F0
0033 0070 0000 0000 0020
0034 4809 E003 001C 00F0
0035 2F5C 0000 0000 0060
0036 2P00 00C0 0000 0060
0037 56E0 0000 0000 0040
0038 2380 0000 0070 0060
0039 4809 0E41 0020 00FC
0040 0E0C 0000 0030 003C
0041 4809 E000 0000 00F0
0042 0E30 22E8 0000 0070 006C
0043 4809 0E41 2030 00F0
0044 0000 0000 0000 0020
0045 4809 0070 0000 20F0
0046 0034 4809 0F43 0010 00F0
0047 0035 60E0 0000 0000 0060
0048 4869 0E41 0000 00F0
0049 4809 0E5E 0030 002C
0050 78C9 0000 0000 0060
0051 1E70 0000 0030 0060
0052 4F10 0000 0000 0060
0053 4809 0000 0000 00F0
0054 4809 0E40 0000 00F0
0055 4809 0E40 0000 00F0
0056 4809 0E40 0000 00F0
0057 4809 0E40 0000 00F0
0058 4809 0E40 0000 00F0
0059 4809 0E40 0000 00F0
0060 4809 0E40 0000 00F0
0061 4809 0E40 0000 00F0
0062 4809 0E40 0000 00F0
0063 4809 0E40 0000 00F0
0064 4809 0E40 0000 00F0
0065 4809 0E40 0000 00F0
0066 4809 0E40 0000 00F0
0067 4809 0E40 0000 00F0
0068 4809 0E40 0000 00F0
0069 4809 0E40 0000 00F0
0070 4809 0E40 0000 00F0
0071 4809 0E40 0000 00F0
0072 4809 0E40 0000 00F0
0073 4809 0E40 0000 00F0
0074 4809 0E40 0000 00F0
0075 4809 0E40 0000 00F0
0076 4809 0E40 0000 00F0
0077 4809 0E40 0000 00F0
0078 4809 0E40 0000 00F0
0079 4809 0E40 0000 00F0
0080 4809 0E40 0000 00F0
0081 4809 0E40 0000 00F0
0082 4809 0E40 0000 00F0
0083 4809 0E40 0000 00F0
0084 4809 0E40 0000 00F0
0085 4809 0E40 0000 00F0
0086 4809 0E40 0000 00F0
0087 4809 0E40 0000 00F0
0088 4809 0E40 0000 00F0
0089 4809 0E40 0000 00F0
0090 4809 0E40 0000 00F0
0091 4809 0E40 0000 00F0
0092 4809 0E40 0000 00F0
0093 4809 0E40 0000 00F0
0094 4809 0E40 0000 00F0
0095 4809 0E40 0000 00F0
0096 4809 0E40 0000 00F0
0097 4809 0E40 0000 00F0
0098 4809 0E40 0000 00F0
0099 4809 0E40 0000 00F0
0100 4809 0E40 0000 00F0

```

```

OPCODE - 1 = MPCR
X
X *F* INTO A2
OP20F:
X
OP200:
X
X RR TYPE SUBTRACT REGISTER
X (R(A)) - (R(H)) INTO R(A)
X SET CC, CARRY AND OVERFLOW
X (R(A)) INTO B
X (R(A)) INTO MS WORD OF A2
CONTENISRA - 1 = CPCR
9 L = A2; IF LCI
CMP 16 = SAR; 15 = LIT
A3 AND LIT = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B L = B; SET LC2
A2 - B = MIR
IF .ADV THEN SET LCI
CARRY - 1 = CPCR
CHECKOV - 1 = CPCR
MIR = B; MIR
16 = SAR
A3 R = MAR2
EINPUT - 1 = CPCR
SETCCA - 1 = CPCR
OPCODE - 1 = MPCR
X
X ADDR OF R(A)
X SET THE CONDITION BITS
X RI TYPE 2 SUBTRACT (INDIRECT)
X (R(A)) - (Y*) INTO R(A),
X SET CC, CARRY, AND OV BITS
X Y* INTO ERI
CONTENISRM - 1 = CPCR
B L = B; RI
CMP 8 = SAR
A3 = B
CONTENISFA - 1 = CPCR
E L = A2
CMP 16 = SAR
ASR
RVAR = BR2
EQUILIN - 1 = CPCR
B L = B
CMP 16 = SAR
A2 - B = MIR; SET LC2
X (R(A)) - (Y*) INTO MIR
A2 - B WHEN SET LCI
CARRY - 1 = CPCR
PHI
B R = B; MIR

```









```

0071 3690 0000 0030 0060
0072 4800 0000 0030 0060
0073 4800 0000 0030 0060
0074 4800 0000 0030 0060
0075 4824 0000 0030 0060

0076 16FC 0000 0030 0060
0077 1700 0000 0030 0060
0078 3000 0000 0030 0060
0079 171C 0000 0030 0060

0P210:
007A 4809 0C40 0030 0060
007B 30F0 00C0 0030 0060
007C 4809 2C55 0030 0060
007D 51CC 00C0 0030 0060
007E 2F3C 00C0 0030 0060
007F 4809 0C41 2030 0060
0080 0000 0000 0030 0060
0081 4809 0F41 0030 0060
0082 001C 00C0 0030 0060
0083 4809 2F5C 0030 0060
0084 4809 2F5C 0030 0060
0085 4805 0050 0030 0060
0086 4809 0E55 0030 0060
0087 00F0 0000 0030 0060
0088 51C0 0000 0030 0060
0089 2F3C 00C0 0030 0060
008A 4809 0C41 1030 0060
008B 0010 00C0 0030 0060
008C 4809 2F5C 0030 0060
008D 2F30 0000 0030 0060
008E 4809 EC5C 0030 0060
008F 4849 CC5E 0030 0060
0090 78C9 0000 0030 0060
0091 4E70 0000 0030 0060
0092 4F10 0000 0030 0060
0093 49C9 00C0 0030 0060
0094 200C 00C0 0030 0060
0095 4809 00C0 0030 0060
0096 4809 0C40 0030 0060
0097 0000 00C0 0030 0060
0098 4809 0C41 0030 0060
0099 4809 00C0 8030 0060
009A 4809 00C0 0030 20F0
009B 0000 00C0 7016 0060
009C 2F5C 00C0 0030 0060
009D 4809 F0D2 0030 0060
009E 4809 00C0 0030 0060
009F 2F50 0000 0030 0060
00A0 56EC 0000 0030 0060
00A1

0P211:
00A2 3690 0000 0030 0060
00A3 4800 0000 0030 0060
00A4 4800 0000 0030 0060
00A5 4800 0000 0030 0060
00A6 4824 0000 0030 0060

0P21F:
0P210 - 1 = MPCR
0P211 - 1 = MPCR
FAULT - 1 = MPCR
0P213 - 1 = MPCR

B R = B
4 = SARJ 15 = LIT
LIT AND 0 = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B L = A2
COMP 16 = SAR
BHAR L = BRI
COMP 8 = SARJ 1 = LIT
LIT OR BHAR = MAR2
EINPUT - 1 = CPCR
A2 AND LIT = B
15 = LIT
REGSTACK - 1 = CPCR
B L = A3
COMP 16 = SARJ 1 = LIT
LIT OR BHAR = MAR2
A3 OR B = B
A2 - 0 = MIRJ SET LC2
IF ADV THEN SET LC1
CARRY - 1 = CPCR
DHJ SET LC1
SETCCA - 1 = CPCR
BRI
B R = MIR
16 = SAR
B L = B
B R = B
BHAR R = MAR2, A3
EINPUT - 1 = CPCR
A3 OR 1 = MAR2
B = MIR
EQUIPUT - 1 = MPCR
OPCODE - 1 = MPCR

```

```

04478000 D
04499000 D
04500000 D
04510000 D
04520000 D
04530000 D
04540000 D
04550000 D
04560000 D
04570000 D
04580000 D
04590000 D
045A0000 D
045B0000 D
045C0000 D
045D0000 D
045E0000 D
045F0000 D
04600000 D
04610000 D
04620000 D
04630000 D
04640000 D
04650000 D
04660000 D
04670000 D
04680000 D
04690000 D
046A0000 D
046B0000 D
046C0000 D
046D0000 D
046E0000 D
046F0000 D
04700000 D
04710000 D
04720000 D
04730000 D
04740000 D
04750000 D
04760000 D
04770000 D
04780000 D
04790000 D
047A0000 D
047B0000 D
047C0000 D
047D0000 D
047E0000 D
047F0000 D
04800000 D
04810000 D
04820000 D
04830000 D
04840000 D
04850000 D
04860000 D
04870000 D
04880000 D
04890000 D
048A0000 D
048B0000 D
048C0000 D
048D0000 D
048E0000 D
048F0000 D
04900000 D
04910000 D
04920000 D
04930000 D
04940000 D
04950000 D
04960000 D
04970000 D
04980000 D
04990000 D
049A0000 D
049B0000 D
049C0000 D
049D0000 D
049E0000 D
049F0000 D
04A00000 D
04A10000 D
04A20000 D
04A30000 D
04A40000 D
04A50000 D
04A60000 D
04A70000 D
04A80000 D
04A90000 D
04AA0000 D
04AB0000 D
04AC0000 D
04AD0000 D
04AE0000 D
04AF0000 D
04B00000 D
04B10000 D
04B20000 D
04B30000 D
04B40000 D
04B50000 D
04B60000 D
04B70000 D
04B80000 D
04B90000 D
04BA0000 D
04BB0000 D
04BC0000 D
04BD0000 D
04BE0000 D
04BF0000 D
04C00000 D
04C10000 D
04C20000 D
04C30000 D
04C40000 D
04C50000 D
04C60000 D
04C70000 D
04C80000 D
04C90000 D
04CA0000 D
04CB0000 D
04CC0000 D
04CD0000 D
04CE0000 D
04CF0000 D
04D00000 D
04D10000 D
04D20000 D
04D30000 D
04D40000 D
04D50000 D
04D60000 D
04D70000 D
04D80000 D
04D90000 D
04DA0000 D
04DB0000 D
04DC0000 D
04DD0000 D
04DE0000 D
04DF0000 D
04E00000 D
04E10000 D
04E20000 D
04E30000 D
04E40000 D
04E50000 D
04E60000 D
04E70000 D
04E80000 D
04E90000 D
04EA0000 D
04EB0000 D
04EC0000 D
04ED0000 D
04EE0000 D
04EF0000 D
04F00000 D
04F10000 D
04F20000 D
04F30000 D
04F40000 D
04F50000 D
04F60000 D
04F70000 D
04F80000 D
04F90000 D
04FA0000 D
04FB0000 D
04FC0000 D
04FD0000 D
04FE0000 D
04FF0000 D

```



```

00A2 4809 0C40 003C 0C60
00A3 4809 00C0 0C7C 00B0
00A4 4809 2E55 0030 00F0
00A5 51C0 00C0 0070 006F
00A6 2F30 00C0 0000 006E
00A7 4809 0C41 2C30 00F0
00A8 00C0 00C0 003C 0020
00A9 4809 0F41 0C70 00F0
00AA 0010 00C0 0000 0000
00AB 4809 2F5C 0C1C 00F0
00AC 2F3C 00C0 0000 006E
00AD 4809 C05C 2030 00F0
00AE 4809 E556 0000 00F0
00AF 00FC 0000 0000 00E0
00B0 51C0 0000 0000 006E
00B1 2F3C 00C0 0000 0060
00B2 4809 0C41 0C10 00F0
00B3 50E0 0000 0000 003C
00B4 4809 2F5C 001C 00F0
00B5 4809 0C41 0070 00BA
00B6 4809 0C41 0000 0070
00B7 000C 0050 0000 0070
00B8 65E0 0000 003C 0070
00B9 4809 E08A 0000 00F0
00BA 4809 C05E 0C90 00F0
00BB 78C9 0000 0000 00F0
00BC 4E1C 0500 0070 0060
00BD 49C9 0000 0000 00F0
00BE 49C9 0000 0000 00F0
00BF 49C9 0000 0000 00F0
00C0 2000 0000 0000 0060
00C1 4809 0000 0000 00F0
00C2 4809 0C40 8C90 00F0
00C3 000C 0000 0000 0020
00C4 4809 0C41 0030 00F0
00C5 4809 0C40 8B70 00F0
00C6 4809 0000 007C 00FF
00C7 4809 0F43 8C1C 0000
00C8 001C 0000 0000 009C
00C9 2F50 0000 0000 0060
00CA 4809 2F5C 001C 00F0
00CB 4809 0C40 0000 00F0
00CC 2F5C 0000 0000 0060
00CD 68EC 0000 00C0 0060

```

0P213:

```

00CE 5700 0C40 0020 0060
00CF 4809 0C41 0C10 00FF
00D0 000C 00C0 0070 003F
00D1 60EC 0C00 0C7C 0060
00D2 4809 0C41 2070 00F0
00D3 000C 0000 0000 0020
00D4 4809 2F5C 0F1C 00F0
00D5 001C 0000 0000 0000
00D6 50E0 0000 0000 0060
00D7 4809 C05C 0030 0060

```

```

0 R = B
q = SARI 15 = LIT
LIT AND B = B
REGSTACK - 1 = CPCR
FINPUT - 1 = CPCR
R L = A2
COMP 16 = SAR
BHAR L = BR1
COMP 8 = SAR J = LIT
LIT OR BHAR = MAR2
FINPUT - 1 = CPCR
A2 OR B = A2
A3 AND LIT = 0
15 = LIT
REGSTACK - 1 = CPCR
FINPUT - 1 = CPCR
R L = BR2
COMP 8 = SAR
EYULIN - 1 = CPCR
LIT OR BHAR L = ER2
COMP 8 = SAR J = LIT
COMP 16 = SAR
EYULIN - 1 = CPCR
A3 OR B = B
A2 - D = MIR J SET LC2
IF ADV THEN SET LC1
CHECKOV - 1 = CPCR
BH1 SET LC1
SETCCA - 1 = CPCR
BH1
R R = MIR
16 = SAR
R L = B
R R = B
ASR
BHAR R = MAR2
8 = SAR J = LIT
FINPUT - 1 = CPCR
LIT OR BHAR = MAR2
B = MIR
FINPUT - 1 = CPCR
OPCODE - 1 = CPCR

```

```

R(X),R(A+1), SET CC, CARRY AND 0V BYTE
% ISOLATE *A*
% R(A) INTO E
% R(A) INTO MS WORD OF A2
% SAVE ADDR OF R(A)
% R(A+1)
% R(A+1) INTO B
% A2 = R(A)/(R(A+1))
% ISOLATE *M*
% CR(X) INTO B
% R(RH) INTO E
% (*) INTO B
% ADDR OF Y+1
% (*) INTO MS WORD OF A3
% R = (Y)/(Y+1)
% PERFORM SUBTRACTION
% SET THE 0V BITS
% SET THE CONVICTION BITS
% NEW R(A)
% NEW R(A+1)
% REF BR1
% ADDR OF R(A)
% WRITE NEW R(A)
% R(A+1)
% WRITE NEW R(A+1)
%
% RY TYPE SUBTRACT DOUBLE
% R(X),R(A+1),R(Y),R(A+1),R(A+1)
% SET CARRY AND CARRY BYTE
% Y ADDR INTO E
% (Y) INTO B
% (Y) INTO MS WORD OF A2
% ADDR OF Y+1
% (Y+1) INTO B
% MIR = (Y)/(Y+1)

```









```

LEW0 0007 0103 0000 1000 0000
0E0E 0000 0000 0000 0020
0E0F 4809 0C40 8B30 00FC
0E10 2F50 0000 0C70 0060
0E11 26D0 0000 0000 0060
0E12 56E0 0000 0070 0060

0P2211
0E13 22BC 00C0 0000 0060
0E14 4809 0C40 2C70 001C
0E15 00FC 0000 0070 00A0
0E16 4809 0E50 0000 00F0
0E17 51CC 0000 0000 006C
0E18 1E30 0C40 0010 006C
0E19 0000 0000 0000 0030
0E20 56E0 00C0 0C30 006C
0E21 4809 0C40 0000 00F0
0E22 00C0 0000 0070 0020
0E23 4809 0000 0070 0020
0E24 48C9 0C40 8B30 00F0
0E25 2F50 0000 0000 0060
0E26 2000 0000 0070 0060
0E27 56E0 00C0 0070 0060

0P2221
0E28 4809 2C50 0030 00F0
0E29 00FC 0000 0000 0060
0E2A 4809 0C50 0030 00F0
0E2B 5019 0C00 0070 00FC
0E2C 2380 00C0 0000 0060
0E2D 4809 0C40 0000 0060
0E2E 4809 0E50 0070 006C
0E2F 5330 0000 0C70 0060
0E30 4809 0000 0000 00FC
0E31 4809 0C00 0000 0020
0E32 4809 0C40 0030 00F0
0E33 4809 0E00 0070 00F0
0E34 4809 0E00 0070 00F0
0E35 22BC 0000 0C30 0060
0E36 4809 0C40 2C30 00F0
0E37 0000 00C0 0000 0020
0E38 4809 0C40 0030 00F0
0E39 78C9 0000 0000 00F0
0E3A 1E70 00C0 0070 006C
0E3B 4F10 0000 0000 0060
0E3C 4809 0000 0000 00F0
0E3D 4809 0C40 8B30 00F0
0E3E 0000 0000 0070 0020
0E3F 2F50 00C0 0070 0060
0E40 2000 0000 0000 0060

```

```

06679000 0
06684000 0
06691000 0
06698000 0
06705000 0
06712000 0
06719000 0
06726000 0
06733000 0
06740000 0
06747000 0
06754000 0
06761000 0
06768000 0
06775000 0
06782000 0
06789000 0
06796000 0
06803000 0
06810000 0
06817000 0
06824000 0
06831000 0
06838000 0
06845000 0
06852000 0
06859000 0
06866000 0
06873000 0
06880000 0
06887000 0
06894000 0
06901000 0
06908000 0
06915000 0
06922000 0
06929000 0
06936000 0
06943000 0
06950000 0
06957000 0
06964000 0
06971000 0
06978000 0
06985000 0
06992000 0
06999000 0
07006000 0
07013000 0
07020000 0
07027000 0
07034000 0
07041000 0
07048000 0
07055000 0
07062000 0
07069000 0
07076000 0
07083000 0
07090000 0
07097000 0
07104000 0
07111000 0
07118000 0
07125000 0
07132000 0
07139000 0
07146000 0
07153000 0
07160000 0
07167000 0
07174000 0
07181000 0
07188000 0
07195000 0
07202000 0
07209000 0
07216000 0
07223000 0
07230000 0
07237000 0
07244000 0
07251000 0
07258000 0
07265000 0
07272000 0
07279000 0
07286000 0
07293000 0
07300000 0
07307000 0
07314000 0
07321000 0
07328000 0
07335000 0
07342000 0
07349000 0
07356000 0
07363000 0
07370000 0

```

```

X SET THE CONDITION BITS
X
X
X TYPE R1 TYPE 2 ADD, (R(A)),(Y) ->
X R(A), SET CC, CARRY, AND 0V BITS
X (R(A)) INTO B
X (R(A)) INTO MS WORD CF A2
X
X (R(H)) INTO B
X (Y) INTO B
X (Y) INTO MS WORD OF R
X
X ADDR OF R(A)
X
X WRITE NEW R(A)
X
X TYPE RK ADD, (R(A)),Y -> R(A)
X SET CC, CARRY AND 0V BITS
X
X
X (R(H)) INTO B
X (R(H)) INTO MS WORD OF B
X A3 = (R(H))/INSTRUCTION
X Y = INTO B
X (R(H)) INTO A2
X Y INTO MIR
X (R(A)) INTO B
X (R(A)) INTO MS WORD OF A2
X PERFORM ADDITION
IF ADV THEN SET LC1
CARRY - 1 = CPGR
CHECKOV - 1 = CPGR
BHI
B R = B, MIR
16 = SAR
OUTPUT - 1 = CPGR
SETCCA - 1 = CPGR
X SET THE CONDITION BITS

```



0P2231:

0E42 370C 0000 0C70 006C  
 0E43 48F9 C041 0C1C 00F0  
 0E44 000C 00C0 00C0 003C  
 0E45 50E0 00C0 00D0 0060  
 0E46 4809 0041 0C90 C0F0  
 0E47 0000 00C0 00C0 C02C  
 0E48 48F9 E700 00C0 C0F0  
 0E49 228F 00C0 00D0 0060  
 0E4A 48C9 0041 2030 C0F0  
 0E4B 000C 00C0 00C0 C02C  
 0E4C 4809 C040 003C 00F0  
 0E4D 78C9 00C0 00D0 0060  
 0E4E 1E70 0000 0000 0060  
 0E4F 4F1C 00C0 00D0 0060  
 0E50 4809 00C0 00C0 00F0  
 0E51 4809 0040 003C 00F0  
 0E52 2000 00C0 00D0 0060  
 0E53 4809 00C0 00C0 00F0  
 0E54 2E5C 0000 00D0 0060  
 0E55 56E0 00D0 00D0 C040

0PFC0E23: XFC00E - 1 = CFCR  
 A2 + AMPCR = AMPCR  
 0P23F - 1 = AMPCR  
 SIEP  
 EXEC

0P23F:

0E5B 1780 0000 0070 0040  
 0E5C 179C 00C0 00C0 C040  
 0E5D 300C 00C0 00C0 C040  
 0E5E 1740 0000 0070 C040

0P230:

0E5F 4809 2C55 00C0 C0FC  
 0E60 00F0 00C0 00C0 C0FC  
 0E61 51CC 00C0 00D0 0060  
 0E62 2E3C 00C0 00D0 0060  
 0E63 4809 0041 20C0 00F0  
 0E64 001C 00D0 00C0 C040  
 0E65 48C9 2F5C 001C C0F0  
 0E66 2F3C 00D0 00C0 0060  
 0E67 4809 C05C 003C 00F0  
 0E68 4809 E0C0 003C C0FC  
 0E69 30FC 00C0 00D0 C08C  
 0E6A 4809 2C55 00D0 00FC  
 0E6B 51CC C0D0 0070 0060  
 0E6C 48C9 C041 00C0 C0FC  
 0E6D 000C 00C0 00D0 003C  
 0E6E 2F3C 00C0 00D0 C060  
 0E6F 4809 C041 2070 00FC  
 0E70 0010 00C0 00D0 C040

X  
 X RX TYPE ADD, (R(A))+(Y) -> R(A)  
 X SET CC, CARRY, AND OV BITS  
 X Y INTO P

RAMFIELD - 1 = CPCR  
 B L = 0R2  
 COMP 8 = SAR  
 FHULIN - 1 = CPCR  
 B L = HIP  
 16 = SAR  
 A3 = B

CONTENTSRA - 1 = CPCR  
 P L = A2, BHI  
 COMP 16 = SAR  
 A2 + B = MIR  
 IF ADV THEN SET LCI  
 CARRY - 1 = CPCR  
 CHECKOV - 1 = CPCR

BHI = MIR, B  
 B R = SAR  
 16 SAR  
 COMP 16 = CPCR  
 INPUT - 1 = CPCR  
 0PFC00E - 1 = MPCC

X  
 X SET THE CONDITION BITSX  
 X \*F= INTO A2

X

04777C00 0  
 04771C00 0  
 04772C00 0  
 04773C00 0  
 04774C00 0  
 04775C00 0  
 04776C00 0  
 04777C00 0  
 04778C00 0  
 04779C00 0  
 04780C00 0  
 04781C00 0  
 04782C00 0  
 04783C00 0  
 04784C00 0  
 04785C00 0  
 04786C00 0  
 04787C00 0  
 04788C00 0  
 04789C00 0  
 04790C00 0  
 04791C00 0  
 04792C00 0  
 04793C00 0  
 04794C00 0  
 04795C00 0  
 04796C00 0  
 04797C00 0

X  
 X TYPE RR ADD DOUBLE, (R(A))+(R(A+1)) +  
 X (R(H))+(R(H+1)) INTO R(A),R(A+1)  
 X SET CC, CARRY AND OV BITS  
 X ISOLATE \*HX  
 X (R(H)) INTO B  
 X (R(H)) INTO MS WORD OF A2  
 X ADDR OF R(H+1)  
 X (R(H+1)) INTO B  
 X MIR = (R(H))/(R(H+1))X  
 X ISOLATE \*AX  
 X TEMP STORAGEX  
 X (R(A)) INTO B  
 X (R(A)) INTO MS WORD GF A2X  
 X LIT































OFA5 35CC 0000 0000 0000  
 OFA6 4809 E001 1000 0000  
 OFA7 0800 0000 0000 0000  
 OFA8 0000 0000 0000 0000  
 OFA9 2F50 0000 0000 0000  
 OFAA 56E0 0000 0000 0000

0P2611

CFAB 4809 CC40 8800 0000  
 CFAC 9CFC 0000 0000 0000  
 OFA0 4809 2C55 6800 0000  
 OFA1 31CC 0000 0000 0000  
 OFAF 4809 0F41 0000 0000  
 OFB0 90CC 0000 0000 0000  
 OFB1 4809 0F46 0000 0000  
 OFB2 51CC 0000 0000 0000  
 OFB3 2F30 0000 0000 0000  
 OFB4 4809 0C40 2000 0000  
 OFB5 4809 0E56 0000 0000  
 OFB6 0000 0000 0000 0000  
 OFB7 51CC 0000 0000 0000  
 OFB8 2F30 0000 0000 0000  
 OFB9 4809 0C41 0000 0000  
 OFBA 90CC 0000 0000 0000  
 OFBB 0000 0000 0000 0000  
 OFBC 4809 0F49 0000 0000  
 OFBD 2000 0000 0000 0000  
 OFBE 4809 E000 8000 0000  
 OFBF 0000 0000 0000 0000  
 OFC0 4809 0F47 8000 0000  
 OFC1 90CC 0000 0000 0000  
 OFC2 2F50 0000 0000 0000  
 OFC3 51CC 0000 0000 0000  
 OFC4 4809 0F45 0000 0000  
 OFC5 31CC 0000 0000 0000  
 OFC6 4809 E001 1000 0000  
 OFC7 90CC 0000 0000 0000  
 OFC8 2F50 0000 0000 0000  
 OFC9 4809 E000 8000 0000  
 OFCA 56E0 0000 0000 0000

0P2621

CFCC 4809 2C55 6800 0000  
 CFCE 4809 0C53 0000 0000  
 OFE0 4809 0C52 0000 0000  
 OFE1 2810 0000 0000 0000  
 OFE2 3100 0000 0000 0000  
 OFE3 4809 0C41 0000 0000  
 OFE4 00CC 0000 0000 0000  
 OFE5 4809 E000 8000 0000  
 OFE6 4809 E000 8000 0000  
 OFE7 4809 CC40 2000 0000  
 OFE8 4809 E000 8800 0000

REGSTACK - I = CPCR  
 X R(A+1) INTO MAR2  
 05156000 0  
 05159000 0  
 05160000 0  
 05161000 0  
 05162000 0  
 05163000 0  
 05164000 0  
 05165000 0  
 05166000 0  
 05167000 0  
 05168000 0  
 05169000 0  
 05170000 0  
 05171000 0  
 05172000 0  
 05173000 0  
 05174000 0  
 05175000 0  
 05176000 0  
 05177000 0  
 05178000 0  
 05179000 0  
 05180000 0  
 05181000 0  
 05182000 0  
 05183000 0  
 05184000 0  
 05185000 0  
 05186000 0  
 05187000 0  
 05188000 0  
 05189000 0  
 05190000 0  
 05191000 0  
 05192000 0  
 05193000 0  
 05194000 0  
 05195000 0  
 05196000 0  
 05197000 0  
 05198000 0  
 05199000 0  
 05200000 0  
 05201000 0  
 05202000 0  
 05203000 0  
 05204000 0  
 05205000 0  
 05206000 0  
 05207000 0  
 05208000 0  
 05209000 0  
 05210000 0  
 05211000 0  
 05212000 0  
 05213000 0  
 05214000 0  
 05215000 0  
 05216000 0  
 05217000 0

X BI TYPE 2 MULTIPLY (INDIRECT)  
 X (R(A+1)) X (Y\*) = R(A),R(A+1), SET CC

X ISOLATE \*A\*  
 X R(A)

X R(A+1) INTO MAR2  
 X (R(A+1)) INTO B  
 X ISOLATE \*M\*

X R(A) INTO MAR2  
 X Y\* INTO E

X (Y\*) INTO B  
 X MULTI (R(A+1)) X (Y\*)  
 X PRODUCT IN A3  
 X SET THE CONDITION BITS

X REF ERI  
 X R(A)

X R(A+1) INTO MAR2  
 X R(A+1)

X TYPE RK MULTIPLY (CONSTANT)  
 X (R(A+1)) X Y = R(A),R(A+1), SET CC  
 X ISOLATE \*M\*

X CHECK FOR H = 0  
 X (R(H)) INTO B

X A3 = (R(H))/INSTRUCTION  
 X \*Y\* INTO B  
 X (R(H)) INTO A2

X Y INTO B











1C40 31C0 00E9 0070 006C REGSTACK - 1 = CPCR  
 1C41 48C9 0F41 0020 0060 BMAR L = BRI  
 1C42 48C9 0F41 0020 0060 COMP 8 = SAR  
 1C43 2E3C 00C3 0030 0030 EMPTUT - 1 = CPCR  
 1C44 4809 0C41 2C00 0020 B L = A2  
 1C45 00CC 0000 0020 0020 COMP 16 = SAR  
 1C46 4809 0F46 0030 00F0 BMAR + 1 = B  
 1C47 31C0 00C3 0020 0060 REGSTACK - 1 = CPCR  
 1C48 2F3C 00C0 0030 0060 EMPTUT - 1 = CPCR  
 1C49 4809 0F5C 2E30 00F0 A2 DR 0 = A2  
 1C4A 4809 115 6 0030 00F0 A3 AND LIT = 0  
 1C4B 00F0 00C0 0030 0060 15 = LIT  
 1C4C 31C0 00C0 0030 0060 REGSTACK - 1 = CPCR  
 1C4D 2F3C 00C0 0030 0060 EMPTUT - 1 = CPCR  
 1C4E 4809 0C41 001C 00C0 B L = BR2  
 1C4F 000C 00C0 0030 0030 COMP 8 = SAR  
 1C50 50E0 00C0 0060 0060 EHULIN - 1 = CPCR  
 1C51 48C9 0C41 083C 00F0 B L = BJ SET LCI  
 1C52 000C 00C3 0020 0020 COMP 16 = SAR  
 1C53 240C 00C0 0020 0060 DIV - 1 = CPCR  
 1C54 20B8 00C0 0060 0060 IF LCI THEN SET LCI  
 1C55 50AC 0000 0060 0060 SETOVBIT - 1 = CPCR  
 1C56 2819 00C0 0030 0060 IF LCI THEN SKIP  
 1C57 5050 00C0 0060 0060 CLEAROV - 1 = CPCR  
 1C58 4809 0C00 003C 00FC A2 = MIR  
 1C59 2000 00C0 003C 00FC A3 = 0  
 1C5A 2000 00C0 003C 00FC ASRCCA - 1 = CPCA  
 1C5B 4809 0C00 0000 20FC REP BRI  
 1C5C 48C9 0E43 8E1C 00F0 BMAR R = MAR2  
 1C5D 300C 0700 0030 001C R = SAR  
 1C5E 2F5F 08C0 003C 006C EOUTPUT - 1 = CPCR  
 1C5F 4809 E0C3 0E30 00F0 A3 = MIR  
 1C60 48C9 0F46 0830 00F0 BMAR + 1 = B  
 1C61 31C0 0000 0030 0060 REGSTACK - 1 = CPCR  
 1C62 2F5C 00C0 0030 006C EOUTPUT - 1 = CPCR  
 1C63 66EC 00C3 0070 0040 OPCCODE - 1 = MPCR  
  
 1C64 4809 E156 0000 0060 A3 AND LIT = B  
 1C65 000C 0000 0000 00E0 15 = LIT  
 1C66 4809 0C52 00C0 00F0 0 EOL B  
 1C67 6819 00C0 0050 00F0 IF TRUE THEN SKIP  
 1C68 238C 00C3 0000 006C CONTENTSRM - 1 = CPCR  
 1C69 000C 0C41 083C 00FC B L = B  
 1C6A 4809 E05C 100C 0020 FEETCH = A3  
 1C6B 6330 00C3 0000 0060 A1 R = A2  
 1C6C 4809 0F0C 0020 00F0 16 = SAR  
 1C6D 0000 00C0 0020 0020 A2 + B = B  
 1C6E 4809 0C41 1030 00FC A3 L = A3  
 1C6F 4809 E0C3 1030 00FC A3 R = A3  
 1C70 4809 E0C3 1030 00FC A3 DR B = A3  
 1C71 4809 E0C3 1030 00FC A3 R = B  
 1C72 4809 E0C3 100C 00FC 4 = SAR, 15 = LIT  
 1C73 4809 E0C0 8B30 00FC LIT AND B = B  
 1C74 30FC 00C0 000C 0080 REGSTACK - 1 = CPCR  
 1C75 4809 2C55 0000 00F0  
 1C76 31C0 00C3 0030 0060

OP272:

02338C0C D X TEMP STORAGE  
 05339000 C X (R(A)) INTO B  
 05340000 C X (R(A)) INTO B  
 05341000 D X R(A+1)  
 05342000 D X R(A+1) INTO MAR2  
 05343000 D X (R(A+1)) INTO B  
 05344000 D X (R(A+1)) INTO B  
 05345000 D X ISOLATE \*M\*  
 05346000 D X Y\* INTO E  
 05347000 D X (Y\*) INTO B  
 05348000 C X LEFT JUSTIFY (Y\*)  
 05349000 D X (R(A))R(A+1)/(Y\*)  
 05350000 D X (R(A))R(A+1)/(Y\*)  
 05351000 D X (R(A))R(A+1)/(Y\*)  
 05352000 D X (R(A))R(A+1)/(Y\*)  
 05353000 C X (R(A))R(A+1)/(Y\*)  
 05354000 C X (R(A))R(A+1)/(Y\*)  
 05355000 C X (R(A))R(A+1)/(Y\*)  
 05356000 D X (R(A))R(A+1)/(Y\*)  
 05357000 D X (R(A))R(A+1)/(Y\*)  
 05358000 D X (R(A))R(A+1)/(Y\*)  
 05359000 C X (R(A))R(A+1)/(Y\*)  
 05360000 D X (R(A))R(A+1)/(Y\*)  
 05361000 D X (R(A))R(A+1)/(Y\*)  
 05362000 D X (R(A))R(A+1)/(Y\*)  
 05363000 D X (R(A))R(A+1)/(Y\*)  
 05364000 D X (R(A))R(A+1)/(Y\*)  
 05365000 D X (R(A))R(A+1)/(Y\*)  
 05366000 D X (R(A))R(A+1)/(Y\*)  
 05367000 D X (R(A))R(A+1)/(Y\*)  
 05368000 D X (R(A))R(A+1)/(Y\*)  
 05369000 D X (R(A))R(A+1)/(Y\*)  
 05370000 D X (R(A))R(A+1)/(Y\*)  
 05371000 D X (R(A))R(A+1)/(Y\*)  
 05372000 D X (R(A))R(A+1)/(Y\*)  
 05373000 D X (R(A))R(A+1)/(Y\*)  
 05374000 D X (R(A))R(A+1)/(Y\*)  
 05375000 D X (R(A))R(A+1)/(Y\*)  
 05376000 D X (R(A))R(A+1)/(Y\*)  
 05377000 D X (R(A))R(A+1)/(Y\*)  
 05378000 D X (R(A))R(A+1)/(Y\*)  
 05379000 D X (R(A))R(A+1)/(Y\*)  
 05380000 D X (R(A))R(A+1)/(Y\*)  
 05381000 D X (R(A))R(A+1)/(Y\*)  
 05382000 D X (R(A))R(A+1)/(Y\*)  
 05383000 D X (R(A))R(A+1)/(Y\*)  
 05384000 D X (R(A))R(A+1)/(Y\*)  
 05385000 D X (R(A))R(A+1)/(Y\*)  
 05386000 D X (R(A))R(A+1)/(Y\*)  
 05387000 D X (R(A))R(A+1)/(Y\*)  
 05388000 D X (R(A))R(A+1)/(Y\*)  
 05389000 D X (R(A))R(A+1)/(Y\*)  
 05390000 D X (R(A))R(A+1)/(Y\*)  
 05391000 D X (R(A))R(A+1)/(Y\*)  
 05392000 D X (R(A))R(A+1)/(Y\*)  
 05393000 D X (R(A))R(A+1)/(Y\*)  
 05394000 D X (R(A))R(A+1)/(Y\*)  
 05395000 D X (R(A))R(A+1)/(Y\*)  
 05396000 D X (R(A))R(A+1)/(Y\*)  
 05397000 D X (R(A))R(A+1)/(Y\*)









```

ICAF 4809 C0C0 0030 20FC
ICB0 4809 0F30 081C 00F0
ICB1 0000 0000 0000 0010
ICB2 2F5C 00C0 0C30 0060
ICB3 4809 0F45 0B30 00F0
ICB4 51C0 00C0 0030 0060
ICB5 4809 E0D3 0F30 00FC
ICB6 2F50 00C0 00C0 0060
ICB7 56E0 00C0 0030 0040

10B8 5F9C C0C0 003C 0C60
10B9 4809 6C40 0040 00F0
10BA 18EC C0C0 007C C0CC
10BB 4809 0000 0000 00FC
10BC 4824 00C0 0050 00FC

10BD 18FC 00C0 003C 0040
10BE 190C 0000 007C C040
10BF 191C 00C0 009C 004C
11C0 1920 00C0 0C00 0040

10C1 228C C000 0070 0060
10C2 4809 0C40 0030 00FC
10C3 2380 00C0 0080 006C
10C4 4809 0C40 2030 00FC
10C5 4809 C036 001C 00FC
10C6 000C 0040 0050 0020
10C8 2F50 0000 0000 006C
10C9 20D0 0000 0000 006C
11CA 66E0 C0C0 003C 0040

10CB 238C 00C0 0070 006C
10CC 48F9 6C41 001C 00FC
10CD 00C0 00C0 0070 0030
10CE 60EC 00C0 0030 0060
10CF 48C9 6C40 003C 00FC
10D0 4809 E0F3 0B00 00FC
10D1 2280 00C0 007C 0060
10D2 48C9 0C40 2000 00FC
10D3 4809 C056 0030 00FC
10D4 2F5C 00C0 0000 0060
10D5 20D0 00C0 003C 006C
10D6 56E0 60C0 0030 0040

10D7 4809 2C56 003C 00FC
10D8 00FC C0C 003C 00FC
10D9 4809 6C52 0C30 00FC
10DA 6819 00C0 0030 00FC
10DB 238C 0000 0C30 006C

OP000E30:  %FCODE - 1 = CPCR
           A2 = MIR, ASR
           DMAR R = MARZ
           B = SAR
           EUIPUT - 1 = CPCR
           DMARSHR - 1 = B
           DMARSHR - 1 = CPCR
           A2 = MIR, ASR
           EUIPUT - 1 = CPCR
           OPCODE - 1 = MPCCR

OP30F1:   %FCODE - 1 = MPCCR
           OP301 - 1 = FPCR
           OP302 - 1 = MPCCR
           OP303 - 1 = MPCCR

OP30C1:   %TYPE RR AND (REGISTER)
           % (CRCA) AND (CRHS) = R(A), SET CC
           B = MIR AND B = B
           CONTENTSRA - 1 = CPCR
           CONTENTSRM - 1 = CPCR
           B = A2, DMAR, P
           A3 = DMAR
           A3 = DMAR
           A3 = SAR
           EUIPUT - 1 = CPCR
           SEICCA - 1 = CPCR
           OPCODE - 1 = MPCCR

OP301:    %PI TYPE 2 AND (INDIRECT)
           % (R(A)) AND (Y*) = R(A), SET CC
           B L = BR2
           COMP B = SAR
           ENULIN - 1 = CPCR
           B = MIR
           A3 = B
           CONTENTSRA - 1 = CPCR
           A2 AND B = MIR, B
           EUIPUT - 1 = CPCR
           SEICCA - 1 = CPCR
           OPCODE - 1 = MPCCR

OP302:    %TYPE RK AND (CONSTANT)
           % (R(A)) AND (Y) = R(A), SFT CC
           LIT AND B = B
           B = LIT
           C = LIT
           IF TRUE THEN SKIP
           CONTENTSRM - 1 = CPCR
           % (RHS) INTO 9

```













```

1134 19A0 00C0 C0C0 C040
1135 19B0 00D0 00D0 C040
113C 19C0 00C0 00C0 C040

1130 2280 C0C0 00D0 0060
113E 3809 0C40 00F0 0060
113F 2380 00D0 00C0 0060
1140 4809 0C40 20D0 00F0
1141 4809 0C40 0040 00F0
1142 4809 00D0 8010 00F0
1143 00C0 00C0 00D0 0020
1144 2F50 00D0 00D0 0060
1145 20D0 00C0 00D0 0060
1146 56E0 00D0 00D0 0040

```

0P320:

```

CONTENISRA - 1 = CPCR
B = MIR
CONTENISRM - 1 = CPCR
B = A2, BHI
A2 XOR B = MIR, F
A3 R = MAR2
16 = SAR
EUIPUT - 1 = CPCR
SETCCA - 1 = CPCR
DFCODE - 1 = MPCR

```

0P321:

```

CONTENISRM - 1 = CPCR
B = BHE
COMP - 1 = SAR
FNULLIN - 1 = CPCR
B = MIR
A3 = B
CONTENISRA - 1 = CPCR
B = A2, BHI
A2 XOR B = MIR, F
EUIPUT - 1 = CPCR
SETCCA - 1 = CPCR
DFCODE - 1 = MPCR

```

0P322:

```

LIT AND B = B
15 = LIT
IF TRUE THEN SKIP
CONTENISRM - 1 = CPCR
B LL = B
COMP 16 = SAR
A3 OR B = A3
IFETCH - 1 = CPCR
13 R = SAR, 15 = LIT
A2 + B = MIR
A3 = B
CONTENISRA - 1 = CPCR
B = A2, BHI
A2 XOR B = MIR, F
EUIPUT - 1 = CPCR
SETCCA - 1 = CPCR
DFCODE - 1 = MPCR

```

0P323:

```

LIT AND B = B
15 = LIT
IF TRUE THEN SKIP
CONTENISRM - 1 = CPCR
B LL = B
COMP 16 = SAR
A3 OR B = A3
IFETCH - 1 = CPCR
13 R = SAR, 15 = LIT
A2 + B = MIR
A3 = B
CONTENISRA - 1 = CPCR
B = A2, BHI
A2 XOR B = MIR, F
EUIPUT - 1 = CPCR
SETCCA - 1 = CPCR
DFCODE - 1 = MPCR

```

```

05639C00 0
05640C00 0
05641C00 0
05642C00 0
05643C00 0
05644C00 0
05645C00 0
05646C00 0
05647C00 0
05648C00 0
05649C00 0
05650C00 0
05651C00 0
05652C00 0
05653C00 0
05654C00 0
05655C00 0
05656C00 0
05657C00 0
05658C00 0
05659C00 0
05660C00 0
05661C00 0
05662C00 0
05663C00 0
05664C00 0
05665C00 0
05666C00 0
05667C00 0
05668C00 0
05669C00 0
05670C00 0
05671C00 0
05672C00 0
05673C00 0
05674C00 0
05675C00 0
05676C00 0
05677C00 0
05678C00 0
05679C00 0
05680C00 0
05681C00 0
05682C00 0
05683C00 0
05684C00 0
05685C00 0
05686C00 0
05687C00 0
05688C00 0
05689C00 0
05690C00 0
05691C00 0
05692C00 0
05693C00 0
05694C00 0
05695C00 0
05696C00 0
05697C00 0

```

```

X
X RR TYPE EXCLUSIVE OR (REGISTER)
X (R(A)) XOR (R(M)) = R(A), SET CC
X (R(A)) INTO B
X (R(M)) INTO B
X R(A)
X SET THE CONDITION BITS
X
X RI TYPE 2 EXCLUSIVE OR (INDIRECT)
X (R(A)) XOR (Y) = R(A), SET (C
X Y) INTO B
X (Y) INTO B
X (R(A)) INTO B
X SET THE CONDITION BITS
X
X RK TYPE EXCLUSIVE OR (CONSTANT)
X (R(A)) XOR Y = R(A), SET CC
X ISOLATE "H"
X CHECK FOR H = 0
X (R(M)) INTO B
X A3 = (R(I))/INSTRUCTION
X *P* INTO B
X Y INTO MIR
X (R(A)) INTO B
X
X RX TYPE EXCLUSIVE OR
X (R(A)) XOR (Y) = R(A), SET CC

```

















11FC 238C 00F0 00C0 0060 0060  
 11FD 4809 0C41 001E 00FD  
 11FE 0000 0C40 003E 0030  
 11FF 50EC 00F0 0050 0060  
 1200 4809 0C40 0050 007C  
 1201 4809 0E00 8800 0040  
 1202 80F0 0000 8000 0060  
 1203 4809 2E56 0070 00FC  
 1204 4809 0000 0000 0060  
 1205 2E30 0060 0070 0060  
 1206 4809 0C40 2070 00E0  
 1207 4809 0F45 0030 00E0  
 1208 51CC 0000 0000 0060  
 1209 2E3C 0F00 0000 0060  
 120A 4609 0C56 2020 00FC  
 120B 4809 0C40 1070 00FC  
 120C 4809 0E56 0030 00FC  
 120D 2000 00C0 00C0 0060  
 120E 64E0 0C60 00C0 0040

120F 4809 2E56 00D0 00FC  
 1210 00F0 0000 0000 00EC  
 1211 4809 0C52 0000 00FC  
 1212 6819 0000 0050 00FC  
 1213 238C 0000 0050 006C  
 1214 4809 0C41 0050 0070  
 1215 0000 00C0 00C0 0020  
 1216 4809 0EC0 1070 00FC  
 1217 4809 0000 0000 0060  
 1218 4809 0000 0000 0060  
 1219 0000 00C0 0000 0020  
 121A 4809 0C40 0030 00E0  
 121B 4809 0E00 8800 00FC  
 121C 30FC 0500 0020 0080  
 121D 4809 2E56 0020 00FC  
 121E 51CC 00C0 0000 006C  
 121F 2E30 00C0 0000 006C  
 1220 4809 0C40 2070 00FC  
 1221 4809 0F45 0030 00FC  
 1222 51CC 00C0 0030 0060  
 1223 2F30 00C0 0070 0060  
 1224 4809 0C56 2020 00FC  
 1225 4809 0C40 1070 00FC  
 1226 4809 0E56 0030 00FC  
 1227 2000 00C0 0000 0060  
 1228 66E0 00F0 0030 0040

1229 570C 0000 0020 006C  
 122A 4809 0C40 001E 00FD  
 122B 0000 00C0 0050 0030  
 122C 60E0 00C0 0000 006C  
 122D 4809 0C40 0000 00FC

0342:  
 CONTESTSRM - I = CPCR  
 BL = BR2  
 COMP 8 = SAR  
 EHLIN - I = CPCR  
 P = MIR  
 A3 R = B  
 4 = SAR, 15 = LIT  
 LIT AND B = B  
 REGSTACK - I = CPCR  
 EHLIN - I = CPCR  
 P = A3, BHI  
 A3 AND B = 0  
 SETFC - I = CPCR  
 OPCODE - I = MPCR  
 LIT AND B = B  
 15 = LIT  
 0 EOL B  
 IF TRUE THEN SKIF  
 CONTESTSRM - I = CPCR  
 BL = 0  
 COMP 16 = SAR  
 A3 OR B = A3  
 IFEICH - I = CPCR  
 A3 R = SAR  
 A3 = SAR  
 A3 R = B  
 A3 R = B  
 4 = SAR, 15 = LIT  
 LIT AND B = B  
 REGSTACK - I = CPCR  
 EHLIN - I = CPCR  
 P = A3, BHI  
 A3 AND B = B  
 SETFC - I = CPCR  
 OPCODE - I = MPCR  
 RANFIELD - I = CPCR  
 COMP = BR2  
 EHLIN - I = CPCR  
 P = MIR

0343:  
 CONTESTSRM - I = CPCR  
 BL = BR2  
 COMP 8 = SAR  
 EHLIN - I = CPCR  
 P = MIR  
 A3 R = B  
 4 = SAR, 15 = LIT  
 LIT AND B = B  
 REGSTACK - I = CPCR  
 EHLIN - I = CPCR  
 P = A3, BHI  
 A3 AND B = B  
 SETFC - I = CPCR  
 OPCODE - I = MPCR  
 LIT AND B = B  
 15 = LIT  
 0 EOL B  
 IF TRUE THEN SKIF  
 CONTESTSRM - I = CPCR  
 BL = 0  
 COMP 16 = SAR  
 A3 OR B = A3  
 IFEICH - I = CPCR  
 A3 R = SAR  
 A3 = SAR  
 A3 R = B  
 A3 R = B  
 4 = SAR, 15 = LIT  
 LIT AND B = B  
 REGSTACK - I = CPCR  
 EHLIN - I = CPCR  
 P = A3, BHI  
 A3 AND B = B  
 SETFC - I = CPCR  
 OPCODE - I = MPCR  
 RANFIELD - I = CPCR  
 COMP = BR2  
 EHLIN - I = CPCR  
 P = MIR

05878C00 U  
 05879C00 U  
 05880C00 U  
 05881C00 U  
 05882C00 U  
 05883C00 U  
 05884C00 U  
 05885C00 U  
 05886C00 U  
 05887C00 U  
 05888C00 U  
 05889C00 U  
 05890C00 U  
 05891C00 U  
 05892C00 U  
 05893C00 U  
 05894C00 U  
 05895C00 U  
 05896C00 U  
 05897C00 U  
 05898C00 U  
 05899C00 U  
 05900C00 U  
 05901C00 U  
 05902C00 U  
 05903C00 U  
 05904C00 U  
 05905C00 U  
 05906C00 U  
 05907C00 U  
 05908C00 U  
 05909C00 U  
 05910C00 U  
 05911C00 U  
 05912C00 U  
 05913C00 U  
 05914C00 U  
 05915C00 U  
 05916C00 U  
 05917C00 U  
 05918C00 U  
 05919C00 U  
 05920C00 U  
 05921C00 U  
 05922C00 U  
 05923C00 U  
 05924C00 U  
 05925C00 U  
 05926C00 U  
 05927C00 U  
 05928C00 U  
 05929C00 U  
 05930C00 U  
 05931C00 U  
 05932C00 U  
 05933C00 U  
 05934C00 U  
 05935C00 U  
 05936C00 U  
 05937C00 U

X (Y\*) INTO B  
 X (Y\*) INTO B  
 X TEMP STORAGE  
 X ISOLATE \*A\*  
 X (R(A)) INTO E  
 X (R(A+1))  
 X (R(A+1)) INTO HAR2  
 X (R(A+1)) INTO B  
 X (R(A)) AND (R(A+1))  
 X (Y\*) AND (R(A+1))  
 X SET THE CONDITION BITS  
 X  
 X  
 X TYPE BK COMPARE MASKED ((CONSTANT)  
 X (R(A)) AND (R(A+1)) ; Y AND (R(A+1))  
 X AND SET CONDITION BITS  
 X ISOLATE M  
 X CHECK FOR M = 0  
 X (R(H)) INTO B  
 X A3 = (R(H))/INSTRUCTION  
 X \*Y\* INTO B  
 X (R(H)) INTO A2  
 X Y INTO D  
 X ISOLATE \*A\*  
 X (R(A)) INTO HAR2  
 X (R(A)) INTO E  
 X (R(A+1))  
 X (R(A+1)) INTO HAR2  
 X (R(A+1)) INTO B  
 X (R(A)) AND (R(A+1))  
 X Y AND (R(A+1))  
 X SET THE CONDITION BITS  
 X  
 X  
 X PX TYPE COMPARE MASKED  
 X (R(A)) AND (R(A+1)) ; (Y) AND (R(A+1))  
 X AND SET CONDITION BITS  
 X Y INTO D  
 X (Y) INTO B  
 X TEMP STORAGE







05998100 U  
05999100 U  
06000100 U  
06001100 U  
06002100 U  
06003100 U  
06004100 U  
06005100 U  
06006100 U  
06007100 U  
06008100 U  
06009100 U  
06010100 U  
06011100 U  
06012100 U  
06013100 U  
06014100 U  
06015100 U  
06016100 U  
06017100 U  
06018100 U  
06019100 U  
06020100 U  
06021100 U  
06022100 U  
06023100 U  
06024100 U  
06025100 U  
06026100 U  
06027100 U  
06028100 U  
06029100 U  
06030100 U  
06031100 U  
06032100 U  
06033100 U  
06034100 U  
06035100 U  
06036100 U  
06037100 U  
06038100 U  
06039100 U  
06040100 U  
06041100 U  
06042100 U  
06043100 U  
06044100 U  
06045100 U  
06046100 U  
06047100 U  
06048100 U  
06049100 U  
06050100 U  
06051100 U  
06052100 U  
06053100 U  
06054100 U  
06055100 U  
06056100 U  
06057100 U

COMP 0 = SAR  
EMULIN - 1 = CPCR  
C L = B, A3  
COMP 16 = SAR  
IF NOT M5T THEN STEP ELSE SKIP  
P351 - 1 = MPCR  
SET11 - 1 = MPCR  
L L = B  
COMP 30 = SAR  
A3 OR B R = MIR, D  
16 = SAR  
RHAR L = BR2  
COMP 8 = SAR  
EMULOUT - 1 = MPCR  
OPCODE - 1 = MPCR  
A1 C = A1+C+SAR  
25 = SAR  
A1 AND B110 C = A1  
B C = B  
30 = SAR  
LIT OR B C = MIR  
J = LIT, B = SAR  
RHAR L = BR2  
COMP 8 = SAR  
EMULOUT - 1 = CPCR  
OPCODE - 1 = MPCR  
LIT AND P = B  
15 = LIT  
O EOL B  
IF TRUE THEN SKIP  
CONTENTSRM - 1 = CPCR  
P L = B  
COMP 16 = SAR  
A3 OR B = A3  
IFETCH - 1 = CPCR  
A3 R = A2  
PSW = LIT# 16 = SAR  
A2 + B = MIR  
LIT = HAR2  
EMULPUT - 1 = CPCR  
A1 OR B10 C = A1  
OPCODE - 1 = MPCR  
RYMFIELD - 1 = CPCR  
B L = BR2, A3  
COMP 8 = SAR  
EMULIN - 1 = CPCR  
B L = B  
COMP 16 = SAR  
IF NOT M5T THEN STEP ELSE SKIP  
P353 - 1 = MPCR

125E 300P 0000 0000 0000  
125F 500E 0000 0000 0000  
1260 0000 0000 0000 0000  
1262 4009 0000 0000 0000  
1263 4009 0000 0000 0000  
1264 1A0C 0000 0000 0000  
1265 216F 0000 0000 0000  
1266 4809 0000 0000 0000  
1267 200C 0000 0000 0000  
1268 4809 0000 0000 0000  
1269 4809 0000 0000 0000  
126A 4809 0000 0000 0000  
126B 4809 0000 0000 0000  
126C 4809 0000 0000 0000  
126D 4809 0000 0000 0000  
126E 4809 0000 0000 0000  
126F 4809 0000 0000 0000  
1270 4809 0000 0000 0000  
1271 4809 0000 0000 0000  
1272 4809 0000 0000 0000  
1273 4809 0000 0000 0000  
1274 4809 0000 0000 0000  
1275 4809 0000 0000 0000  
1276 4809 0000 0000 0000  
1277 4809 0000 0000 0000  
1278 4809 0000 0000 0000  
1279 4809 0000 0000 0000  
127A 4809 0000 0000 0000  
127B 4809 0000 0000 0000  
127C 4809 0000 0000 0000  
127D 4809 0000 0000 0000  
127E 4809 0000 0000 0000  
127F 4809 0000 0000 0000  
1280 4809 0000 0000 0000  
1281 4809 0000 0000 0000  
1282 4809 0000 0000 0000  
1283 4809 0000 0000 0000  
1284 4809 0000 0000 0000  
1285 4809 0000 0000 0000  
1286 4809 0000 0000 0000  
1287 4809 0000 0000 0000  
1288 4809 0000 0000 0000  
1289 570C 0000 0000 0000  
128A 4809 0000 0000 0000  
128B 4809 0000 0000 0000  
128C 4809 0000 0000 0000  
128D 4809 0000 0000 0000  
128E 4809 0000 0000 0000  
128F 4809 0000 0000 0000  
1290 4809 0000 0000 0000  
1291 1A0C 0000 0000 0000

0352:  
LIT AND P = B  
15 = LIT  
O EOL B  
IF TRUE THEN SKIP  
CONTENTSRM - 1 = CPCR  
P L = B  
COMP 16 = SAR  
A3 OR B = A3  
IFETCH - 1 = CPCR  
A3 R = A2  
PSW = LIT# 16 = SAR  
A2 + B = MIR  
LIT = HAR2  
EMULPUT - 1 = CPCR  
A1 OR B10 C = A1  
OPCODE - 1 = MPCR

0353:  
RYMFIELD - 1 = CPCR  
B L = BR2, A3  
COMP 8 = SAR  
EMULIN - 1 = CPCR  
B L = B  
COMP 16 = SAR  
IF NOT M5T THEN STEP ELSE SKIP  
P353 - 1 = MPCR

1279 4809 2C55 0B70 0000  
127A 00F0 0000 0000 0000  
127B 4809 0000 0000 0000  
127C 5819 0000 0000 0000  
127D 238C 0000 0000 0000  
127E 4809 0000 0000 0000  
127F 4809 0000 0000 0000  
1280 4809 0000 0000 0000  
1281 533C 0000 0000 0000  
1282 4809 0000 0000 0000  
1283 4809 0000 0000 0000  
1284 4809 0000 0000 0000  
1285 4809 0000 0000 0000  
1286 4809 0000 0000 0000  
1287 4809 0000 0000 0000  
1288 56E0 0000 0000 0000  
1289 4809 2C55 0B70 0000  
128A 00F0 0000 0000 0000  
128B 4809 0000 0000 0000  
128C 5819 0000 0000 0000  
128D 238C 0000 0000 0000  
128E 4809 0000 0000 0000  
128F 4809 0000 0000 0000  
1290 4809 0000 0000 0000  
1291 533C 0000 0000 0000



```

1292 216F 00E0 0000 C060
1293 4809 00C1 2000 C0FF
1294 200F 0000 00C0 C0FF
1295 200F 0000 00C0 0000
1296 4809 C5C0 803F C0F0
1297 0000 0000 003F 0020
1298 4809 00C0 003F 0020
1299 61E0 0000 0000 C060
129A 4809 0000 0000 0040
129B 4809 A0C1 C000 00F0
129C 4809 00C0 0000 003E
129D 4809 00C0 0000 003E
129E 4809 00C1 803F 00F0
129F AC0C 0000 00C0 C030
129G 4809 2050 8190 00F0
12A0 2030 C0C0 0000 C040
12A1 4809 E0C0 C61C 00F0
12A2 61E0 0000 0000 C060
12A3 66E0 0000 0000 C040

1248 3000 00C0 00C0 0640

1245 4E5C 0000 00C0 0040

OPCODE401:
1246 5F00 00C0 0000 006C
1247 4809 00C0 0000 006C
1248 6806 00C0 0000 00F0
1249 1AEC 0000 0000 0040
124A 4809 0040 8000 00C0
124B 90FC 0000 0000 C080
124C 4809 205E 2000 00F0
124D 4809 205E 2000 00F0
124E 0000 0000 0000 C0E0
124F 7819 0000 0000 0040
1250 30C0 0000 0000 0040
1251 4809 C640 00C0 00F0
1252 1AFC 00C0 0000 C0C0
1253 4809 0000 0000 0000
1254 4824 0000 0000 00F0

JUMP4C:
1255 1000 0000 0000 0040
1256 181F 0000 0000 0040
1257 1830 0000 0000 0040
1258 1830 0000 0000 0040
1259 1840 0000 0000 0040
125A 1850 0000 0000 0040
125B 4E5C 0000 0000 0040
125C 4E5C 0000 0000 0040
125D 185C 00C0 0000 0040
125E 186C 00C0 0000 0040
125F 1860 00C0 0000 0040
1260 1890 0000 0000 0040

12C1 226C 0000 0000 0060

```

```

% SET THE CONDITION BITS
% SET BIT 14 OF (Y)
% RESTORE Y INTO BR2
% PUT CC DIT 9 INTO LS BIT
% SET BIT 9 TO 0, AND RESTORE A1
% SET (Y) BIT 14,15
% RESTORE Y INTO BR2
% NOT ASSIGNED, GENERATES INTERRUPT
% FAULT
% JUMP TO FAULT HANDLING ROUTINE
% NOT IMPLEMENTED
% THIS ROUTINE ANALYZES THE 4th OPCODE
% IF FIELD RETURNED IN A2
% SPECIAL CASE #01
% ISOLATE THE 14th FIELD
% B AND A2 = 14th FIELD
% TEST FOR NOT ASSIGNED INST.
% CC INDICATES = 0F 01 JUMP EQUAL
% CC RETURNED IN B

```





```

0 EDI B
IF FALSE THEN SET LCI
OP40X - I = MPCR

0P40X01: CHECKCC - I = CPCR
        D GTR 0
        IF FALSE THEN SET LCI
        OP40X - I = MPCR

0P40X02: CHECKCC - I = CPCR
        LIT GE0 B
        2 = LIT
        IF FALSE THEN SET LCI
        OP40X - I = MPCR

0P40X03: CHECKCC - I = CPCR
        LIT EDL E
        3 = LIT
        IF FALSE THEN SET LCI
        OP40X - I = MPCR

0P40X04: A1 R = A2
        27 = SAR
        A2
        IF NOT LET THEN SET LCI
        OP40X - I = MPCR

0P40X05: A1 R = A2
        2 = SAR
        A2
        IF NOT LET THEN SET LCI
        OP40X - I = MPCR

0P40X10: OP40X - I = MPCR

0P40X11: WAIT
        STEP
        OP40X - I = MPCR

0P40X12: A1 R = A2
        29 = SAR
        A2
        IF NOT LET THEN SET LCI ELSE SKIP
        OP40X - I = MPCR
        WAIT
        STEP
        OP40X - I = MPCR

0P40X13: A1 R = A2
        30 = SAR
        A2

```

```

06118C00 0
C6119C00 0
C6120C00 0
06121C00 0
06122C00 0
06123C00 0
06124C00 0
06125C00 0
06126C00 0
06127C00 0
06128C00 0
06129C00 0
06130C00 0
06131C00 0
06132C00 0
06133C00 0
06134C00 0
06135C00 0
06136C00 0
06137C00 0
06138C00 0
06139C00 0
06140C00 0
06141C00 0
06142C00 0
06143C00 0
06144C00 0
C6145C00 0
06146C00 0
06147C00 0
C6148C00 0
06149C00 0
C6150C00 0
06151C00 0
06152C00 0
06153C00 0
06154C00 0
06155C00 0
06156C00 0
06157C00 0
C6158C00 0
06159C00 0
06160C00 0
06161C00 0
06162C00 0
06163C00 0
06164C00 0
06165C00 0
06166C00 0
06167C00 0
06168C00 0
06169C00 0
06170C00 0
06171C00 0
06172C00 0
06173C00 0
06174C00 0
06175C00 0
06176C00 0
06177C00 0

```



```

126C 5100 07C0 000C 00F0 06179600 D
126D 5019 0000 0000 00F0 06187600 D
126E 1040 07C0 06C0 0040 06191600 D
126F 4800 00F0 07FF 00F0 06191600 D
1270 4809 00C0 0000 00F0 06182700 D
1271 105C 00C0 0000 0040 06183C00 D
1272 5F90 09C0 0000 0060 06184900 D
1273 4369 0640 0040 00FC 06185500 D
1274 1C6F 00C0 0000 00C0 06186600 C
1275 4809 00C0 0000 00F0 06187600 D
1276 4024 00F0 0000 00F0 06188600 D
1277 1C7C 0000 0000 0040 06189600 D
1278 3000 0000 0000 0040 06190000 F
1279 1C8C 0000 0000 0040 06191400 C
127A 1C90 0000 0000 0040 06192000 C
127B 1C96 0000 0000 0040 06193000 D
127C 2800 0000 0000 00F0 06194700 D
127D 4669 0152 0000 0040 06195000 D
127E 007C 0000 0000 00C0 06196600 D
127F 5100 0000 0000 0060 06200000 D
1280 2F3C 0000 0000 0060 06201000 D
1281 4809 0000 0000 00FC 06202000 D
1282 0C00 0000 0000 00F0 06203000 D
1283 4809 0000 0000 00F0 06204000 D
1284 4809 AC5C 4030 00F0 06205000 D
1285 566E 0000 0000 0040 06206000 D
1286 260B 09C0 0000 00F0 06207000 D
1287 1D3C 00C0 0000 0040 06208000 D
1288 4809 E155 0000 00F0 06209000 D
1289 00FF 00C0 0000 00E0 06210000 D
1290 4809 0052 0000 00F0 06211000 C
1291 5A89 00C0 0000 00FC 06212000 D
1292 5100 00C0 0000 0060 06213000 C
1293 0200 0000 0000 00C0 06214000 D
1294 4809 0000 0000 00FC 06215000 D
1295 1D30 0000 0000 0040 06216000 D
1296 4809 E400 0000 00FC 06217000 D
1297 4809 A0D0 0000 00F0 06218000 D
1298 0000 0000 0000 0020 06219000 D
1299 4809 A001 4030 00FC 06220000 D
1300 4809 AC5C 4030 00FC 06221000 D
1301 566E 00C0 0000 0040 06222000 D
1302 1D30 0000 0000 0040 06223000 D
1303 4809 E400 0000 00FC 06224000 D
1304 4809 C041 0000 00F0 06225000 D
1305 4809 C000 0000 0060 06226000 D
1306 570C 00C0 0000 0060 06227000 D
1307 4809 C041 0000 00F0 06228000 D
1308 0000 0000 0000 0030 06229000 D
1309 50E0 00C0 0000 0060 06230000 D
1310 4809 A0C0 0000 00FC 06231000 D
1311 4809 A0C0 0000 00FC 06232000 D
1312 50E0 00C0 0000 0060 06233000 D
1313 4809 A0C0 0000 00FC 06234000 D
1314 4809 A0C0 0000 00FC 06235000 D
1315 50E0 00C0 0000 0060 06236000 D
1316 4809 A0C0 0000 00FC 06237000 D
1317 4809 AC5C 4030 00FC 06238000 D
1318 566E 00C0 0000 0040 06239000 D
1319 570C 00C0 0000 0060 06240000 D
1320 4809 C041 0000 00F0 06241000 D
1321 0000 0000 0000 0030 06242000 D
1322 50E0 00C0 0000 0060 06243000 D
1323 4809 A0C0 0000 00FC 06244000 D
1324 4809 A0C0 0000 00FC 06245000 D
1325 50E0 00C0 0000 0060 06246000 D
1326 4809 A0C0 0000 00FC 06247000 D
1327 4809 A0C0 0000 00FC 06248000 D
1328 50E0 00C0 0000 0060 06249000 D
1329 4809 A0C0 0000 00FC 06250000 D
1330 4809 A0C0 0000 00FC 06251000 D
1331 50E0 00C0 0000 0060 06252000 D
1332 4809 A0C0 0000 00FC 06253000 D
1333 4809 A0C0 0000 00FC 06254000 D
1334 50E0 00C0 0000 0060 06255000 D
1335 4809 A0C0 0000 00FC 06256000 D
1336 4809 A0C0 0000 00FC 06257000 D
1337 50E0 00C0 0000 0060 06258000 D
1338 4809 A0C0 0000 00FC 06259000 D
1339 4809 A0C0 0000 00FC 06260000 D
1340 50E0 00C0 0000 0060 06261000 D
1341 4809 A0C0 0000 00FC 06262000 D
1342 4809 A0C0 0000 00FC 06263000 D
1343 50E0 00C0 0000 0060 06264000 D
1344 4809 A0C0 0000 00FC 06265000 D
1345 4809 A0C0 0000 00FC 06266000 D
1346 50E0 00C0 0000 0060 06267000 D
1347 4809 A0C0 0000 00FC 06268000 D
1348 4809 A0C0 0000 00FC 06269000 D
1349 50E0 00C0 0000 0060 06270000 D
1350 4809 A0C0 0000 00FC 06271000 D
1351 4809 A0C0 0000 00FC 06272000 D
1352 50E0 00C0 0000 0060 06273000 D
1353 4809 A0C0 0000 00FC 06274000 D
1354 4809 A0C0 0000 00FC 06275000 D
1355 50E0 00C0 0000 0060 06276000 D
1356 4809 A0C0 0000 00FC 06277000 D
1357 4809 A0C0 0000 00FC 06278000 D
1358 50E0 00C0 0000 0060 06279000 D
1359 4809 A0C0 0000 00FC 06280000 D
1360 4809 A0C0 0000 00FC 06281000 D
1361 50E0 00C0 0000 0060 06282000 D
1362 4809 A0C0 0000 00FC 06283000 D
1363 4809 A0C0 0000 00FC 06284000 D
1364 50E0 00C0 0000 0060 06285000 D
1365 4809 A0C0 0000 00FC 06286000 D
1366 4809 A0C0 0000 00FC 06287000 D
1367 50E0 00C0 0000 0060 06288000 D
1368 4809 A0C0 0000 00FC 06289000 D
1369 4809 A0C0 0000 00FC 06290000 D
1370 50E0 00C0 0000 0060 06291000 D
1371 4809 A0C0 0000 00FC 06292000 D
1372 4809 A0C0 0000 00FC 06293000 D
1373 50E0 00C0 0000 0060 06294000 D
1374 4809 A0C0 0000 00FC 06295000 D
1375 4809 A0C0 0000 00FC 06296000 D
1376 50E0 00C0 0000 0060 06297000 D
1377 4809 A0C0 0000 00FC 06298000 D
1378 4809 A0C0 0000 00FC 06299000 D
1379 50E0 00C0 0000 0060 06300000 D

```



```

131E 0000 0000 0000 0020
131F 4809 AC61 407C 60F0
1320 4809 AC5C 4C30 60F0
1321 66E0 0070 0070 0040
OP401:
1322 559C 0070 0070 0040
OP401:
1323 5F90 00C0 0030 0060
1324 4809 6A09 004C 60FC
1325 1CAC 0000 0C30 00C0
1326 4009 0060 0C0C 60F0
1327 4824 0060 0070 00FC
OP401:
1328 1C80 00C0 007C 0040
1329 1CC0 0070 0C70 0040
132A 1CD0 00C0 009C 604C
132B 1CE0 0060 000C 0040
OP410:
132C 2260 00C0 0C70 0060
132D 4809 0C52 0C30 60F0
132E 56FC 00C0 000C 00F0
132F 56E0 007C 0070 0040
1330 4809 0C40 207C 00F0
1331 4809 0C20 203C 00F0
1332 2F50 00C0 000C 0060
1333 2380 00C0 000C 0060
1334 1809 AC60 0C30 60F0
1335 0000 00C0 0C30 0020
1336 4809 AC71 4000 00F0
1337 4809 AC5C 407C 60F0
1338 56FC 00C0 0000 0040
OP411:
1339 2260 00C0 000C 0060
133A 1809 6C52 007C 60FC
133B 680B 0060 007C 60F0
133C 56E0 0060 0000 0040
133D 5590 0070 0070 0040
OP412:
133E 2260 00C0 000C 0060
133F 1809 6C52 007C 60FC
1340 680B 0060 007C 60FC
1341 56FC 00C0 003C 6040
1342 4809 0C40 203C 60FC

```

```

16 = SAR
AI L = AI
AI OR D = AI
OPCODE - 1 = MPCR

```

```
RII - 1 = MPCR
```

```

OPCODE41:
%ECODE - 1 = CPCR
%2 = MPCR = AMPCR
OP41F - 1 = AMPCR
STEP
EXEC

```

```

OP410:
OP410 - 1 = MPCR
OP411 - 1 = MPCR
OP412 - 1 = MPCR
OP413 - 1 = MPCR

```

```

OP410:
CONTENTSRA - 1 = CPCR % RETURN (R(A)) IN B
D EOL 0
IF TRUE THEN STEP ELSE SKIP
OPCODE - 1 = MPCR
R = A2
A2 - 1 = HIR
COUNTER - 1 = CPCR
% WRITE NEW (R(A)) VALUE IN R(A)
% B CONTAINS (R(H))
% CLEAR THE OLD PAR
16 = SAR
AI L = AI
AI OR D = AI
OPCODE - 1 = MPCR

```

```

OP410:
CONTENTSRA - 1 = CPCR % RETURN (R(A)) IN B
D EOL 0
IF TRUE THEN STEP ELSE SKIP
OPCODE - 1 = MPCR
R = A2
A2 - 1 = HIR
COUNTER - 1 = CPCR
% WRITE NEW (R(A)) VALUE IN R(A)
% B CONTAINS (R(H))
% CLEAR THE OLD PAR
16 = SAR
AI L = AI
AI OR D = AI
OPCODE - 1 = MPCR

```

```

OP411:
CHECKCC - 1 = CPCR
R EOL 0
IF TRUE THEN STEP ELSE SKIP
OPCODE - 1 = MPCR
RII - 1 = MPCR

```

```

OP412:
CONTENTSRA - 1 = CPCR % PUT (R(A)) IN B
D EOL 0
IF TRUE THEN STEP ELSE SKIP
OPCODE - 1 = MPCR

```

```

06238000 0
06239000 0
06240000 C
06241000 0
06242000 F
06243000 0
06244000 0
06245000 U
06246000 0
06247000 0
06248000 C
06249000 0
06250000 0
06251000 0
06252000 0
06253000 0
06254000 C
06255000 C
06256009 0
06257000 L
06258000 0
06259000 F
06260000 C
06261000 0
06262000 0
06263000 0
06264000 L
06265000 0
06266000 0
06267000 0
06268000 0
06269000 0
06270000 0
06271000 0
06272000 0
06273000 0
06274000 0
06275000 0
06276000 0
06277000 0
06278000 0
06279000 0
06280000 0
06281000 C
06282000 0
06283000 0
06284000 0
06285000 0
06286000 0
06287000 0
06288000 C
06289000 0
06290000 C
06291000 0
06292000 0
06293000 0
06294000 C
06295000 0
06296000 0
06297000 0

```

```
% (Y) INTO PAR
```

```
% LJ LOCAL JUMP
```

```
% (P) + XD -> F
```

```
% TYPE RI (I)
```

```
% (P) + XD -> P
```

```
%
```

```
%
```

```
% INDEX JUMP
```

```
% *F* CODE RETURNED IN A?
```

```
%
```

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%
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%
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06359000 C  
 06359000 C  
 06361000 D  
 06361000 D  
 06362000 D  
 06363000 D  
 06364000 D  
 06365000 C  
 06366000 C  
 06367000 D  
 06368000 D  
 06369000 C  
 06370000 C  
 06371000 C  
 06372000 C  
 06373000 C  
 06374000 C  
 06375000 C  
 06376000 D  
 06377000 D  
 06378000 C  
 06379000 C  
 06380000 C  
 06381000 C  
 06382000 D  
 06383000 D  
 06384000 C  
 06385000 C  
 06386000 C  
 06387000 D  
 06388000 D  
 06389000 C  
 06390000 D  
 06391000 D  
 06392000 D  
 06393000 C  
 06394000 D  
 06395000 D  
 06396000 D  
 06397000 D  
 06398000 D  
 06399000 C  
 06400000 C  
 06401000 D  
 06402000 D  
 06403000 C  
 06404000 D  
 06405000 D  
 06406000 D  
 06407000 C  
 06408000 D  
 06409000 D  
 06410000 D  
 06411000 D  
 06412000 C  
 06413000 C  
 06414000 D  
 06415000 D  
 06416000 C  
 06417000 D

X (P) + 1 INTO R(A); (R(H)) INTO P  
 X B CONTAINS \*A\*  
 X ADDRESS OF R(A) IN MAR2  
 X (P) INTO MS WORD OF A2  
 X (P) INTO LS WORD OF A2  
 X (P) + 1 INTO R(A)  
 X (R(H)) INTO B  
 X CLEAR PAR FIELD  
 X PREPARE FOR NEW PAR  
 X CREATE NEW PAR  
 X  
 X RK TYPE JUMP, LINK REGISTERS  
 X (P) + 2 INTO R(A); Y INTO P  
 X B CONTAINS \*A\*  
 X MAR2 CONTAINS ADDRESS OF R(A)  
 X SAVE OLD PAR  
 X PAR INTO LS WORD OF A2  
 X MIR CONTAINS (P) + 2  
 X PUT (P) + 2 INTO R(A)  
 X \*H\* INTO A3  
 X CHECK IF \*H\* = 0  
 X (R(H)) INTO B  
 X Y INTO B  
 X (Y) INTO B  
 X CLEAR THE PAR  
 X PREPARE FOR THE NEW PAR  
 X CREATE THE NEW PAR  
 X  
 X RK TYPE JUMP, LINK REGISTERS  
 X (P) + 2 INTO R(A); (Y) INTO P  
 X P CONTAINS \*A\*  
 X ADDRESS OF R(A) IN MAR2  
 X (P) INTO MS WORD OF A2  
 X (P) INTO LS WORD OF A2  
 X (P) + 2 INTO MIR  
 X (P) + 2 INTO R(A)  
 X SET UP D FOR RANFIELD  
 X Y INTO B  
 X Y INTO GR2  
 X (Y) INTO B

B R = B  
 4 = SAR, 15 = LIT  
 LIT AND B = F  
 REGSTACK - 1 = CPCR  
 A1 L = A2  
 16 = SAR  
 A2 R = A2  
 EQUIPUT - MIR  
 EQUIPUT - 1 = CPCR  
 COMTENSIM - 1 = CPCR  
 A1 R = A1  
 COMP 16 = SAR  
 A1 L = A1  
 A1 OR B = A1  
 OPCODE - 1 = MPCR  
 O R = B  
 4 = SAR, 15 = LIT  
 LIT AND B = B  
 REGSTACK - 1 = CPCR  
 A1 L = A2  
 COMP 16 = SAR; 2 = LIT  
 A2 R = A2  
 A2 + LIT = MIR  
 EQUIPUT - 1 = CPCR  
 A3 AND LIT = A3  
 15 = LIT  
 A3 EQU P  
 IF TRUE THEN 0 = 0; SKIP X CHECK IF \*H\* = 0  
 COMTENSIM - 1 = CPCR  
 A3 + B = B  
 A3 + B = B  
 A1 R = A1  
 COMP 16 = SAR  
 A1 L = A1  
 A1 OR D = A1  
 OPCODE - 1 = MPCR  
 B R = B  
 4 = SAR, 15 = LIT  
 LIT AND B = F  
 REGSTACK - 1 = CPCR  
 A1 L = A2  
 16 = SAR; 2 = LIT  
 A2 R = A2  
 A2 + LIT = MIR  
 EQUIPUT - 1 = CPCR  
 A3 = B  
 RANFIELD - 1 = CPCR  
 COMP 16 = SAR  
 EULIN - 1 = CPCR

0P421:  
 1372 4809 0C40 000C 00F0  
 1373 50FC 0C00 000C 008C  
 1374 4809 2C56 0000 00FC  
 1375 510C 0000 0000 006C  
 1376 4809 A001 2000 00F0  
 1377 5000 0000 4F00 0020  
 1378 4809 C000 000C 000C  
 1379 4809 C000 000C 000C  
 137A 2F5C 0000 0000 006C  
 137B 2380 0000 0000 006C  
 137C 4009 C000 0000 006C  
 137D 0000 C000 0000 0020  
 137E 4809 A001 4000 00F0  
 137F 4809 AC5C 4000 00F0  
 1380 66EC 0000 0000 0040  
 1381 4809 0C00 880C 00FC  
 1382 80F0 0C00 000C 008C  
 1383 4809 2C56 0000 00FC  
 1384 510C 0000 0000 006C  
 1385 4809 A001 2000 00F0  
 1386 0020 0000 0000 0040  
 1387 4809 C000 AC00 00F0  
 1388 4809 C140 0050 00F0  
 1389 2F5C 0000 0070 006C  
 138A 4809 E856 1000 006C  
 138B 00FC 0000 0000 006C  
 138C 5009 E012 0000 006C  
 138D 5009 0000 0000 006C  
 138E 238C 0000 0000 006C  
 138F 4809 0C00 100C 00FC  
 1390 633C 0000 0000 006C  
 1391 4809 E840 680C 00F0  
 1392 4809 A000 C000 00F0  
 1393 0000 0000 0000 0020  
 1394 4809 A001 4000 00F0  
 1395 4809 AC5C 4000 00F0  
 1396 56EC 0000 0000 0040  
 1397 4809 0C40 980C 00FC  
 1398 80FC 0000 0050 0080  
 1399 4809 2D56 0050 0080  
 139A 510C 0000 0000 006C  
 139B 4809 A001 2000 00F0  
 139C 0020 0000 0070 0040  
 139D 4809 C000 AC00 00F0  
 139E 4809 C140 0050 00F0  
 139F 2F5C 0000 0070 006C  
 13A0 4809 E856 1000 006C  
 13A1 570C 0000 0000 006C  
 13A2 4809 0C01 0000 006C  
 13A3 000C 0000 0000 0030  
 13A4 60E0 0000 0000 0060

0P423:  
 1397 4809 0C40 980C 00FC  
 1398 80FC 0000 0050 0080  
 1399 4809 2D56 0050 0080  
 139A 510C 0000 0000 006C  
 139B 4809 A001 2000 00F0  
 139C 0020 0000 0070 0040  
 139D 4809 C000 AC00 00F0  
 139E 4809 C140 0050 00F0  
 139F 2F5C 0000 0070 006C  
 13A0 4809 E856 1000 006C  
 13A1 570C 0000 0000 006C  
 13A2 4809 0C01 0000 006C  
 13A3 000C 0000 0000 0030  
 13A4 60E0 0000 0000 0060



```

13A5 4809 AGC0 CC0C 00F0
13A6 00C0 C003 00B0 0020
13A7 4809 A0C1 403C 00F0
13A8 4809 AC5C 4C7C 00F0
13A9 66EC 0003 00B0 C0A0

13AA 5F90 C0C0 0C0C 0060
13AB 4809 C6A0 0C40 C0F0
13AC 103C 0003 00B0 0060
13AD 4809 00C0 0C3C 70F0
13AE 482A 00C0 0030 00FC

OPC00E43:
XFCODE - I = CPCR
A2 + AMPCR = AMPCR
OP43F - I = AMPCR
STEP
EXEC

0P43F1
FAULT - I = MPCR
OP431 - I = MPCR
OP432 - I = MPCR
OP433 - I = MPCR

OP431:
CHECKCC - I = CPCR
O EOL B
IF TRUE THEN SKIP
DFCODE - I = MPCR
A1 L = A2 IF LCI
COMP 16 = SAR
A2 R = A2
A2 + I = HIR
A2 L = A2
A3 = B
B L = C-CSR
COMP 24 = SAR
B = SAR
IF HSI THEN - B = E; SET LCI & IF *D* NEGATIVE {FT LCI
B R = B
LIT AND B L = D
LIT AND B L = D
127 = LIT; COMP 16 = SAR
STEP
B = SAR
IF LCI THEN A2 - B R = BR2;A3; SKIP & (P) - D
A2 + B R = BR2;A3
CMULOUT - I = CPCR
A3 R = B
B = SAR
R + I = B
A1 R = A1
COMP 16 = SAR
A1 L = A1
A1 L = A1
A1 OR B = A1
OPCODE - I = MPCR

1301 4809 2E55 0800 00F0
1302 00FC 00C0 0030 00E0
1303 4809 0C52 0C30 00F0

1304 5F90 C0C0 0C0C 0060
1305 4809 C6A0 0C40 C0F0
1306 103C 0003 00B0 0060
1307 4809 00C0 0C3C 70F0
1308 482A 00C0 0030 00FC

OPC00E43:
XFCODE - I = CPCR
A2 + AMPCR = AMPCR
OP43F - I = AMPCR
STEP
EXEC

0P43F1
FAULT - I = MPCR
OP431 - I = MPCR
OP432 - I = MPCR
OP433 - I = MPCR

OP431:
CHECKCC - I = CPCR
O EOL B
IF TRUE THEN SKIP
DFCODE - I = MPCR
A1 L = A2 IF LCI
COMP 16 = SAR
A2 R = A2
A2 + I = HIR
A2 L = A2
A3 = B
B L = C-CSR
COMP 24 = SAR
B = SAR
IF HSI THEN - B = E; SET LCI & IF *D* NEGATIVE {FT LCI
B R = B
LIT AND B L = D
LIT AND B L = D
127 = LIT; COMP 16 = SAR
STEP
B = SAR
IF LCI THEN A2 - B R = BR2;A3; SKIP & (P) - D
A2 + B R = BR2;A3
CMULOUT - I = CPCR
A3 R = B
B = SAR
R + I = B
A1 R = A1
COMP 16 = SAR
A1 L = A1
A1 L = A1
A1 OR B = A1
OPCODE - I = MPCR

1301 4809 2E55 0800 00F0
1302 00FC 00C0 0030 00E0
1303 4809 0C52 0C30 00F0

```

```

06418C00 0
06419C00 0
06420C00 0
06421C00 0
06422C00 0
06423C00 0
06424C00 0
06425C00 0
06426C00 0
06427C00 0
06428C00 0
06429C00 0
06430C00 0
06431C00 0
06432C00 0
06433C00 0
06434C00 0
06435C00 0
06436C00 0
06437C00 0
06438C00 0
06439C00 0
06440C00 0
06441C00 0
06442C00 0
06443C00 0
06444C00 0
06445C00 0
06446C00 0
06447C00 0
06448C00 0
06449C00 0
06450C00 0
06451C00 0
06452C00 0
06453C00 0
06454C00 0
06455C00 0
06456C00 0
06457C00 0
06458C00 0
06459C00 0
06460C00 0
06461C00 0
06462C00 0
06463C00 0
06464C00 0
06465C00 0
06466C00 0
06467C00 0
06468C00 0
06469C00 0
06470C00 0
06471C00 0
06472C00 0
06473C00 0
06474C00 0
06475C00 0
06476C00 0
06477C00 0

X CLEAR THE OLD PAR
X PREPARE TO RECEIVE NEW PAR
X CREATE NEW PAR
X
X JUMP, LINK MEMORY
X *F* RETURNED IN A2
X
X RI TYPE 1, LOCAL JUMP, LINK MEMORY
X ONLY EXECUTE IF CC = 0
X CHECK THE CC CODE
X CHECK IF CC = 0
X
X RI TYPE 1, LOCAL JUMP, LINK MEMORY
X ONLY EXECUTE IF CC = 0
X CHECK THE CC CODE
X CHECK IF CC = 0
X
X PAR INTO A2 (MS WORD)
X PAR INTO A2 (LS WORD)
X PAR INTO UNW
X RESTORE INSTRUCTION INTO B
X *D* SIGN BIT IN PS BIT OF B
X
X SET LCI & IF *D* NEGATIVE {FT LCI
X *D* MAGNITUDE IN LSB OF E
X *D* MAGNITUDE IN B
X
X BR 2;A3; SKIP & (P) - D
X (P) + D
X (P) + 1 INTO (P) + D
X
X (P) + D + 1 INTO B
X CLEAR OLD PAR
X
X BK TYPE JUMP, LINK MEMORY
X (P) + 2 INTO P; Y + 1 INTO P
X ISOLATE *M* FIELD
X IS *H* = 0 ?

```



```

1304 5819 0050 0000 00FF
1305 2380 0050 0030 0060
1306 4809 0050 10FF 00FC
1307 533C 0050 0030 0060
1308 4809 1001 1000 00FF
1309 0050 0050 0050 0030
130A 0852 00C1 2030 00FC
130B 4809 0050 0030 0060
130C 4809 0050 0030 0060
130D 4809 0050 0030 0060
130E 51E0 0000 0000 0060
130F 4809 0050 0030 0060
1310 0000 0000 0000 0010
1311 4809 0050 0030 0060
1312 4809 A000 0000 00FC
1313 0000 0000 0000 0020
1314 4809 A001 4000 00FF
1315 4809 A050 4000 00FF
1316 56E0 0000 0000 0040
1317 5F9C 0000 0000 0060
1318 4809 0050 0030 0060
1319 1D7F 0000 0000 00C0
131A 4809 0000 0030 00FC
131B 4824 0000 0000 00FF
131C 1D8C 0000 0030 0040
131D 1D30 0000 0000 0040
131E 1D8A 0000 0000 0040
131F 1D80 0000 0030 0040
1400 228C 0060 0000 0060
1401 4809 0052 0030 00FF

```

```

IF TRUE THEN SKIP
CONTENTSIR - 1 = CPCR % (R(P)) INTO B
D = A3
IFEICH - 1 = CPCR
% Y INTO B
% X Y INTO B, A3
COMP 8 = SAR
% (P) INTO A2
% (P) INTO A2
% (P) INTO LS WORD OF A2
% MIP CONTAINS (Y) + 2
% (P) % 2 INTO B
% Y INTO A3 LE WORD
% R CONTAINS Y + 1
% CLEAR THE PAR
% CREATE N1W PAR
%
% 0649600 C
% 0649700 D
% 0649800 C
% 0649900 C
% 0650000 D
% 0650100 D
% 0650200 D
% 0650300 C
% 0650400 D
% 0650500 C
% 0650600 C
% 0650700 D
% 0650800 D
% 0650900 D
% 0651000 D
% 0651100 D
% 0651200 D
% 0651300 D
% 0651400 D
% 0651500 D
% 0651600 D
% 0651700 D
% 0651800 D
% 0651900 D
% 0652000 D
% 0652100 D
% 0652200 D
% 0652300 D
% 0652400 D
% 0652500 D
% 0652600 D
% 0652700 D
% 0652800 D
% 0652900 C
% 0653000 C
% 0653100 D
% 0653200 D
% 0653300 D
% 0653400 D
% 0653500 D
% 0653600 D
% 0653700 D

```

OPR433:

```

RXMFIELD - 1 = CPCR
R L = BR2, A3
COMP 8 = SAR
A1 L = A2
COMP 16 = SAR, 2 = LIT
A2 R = A2
% LIT = M1R
% MIP CONTAINS (P) + 2
% (Y) INTO A3
% (Y) + 1 INTO B
% A1 READY TO ACCEPT NEW PAR
% CREATE N1W PAR
%
% JUMP ZERO
% RETURNS *P= CODE IN A

```

OPCODE44:

```

XFCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP44F - 1 = AMPCR
STEP
EXEC
OP440: OP440 - 1 = MPCR
OP441 - 1 = MPCR
OP442 - 1 = MPCR
OP443 - 1 = MPCR

```

OP440:

```

CONTENTSIRA - 1 = CPCR
IF (C) % (R(N)) IN P
B EOL 0
% RETURNS (R(A)) IN B

```



```

1402 6819 0C00 0C00 00F0
1403 66E0 0C00 00C0 0040
1404 2380 0C70 00C0 006C
1405 4869 A0C0 0C30 00FC
1406 00C0 0C00 0C30 002C
1407 4809 A0C1 4C7C 00F0
1408 4879 AC5C 405C 00FC
1409 56E0 0C70 0C30 0040

140A 2250 0060 0070 006C
140B 4800 6800 CC52 0C70 00F0
140C 6819 C000 C09C 00F0
140D 66E0 C0F0 C09C 0040
140E 5590 0C00 009C 0C40

140F 2280 C060 0C60 0060
1410 4809 0C52 0C30 00F0
1411 1411 6819 0C00 003C 00F0
1412 1030 0000 009C 0040
1413 4839 E156 1C90 00F0
1414 00F0 0000 003C 006C
1415 4819 6812 0050 00FC
1416 2310 0C00 009C 00FC
1417 4809 C040 100C 00F0
1418 533C 0000 003C 0060
1419 4809 EC80 0B30 00FC
141A 4809 A000 C09C 00FC
141B 4809 A001 4C9C 00F0
141C 0C00 C0C0 C0C0 002C
141D 4809 A001 4C9C 00F0
141E 4879 AC5C 4C9C 00F0
141F 56E0 0C00 0C30 0040

1420 2250 0000 009C 006C
1421 4809 0C52 C030 00F0
1422 6819 0000 0C00 00F0
1423 103C 0000 009C 0040
1424 4809 C000 0C30 00F0
1425 5700 0000 009C 006C
1426 4809 C041 0C1C 00FC
1427 00C0 0C00 0C30 C030
1428 56E0 0C00 0C30 0060
1429 4809 A000 C09C 00FC
142A 4809 A001 4C9C 00F0
142B 4809 A001 4C9C 00F0
142C 4809 AC5C 4C9C 00F0
142D 56E0 0C00 0C30 0040

142E 5F90 C000 0C30 0060

```

```

IF TRUE THEN SKIP
OPCODE - 1 = MPCR
CONTENTSRR - 1 = CPCR
% RETURNS (R(R)) IN B
% CLEAR OLD PAR
AL R = AI
COMP 16 = SAR
AL L = AI
AL R = AI
OPCODE - 1 = MPCR

% RI TYPE 1 LOCAL JUMP EQUAL
% IF (CC) = 0R 0, (P) + D INTO P
% RETURNS CC BITS IN B
% (P) + D = P
%
% RK TYPE JUMP ZERO
% IF (R(A)) 0, Y INTO P
% GET (R(A)) IN B
% ADVANCE THE PAR BY 1 AND CALL OPCODE
% M* FIELD IN A3
%
% RETURN (R(RH)) IN B
% Y INTO B
% PAR VALUE IN LS WORD OF E
% CLEAR OLD PAR
% CREATE NEW PAR
%
% RX TYPE JUMP ZERO
% IF (F(A)) = 0, (Y) INTO P
% (R(A)) INTO B
% ADVANCE THE PAR BY 1 AND CALL OPCODE
% ANALYZE THE M* FIELD
% PUT Y INTO BR2
% (Y) INTO B
% CLEAR OLD PAR
% CREATE NEW PAR
%
% JUMP NOT ZERO
% RETURN M* FIELD IN LSD OF A2

```

```

OP441:
OP442:
OP443:
OP444:
OP445:

```









```

1439 4809 2C56 0F90 00F0
143A 51C0 0F70 0070 0060
143B 2F30 0F60 0C00 0060
143C 4809 0C52 0000 00F0
143D 500R 0000 0070 00F0
143E 403C 0070 0070 0060
143F 5700 0070 0070 0060
1440 4809 0C74 0010 00F0
1441 0000 0000 0070 0060
1442 501C 0000 0070 0060
1443 4809 4000 0000 0010
1444 0000 0000 0070 0020
1445 4809 4000 403C 00F0
1446 4809 4C15 4C00 00F0
1447 6600 0C15 4C00 0060

1468 5F90 0000 0000 0080
1469 4809 6C40 0070 00F0
146A 1E10 0000 0000 0000
146B 4809 0000 0030 00F0
146C 4824 0000 0070 00F0

1470 1E20 0000 0070 0090
1471 1E3C 0000 0000 0090
1472 1E40 0000 0030 0090
1473 1E50 0000 0000 0090
1474 4824 0000 0070 0090
1475 480E 0000 0000 0090
1476 660E 0000 0000 0090
1477 2380 4000 0000 0060
1478 4809 4000 0000 00F0
1479 3000 0000 0070 0020
147A 4809 4C01 4030 00F0
147D 4809 4C5C 4000 00F0
147E 660E 0000 0000 0040

1470 226F 0000 0000 0060
1471 4809 2C52 0C30 00F0
1472 0030 0000 0030 00F0
1473 0030 0000 0000 00F0
1474 660E 0000 0000 00F0
1475 660E 0000 0000 00F0
1476 4809 4000 0000 00F0
1477 4809 4C01 4030 00F0
1478 4809 4C5C 4000 00F0
1479 3000 0000 0070 0020
147A 4809 4C01 4030 00F0
147D 4809 4C5C 4000 00F0
147E 660E 0000 0000 0040

1483 2280 0000 0000 0060
1484 4809 4C41 0B00 00F0

```

```

LIT AND B = B
REGSTACK - 1 = CPCR
INPUT - 1 = CPEK
B EOL 0
IF TRUE THEN SKIP ELSE SKIP
RUMP - 1 = HPCR
RNFIELD - 1 = CPCR
D L = BR2
COMP B = SAR
EMULIN - 1 = CPCR
A1 R = A1
COMP 16 = SAR
A1 L = A1
A1 DR P = A1
OPCODE - 1 = MPCR

% ISOLATE *A*
% R(A) INTO HAR2
% R(A) INTO B
% ADVANCE THE PAR BY 1 AND CALL OPCODE
% ANALYZE *H* FIELD
% ADDRESS OF Y INTO BR2
% (Y) IN B
% CREATE NEW PAR
% JUMP POSITIVE
% GET *F* CODE IN A2
CONTENTSRA - 1 = CPCR
AMPCR = AMPCR
OP46F - 1 = AMPCR
STEP
EXEC
OP46F:
OP46F - 1 = HPCR
OP461 - 1 = HPCR
OP462 - 1 = HPCR
OP463 - 1 = HPCR

OP460:
CONTENTSRA - 1 = CPCR
% IF (R(A)) >= 0, (R(H)) INTO P
% R(A) INTO P
% SHIFT (R(A)) TO MS WORD
% PUT E IN THE ADDR
% TEST (R(A)) >= 0
% (R(H)) INTO P
% CLEAR THE PAR FIELD
% SET UP NEW PAR
%
%
% RI TYPE 1 LOCAL JUMP >=
% RETURN CC IN LS ENITS OF E
% TEST FOR <
IF TRUE THEN SKIP ELSE SKIP
OPCODE - 1 = MPCR
R11 - 1 = HPCR
% (P) + D = P
%
% RR TYPE JUMP POSITIVE
% IF (R(A)) >= 0, (R(H)) INTO P
% (R(A)) INTO P
% SHIFT (R(A)) TO MS WORD
%
% RI TYPE 1 LOCAL JUMP >=
% RETURN CC IN LS ENITS OF E
% TEST FOR <
IF TRUE THEN SKIP ELSE SKIP
OPCODE - 1 = MPCR
R11 - 1 = HPCR
% (P) + D = P
%
% RR TYPE JUMP POSITIVE
% IF (R(A)) >= 0, Y INTO P
% R(A) INTO P
% SHIFT (R(A)) INTO MS WORD OF B

```







1484 4809 CC41 0070 00F0    X SHIFT (RCA) INTO UHW OF B    06778C00 D  
 B L = B    06779C00 D  
 COMP 16 = SAR    06706C00 D  
 1485 0000 00C3 0070 00F0    % PUT B IN THE ADDR, TEST (RCA) < 0    06781C00 D  
 1486 4809 00C4 0000 00F0    IF RST THEN SKIP    06782C00 D  
 1487 4819 C003 0070 00F0    OPCODE - 1 = MPCR    06783C00 D  
 1488 56EC 00C3 0070 00F0    CONTENTSRM - 1 = CPCR    06784C00 D  
 1489 2380 0000 0000 00E0    AI R = AI    06785C00 D  
 148A 4809 ACC0 CC00 00F0    COMP 16 = SAR    06786C00 D  
 148B 0000 00C0 0070 00F0    AI L = AI    06787C00 C  
 148C 4809 ACC1 4C00 00F0    AI OR B = AI    06788C00 D  
 148D 4809 ACE5 4070 00F0    OPCODE - 1 = MPCR    06789C00 D  
 148E 56EC 0000 0000 00E0    % RI TYPE 1 LOCAL JUMP LESS INSTRUCTION    06791C00 C  
 0P4711    06792C00 D  
 148F 2809 0000 0070 00F0    CHECKCC - 1 = CPCR    06793C00 D  
 1490 226C 00C0 0000 00E0    LIT FOL B    06794C00 D  
 1491 4809 2E52 0000 00F0    3 = LIT    06795C00 D  
 1492 003C 00C3 0000 00E0    IF FALSE THEN SKIP ELSE SKIP    06796C00 D  
 1493 66CB 00C0 0000 00F0    OPCODE - 1 = MPCR    06797C00 D  
 1494 66EC 00C0 C070 00F0    RI1 - 1 = MPCR    06798C00 D  
 1495 5590 0000 0000 00E0    % (P) + 0 = P    06799C00 D  
 1496 220C 00C3 0000 00E0    %    06800000 D  
 1497 4809 0041 C000 00F0    % RK TYPE JUMP NEGATIVE    06801C00 D  
 1498 0000 00C0 0000 00E0    % IF (RCA) < 0, (Y) = P    06802000 D  
 1499 0000 0000 0000 00E0    % (RCA) INTO B    06803C00 D  
 149A 4809 0000 0000 00E0    % SHIFT (RCA) INTO UHW OF B    06804C00 D  
 149B 2380 0000 0000 00E0    % CHECK IF (RCA) < 0    06805C00 C  
 149C 4809 0000 0000 00E0    % ADVANCE THE FAR BY 1 AND CALL OPCODE    06806C00 D  
 149D 0000 00C0 0000 00E0    B L = B    06807C00 C  
 149E 4809 0000 0000 00E0    COMP 16 = SAR    06808C00 D  
 149F 4809 0000 0000 00E0    IF RST THEN SKIP    06809C00 D  
 14A0 4809 0000 0000 00E0    CONTENTSRM - 1 = CPCR    06810C00 D  
 14A1 4809 0000 0000 00E0    AI R = AI    06811C00 D  
 14A2 4809 0000 0000 00E0    IFETCH - 1 = CPCR    06812C00 D  
 14A3 4809 0000 0000 00E0    AI R = AI    06813C00 D  
 14A4 4809 0000 0000 00E0    COMP 16 = SAR    06814C00 D  
 14A5 4809 0000 0000 00E0    AI OP B = AI    06815C00 D  
 14A6 56EC 00C0 0070 00F0    OPCODE - 1 = MPCR    06816C00 D  
 0P4721    06817C00 D  
 14A7 4809 0000 0000 00E0    % CONSTRUCT NEW PAR    06818C00 C  
 14A8 4809 0000 0000 00E0    %    06819C00 D  
 14A9 4809 0000 0000 00E0    % RX TYPE JUMP INSTRUCTION    06820C00 D  
 14AA 4809 0000 0000 00E0    % IF (RCA) < 0, (Y) = P    06821C00 D  
 14AB 4809 0000 0000 00E0    % SHIFT \*A\* INTO LS BITS OF B    06822C00 D  
 14AC 4809 0000 0000 00E0    % ISOLATE \*A\* INTO B    06823C00 D  
 14AD 4809 0000 0000 00E0    REGSTACK - 1 = CPCR    06824C00 D  
 14AE 2F30 0000 0000 00E0    INPUT - 1 = MPCR    06825C00 D  
 14AF 4809 0000 0000 00E0    R L = B    06826C00 D  
 14B0 0000 0000 0000 00E0    COMP 16 = SAR    06827C00 D  
 14B1 4809 0000 0000 00E0    B    06828C00 D  
 14B2 4809 0000 0000 00E0    IF RST THEN SKIP    06829C00 D  
 14B3 4809 0000 0000 00E0    BUMP - 1 = MPCR    06830C00 C  
 14B4 4809 0000 0000 00E0    AI = B    06831C00 D  
 14B5 4809 0000 0000 00E0    COMP FIELD - 1 = CPCR    06832C00 D  
 14B6 570C 00C3 0070 00F0    COMP FIELD - 1 = CPCR    06833C00 D  
 14B7 4809 0000 0000 00E0    COMP B SAR    06834C00 D  
 14B8 4809 0000 0000 00E0    EULIM - 1 = MPCR    06835C00 D  
 14B9 56EC 00C0 0070 00F0    % PUT Y INTO PR2    06836C00 D  
 14BA 4809 0000 0000 00E0    % PUT (Y) INTO B    06837C00 D  
 14BB 56EC 00C0 0070 00F0    %    06838C00 D  
 14BC 4809 0000 0000 00E0    %    06839C00 D  
 14BD 4809 0000 0000 00E0    %    06840C00 D  
 14BE 4809 0000 0000 00E0    %    06841C00 D  
 14BF 4809 0000 0000 00E0    %    06842C00 D  
 14C0 4809 0000 0000 00E0    %    06843C00 D  
 14C1 4809 0000 0000 00E0    %    06844C00 D  
 14C2 4809 0000 0000 00E0    %    06845C00 D  
 14C3 4809 0000 0000 00E0    %    06846C00 D  
 14C4 4809 0000 0000 00E0    %    06847C00 D  
 14C5 4809 0000 0000 00E0    %    06848C00 D  
 14C6 4809 0000 0000 00E0    %    06849C00 D  
 14C7 4809 0000 0000 00E0    %    06850C00 D  
 14C8 4809 0000 0000 00E0    %    06851C00 D  
 14C9 4809 0000 0000 00E0    %    06852C00 D  
 14CA 4809 0000 0000 00E0    %    06853C00 D  
 14CB 4809 0000 0000 00E0    %    06854C00 D  
 14CC 4809 0000 0000 00E0    %    06855C00 D  
 14CD 4809 0000 0000 00E0    %    06856C00 D  
 14CE 4809 0000 0000 00E0    %    06857C00 D  
 14CF 4809 0000 0000 00E0    %    06858C00 D  
 14D0 4809 0000 0000 00E0    %    06859C00 D  
 14D1 4809 0000 0000 00E0    %    06860C00 D  
 14D2 4809 0000 0000 00E0    %    06861C00 D  
 14D3 4809 0000 0000 00E0    %    06862C00 D  
 14D4 56EC 00C0 0070 00F0    OPCODE - 1 = MPCR    06863C00 D  
 0P4731    06864C00 D  
 14D5 4809 0000 0000 00E0    %    06865C00 D  
 14D6 50F0 00C0 0070 00F0    %    06866C00 D  
 14D7 4809 2E55 0070 00F0    %    06867C00 D  
 14D8 51C0 00C0 0000 00E0    %    06868C00 D  
 14D9 2F30 0000 0000 00E0    %    06869C00 D  
 14DA 4809 0000 0000 00E0    %    06870C00 D  
 14DB 0000 0000 0000 00E0    %    06871C00 D  
 14DC 4809 0000 0000 00E0    %    06872C00 D  
 14DD 0000 0000 0000 00E0    %    06873C00 D  
 14DE 4809 0000 0000 00E0    %    06874C00 D  
 14DF 4809 0000 0000 00E0    %    06875C00 D  
 14E0 570C 00C3 0070 00F0    %    06876C00 D  
 14E1 4809 0000 0000 00E0    %    06877C00 D  
 14E2 0000 00C0 0070 00F0    %    06878C00 D  
 14E3 56EC 00C0 0070 00F0    %    06879C00 D













```

1*30 2F5C C0C0 0070 C060
153E 666E 00C0 0070 0040

OP5511
153F 4809 0C40 803C 00FC
1540 80F0 00C0 0070 0060
1541 4809 2C56 0030 C0F0
1542 51C0 00C0 00D0 0060
1543 2F30 0030 0070 0060
1544 4809 2C56 2030 0060
1545 00FC 0000 003C 0060
1546 4809 C643 001C 0060
1547 300C 0000 0070 0060
1548 4809 00C0 0070 0060
1549 2F30 0000 0070 0060
154A 4809 0C40 0030 0060
154B 4809 E356 0030 0060
154C 00FC 00C0 0000 C0E0
154D 51C0 00C0 C030 0060
154E 4809 C643 001C 0060
154F 4809 00C0 0070 0060
1550 51C0 00C0 0070 0060
1551 51C0 00C0 0070 0060
1552 56E0 C0C0 0000 0040

OP5531
1553 5700 C0C0 0070 0060
1554 4809 0C40 0030 C0F0
1555 4809 E3C0 8030 00F0
1556 80F0 C0C0 0000 0060
1557 4809 2C56 0030 0060
1558 51C0 00C0 0000 0060
1559 2F30 0000 0070 0060
155A 4809 2C56 2000 C0F0
155B 00FC 0000 0000 0090
155C 4809 C640 1070 C0F0
155D 4809 0C40 0030 C0E0
155E 4809 00C0 0070 0060
155F 4809 00C0 0070 0060
1560 00FC 00C0 0030 C040
1561 6C19 20C1 0070 00F0
1562 4809 C047 0000 00F0
1563 4809 E041 0020 00F0
1564 0000 00C0 0070 C030
1565 4809 0C40 1030 00F0
1566 4809 E3C0 1000 00F0
1567 4A2C 00C0 0070 0060
1568 66E0 C0C0 0070 C040

OPC00F56:
1569 4E5C 00C0 0070 0040

OPC00E57:
156A 4E50 00C0 0070 0040

OUTPUT - 1 = CPCR
OPCODE - 1 = MPCK

X (AR) -> RM
X SARI STORE ADDRESS REGISTER
X TYPE R1 (AR) A -> Y*
X L = :A1 FIELD
X MAR2 = RA
X B = (R(A))
X A2 = REG #
X PAGEREG CASE + REG #
X SEPARATE APCR ASSIGNMENTS
X B = (AR)
X P = :H1 FIELD
X L = (R(H)) = Y#
X Y = INTO DR2
X (AR) -> Y#
X STORE ADDRESS REGISTER MULTIPLE
X SARI TYPE RX (AR R1...AK R10) ->
X Y...Y+U
X MULTIPLE STORES DO OBSERVE PAGE
X ADDRESSES
X MIR = Y
X E = :A1 FIELD
X L = (R(A))
X A2 HAS PAGE REG #
X P = AR R
X SHIFT COUNT INTO LS BITS OF P
X A COUNT OF ZERO MEANS ALL REG STORED
X COUNT IN B
X ORIGIN ADDR IN B#1
X COUNT IN UHW OF A3
X DESTINATION ADDR IN LHW OF A3
X NOT IMPLEMENTED
X NOT IMPLEMENTED

```









```

1598 4809 0C41 1000 00F0
1599 0010 0000 0070 00A0
159A 4809 2F5C 001C 00FC
159B 2F30 00C0 0070 0060
159C 4809 EC5C 100C 00F0
159D 4809 CF00 0030 00FC
159E 49C9 E000 0070 00FC
159F 2000 0000 0000 0060
15A0 4809 E001 0050 00F0
15A1 0000 0000 0000 0020
15A2 4809 0C40 3030 00F0
15A3 2F50 0000 0000 0060
15A4 4809 00C0 0070 20F0
15A5 4809 0F40 801C 00FC
15A6 4809 0000 0000 0000
15A7 4809 E000 0070 00F0
15A8 0000 0000 0000 0020
15A9 2F5C 00C0 0000 0060
15AA 56E0 0000 0070 00A0

15AB 4809 2C55 7020 00FC
15AC 00F0 C700 0C20 00E0
15AD 28C9 C640 8050 00FC
15AE 80FC 00C0 0070 00A0
15AF 4809 2C55 7020 00F0
15B0 51C0 0F00 0020 0060
15B1 4809 0F41 0020 00F0
15B2 0000 6000 0C30 0030
15B3 2F3C 0000 0C20 0060
15B4 4809 0C41 0030 00F0
15B5 0000 0000 0070 0020
15B6 4809 0C40 0000 00F0
15B7 48C9 C600 0050 00F0
15B8 0C10 0000 0030 00A0
15B9 4809 5E5C 100C 00FC
15BA 2E32 2F5C 001C 00FC
15BB 4809 00C0 0070 00F0
15BC 4809 E0C0 0000 0020
15BD 0000 0F00 0000 00FC
15BE 4809 E001 1070 00FC
15BF 4809 EC5C 1000 80F0
15C0 4809 C5C0 0000 80F0
15C1 48C9 E000 9030 00FC
15C2 4809 00C0 0000 00F0
15C3 2C09 0010 0020 00F0
15C4 4809 0C41 C800 00FC
15C5 49C9 EC5C 1E30 00FC
15C6 2000 00C0 0020 0060
15C7 4809 E001 2F20 00FC
15C8 0000 0000 0070 0020
15C9 4809 C0C0 8030 00FC
15CA 2F50 0000 0020 0060
15CB 4809 0000 0C30 20F0
15CC 4809 0F40 801C 00FC
15CD 0000 0000 0000 0040
15CE 48C9 E0F0 8050 00F0

B L = A3
16 = SAR J 1 = LIT
LIT OR BHAR = MAR2
EINPOT - 1 = CPCK
A3 OR B = A3
A2 = SAR
A3 R = A3+J1 SET LCI
SETCCA - 1 = CPCK
A3 L = B
COMP 16 = SAR
B R = MIR
EUIPOT - 1 = CPCK
ASR
BHAR R = MAR2
B = SAR
A3 = MIR
A2 = SAR
EUIPOT - 1 = CPCK
OPCODE - 1 = MPCK

LIT AND R = A2
15 = LIT
B R = B J IF LCI
4 = SAR J 5 = LIT
LIT AND B = B
REGSTACK - 1 = CPCK
BHAR L = BR1
COMP 8 = SAR
EINPOT - 1 = CPCK
P L = B
COMP 16 = SAR
IF HST THEN SET LCI
COMP 16 = SAR J 1 = LIT
A3 OR B = A3
LIT OR BHAR = MAR2
EINPOT - 1 = CPCK
A3 R = A3
A3 L = A3
A3 OR B = A3
A2 = SAR
A3 R = A3
IF LCI THEN B111 = B
B L = B
A3 OR B = A3+J1 SET LCI
SETCCA - 1 = CPCK
A3 L = A2
COMP 16 = SAR
A2 R = MIR
EUIPOT - 1 = CPCK
BHAR R = MAR2
ASR
B = SAR
A3 R = MIR

07078100 D
C7079000 D
C7080100 D
C7081200 D
C7082300 D
C7083400 D
C7084500 D
C7085600 C
C7086700 C
C7087800 C
C7088900 D
C7089000 D
C7090100 D
C7091200 D
C7092300 D
C7093400 D
C7094500 D
C7095600 D
C7096700 D
C7097800 D
C7098900 D
C7099000 D
C7100100 D
C7101200 D
C7102300 D
C7103400 D
C7104500 D
C7105600 D
C7106700 D
C7107800 D
C7108900 D
C7109000 D
C7110100 C
C7111200 C
C7112300 D
C7113400 D
C7114500 D
C7115600 D
C7116700 D
C7117800 D
C7118900 D
C7119000 D
C7120100 D
C7121200 D
C7122300 D
C7123400 C
C7124500 C
C7125600 C
C7126700 C
C7127800 D
C7128900 D
C7129000 D
C7130100 C
C7131200 D
C7132300 D
C7133400 D
C7134500 D
C7135600 D
C7136700 D
C7137800 D

```

076031



```

15CF 300C 00C0 0000 002C
15D0 2F5C 0000 0000 0060
15D1 66EC 00C0 0000 0040

16 = SAR
EQUIPUT - 1 = CPCR
OPCODE - 1 = MPCR

OPCODE61: XFCODE - 1 = CPCR
A2 + AMPCR = AMPCR
OP61F - 1 = AMPCR
STEP
EXEC

OP61F: OP610 - 1 = MPCR
OP611 - 1 = CPCR
OP612 - 1 = MPCR
OP613 - 1 = MPCR

OP610:
LIT AND B = A2
B = LIT 4 = SAR
B = LIT 4 = SAR
LIT AND B = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
NOT A2 = A2
B L = B
B R = A2
16 = SAR
NOT A2
IF NOT ABT THEN SET LCI
OVBIT - 1 = CPCR
B L = B
COMP 16 = SAR
P R = M1R, B
EQUIPUT - 1 = CPCR
SECCA - 1 = CPCR
OPCODE - 1 = MPCR

OP611:
LIT AND P = A2
15 = LIT 4 = SAR
P R = B
LIT AND R = B
REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
B = A3
A3 L = A3
COMP 16 = SAR
A3 OR B = A3
A2 = B
LIT - B = A2
A2 = SAR
A3 C = A3
A3 L = A3
COMP 16 = SAR

150B 4809 2C56 203C 0060
150C 8CFC 00C0 0000 0080
150D 4809 0C40 8000 0060
150E 4809 2C56 0000 0060
150F 51CC 00C0 0000 0060
1510 2F3C 00C0 0000 0060
1511 4809 CFC0 2030 0060
1512 4809 C0C0 0000 0060
1513 4809 0C41 8000 0060
1514 4809 C0C0 8000 0060
1515 000C 0000 0000 0020
1516 4809 C002 0030 0060
1517 63C9 00C0 0000 0060
1518 5020 00C0 0000 0060
1519 4809 0C41 8000 0060
151A 0000 0000 0000 0020
151B 4809 0C40 8000 0060
151C 2F5C 00C0 0000 0060
151D 200C 0000 0000 0060
151E 50E9 00C0 0000 0040

15EF 4809 2C56 203C 0060
15F0 8CFC 00C0 0000 0080
15F1 4809 0C40 8000 0060
15F2 4809 2C56 0000 0060
15F3 51CC 00C0 0000 0060
15F4 2F3C 00C0 0000 0060
15F5 4809 0C40 1C00 0060
15F6 4809 E0C1 0000 0060
15F7 0100 0000 0000 0040
15F8 4809 E5C0 1070 0060
15F9 4809 C000 1000 0060
15FA 4809 2C56 0000 0060
15FB 4809 C000 0000 0060
15FC 4809 E0C1 9000 0060
15FD 4809 E001 1F00 0060
15FE 000C 00C0 0000 0020

```

```

0712000 0
0713000 0
0714000 0
07141000 L
07141100 L
07142000 0
07143000 0
07144000 L
07145000 L
07146000 0
07147000 0
07148000 0
07149000 0
07150000 0
07151000 0
07152000 0
07153000 0
07154000 0
07155000 0
07156000 0
07157000 0
07158000 0
07159000 0
07160000 0
07161000 0
07162000 0
07163000 0
07164000 0
07165000 0
07166000 0
07167000 0
07168000 0
07169000 0
07170000 0
07171000 0
07172000 0
07173000 0
07174000 L
07175000 0
07176000 0
07177000 0
07178000 0
07179000 0
07180000 0
07181000 0
07182000 0
07183000 0
07184000 0
07185000 0
07186000 0
07187000 0
07188000 0
07189000 0
07190000 0
07191000 0
07192000 0
07193000 0
07194000 0
07195000 0
07196000 0
07197000 0

```

```

X WRITE NEW (R(A))
X
X
X *F* INTO A2
X
X
X
X
X RL TYPE ALG LEFT SINGLE SHIFT
X (R(A)) M (0-2) PLACES, ZERO FILL
X SET C AND SET OVERFLOW FII
X *M* FIELD INTO A2
X
X
X ISOLATE *A*
X (R(A)) INTO E
X
X PERFORM LEFT SHIFT
X
X
X SET THE OVERFLOW BIT
X
X LEFT SHIFTED (R(A))
X WRITE NEW (R(A))
X SET THE CONDITION BITS
X
X
X TYPE RL CIRCULAR LEFT SHIFT
X (R(A)) SHIFTED M (0-3) PLACES, SET CC
X *M* INTO A2
X
X ISOLATE *A* FIELD
X (R(A)) INTO R
X
X
X A3 = (R(A))/(R(A))
X *M* INTO B
X 1,6 COMPLEMENT OF SHIFT AMOUNT
X PERFORM SHIFT
X
X

```



```

15FF 4809 1000 8830 00F0
1600 2F50 0C70 0C70 C060
1601 2C00 0C70 C0C0 C060
1602 56EC 0C60 0C70 004C

0F612:
1603 4809 0C40 8830 00F0
1604 80F0 0000 C000 0080
1605 4809 E155 205C 00F0
1606 4809 2C56 0B50 00F0
1607 51CC 0000 0000 006F
1608 4809 0F41 C050 00F0
1609 0000 0000 0000 003C
160A 2F30 0C70 0C70 C060
160B 4809 0C40 8830 00F0
160C 0000 0000 0000 C04C
160D 4809 2F5C 0000 C04C
160E 2E30 0000 0000 0060
160F 4809 EC5C 1070 00F0
1610 4809 C042 2C0F 00F0
1611 4809 C0C0 0020 00F0
1612 4809 EC00 880C 00F0
1613 4809 0C42 0C70 00F0
1614 63C9 00C0 0C7C 00F0
1615 502C 0000 0000 C06C
1616 4809 C0C0 0C00 80F0
1617 49C9 E0C1 1B9C 00F0
1618 2000 0C70 0C70 C060
1619 4809 EC01 0B30 00F0
161A 000C 0C00 C000 0020
161B 4809 0C40 8C30 00F0
161C 2F50 00C0 0070 C060
161D 4809 0C70 000F 20F0
161E 4809 0F43 801C 00F0
161F 0000 0000 C030 C010
1620 4809 E070 8C30 00F0
1621 2F50 0000 0000 C020
1622 56E1 0000 0030 000C
1623 56E1 0000 0030 000C

0F613:
1624 4809 2C56 207C C0F0
1625 80F0 0000 0000 C080
1626 4809 0C40 8800 00F0
1627 4809 2C56 0B9C 00F0
1628 51C0 00C0 0000 0060
1629 4809 0F41 0C7C 00F0
162A 0000 0000 0000 C030
162B 2F30 0000 0000 0060
162C 4809 0C41 1C30 00F0
162D 0010 0000 0000 0040
162E 4809 2F5C 001C 00F0
162F 2F30 0000 0000 006C
1630 4809 EC5C 1030 00F0
1631 4809 C0C2 200F 00F0

```

```

C7198400 0
C7199400 0
0720C000 0
0720E100 0
0720F400 0
07203400 0
07204400 0
07205000 0
07206400 0
07207000 0
07208400 0
07209000 0
07210000 0
07211000 0
07212400 0
07213400 0
07214000 0
07215000 0
07216000 0
07217000 0
07218000 0
07219000 0
07221000 0
07222400 0
07223000 0
07223400 0
07224000 0
07225000 0
07226000 0
07227000 0
07228400 0
07229000 0
07230000 0
07231000 0
07232000 0
07233000 0
07234000 0
07235000 0
07236000 0
07237000 0
07238000 0
07239000 0
07240000 0
07241000 0
07242000 0
07243000 0
07244000 0
07245000 0
07246000 0
07247000 0
07248000 0
07249000 0
07250000 0
07251000 0
07252000 0
07253000 0
07254000 0
07255000 0
07256000 0
07257000 0

% WRITE OUT NEW(CR(A))
% SET THE CONDITION BITS
%
% RL TYPE ALG LEFT DOUBLE SHIFT
% (CR(A),R(A+1)), H (0-3)
% ZERO FILL, SET CC, AND SET OVERFLOW
%
% *M* INTO A2
% ISOLATE *A* FIELD
% TEMP STORAGE OF R(A)
% (R(A)) INTO P
%
% *M* INTO A2
% R(A+1)
% (R(A+1)) INTO B
% A3 = (R(A))/(R(A+1))
%
% SET THE OVERFLOW BIT
% SET THE CONDITION BITS
%
% OUTPUT (CR(A+1))
% REFERENCE PRI
% R(A)
%
% OUTPUT (R(A))
%
% RL TYPE CIRCULAR LEFT DOUBLE SHIFT
% (CR(A),R(A+1)), H (0-3) AND SET CC
% *M* INTO A2
%
% *A* INTO B
% TEMP STORAGE
% (R(A)) INTO B
%
% P(A+1)
% (CR(A+1)) INTO P
% A3 = (R(A))/(R(A+1))

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1662 4809 2F5C 0C1C C0F0
1663 2F3C 0C0C 0C00 0C60
1664 203C 0C5C 203C 0C60
1665 4809 C5C5 203C 0C60
1666 4889 C5E5 0C4C 0C60
1667 78C9 0C60 0C00 0C60
1668 1E7C 0C0C 0C0C 0C60
1669 4F1C 0C0C C67C 0C60
1670 4969 0C0C 0C0C 0C60
1671 4809 0C0C 0C0C 0C60
1672 4859 0C4C 2C00 C0F0
1673 0C0C 0C0C 0C00 C0F0
1674 4809 C40C 0C0C 0C60
1675 2F50 0C0C 0C00 C060
1676 56EC 0C00 0C00 C040

1677 228C 0C0C 0C00 0C60
1678 4809 C41C 203C 0C60
1679 0C0C 0C0C 0C00 0C40
167A 4809 E155 0C3C 0C60
167B 4809 0C41 0C0C 0C60
167C 4809 C40C 0C9C 0C60
167D 78C9 0C0C 0C0C 0C60
167E 1E7C 0C0C 700C C060
167F 4F1C 0C0C 0C0C 0C60
1680 4809 0C0C 0C00 0C60
1681 4809 0C40 8E3C 0C60
1682 0C0C 0C0C 0C3C 0C20
1683 200C 0C0C 0C30 0C60
1684 2F5C 0C0C 0C00 C060
1685 56EC 0C00 C00C 0C40

1686 4809 0C40 8E30 C0F0
1687 3C0C 0C0C 0C00 0C60
1688 4809 2F55 0C3C 0C60
1689 4809 E155 0C3C 0C60
168A 51C0 0C0C 0C00 C060
168B 4809 C41C 0C70 0C60
168C 0C0C 0C0C 0C30 C0C0
168D 2F3C 0C0C C4CC C06C
168E 4809 C41C 2C3C C0F0
168F 0C1C C0C0 0C0C C040
1690 4809 2F5C C61C C060
1691 2F3C C0C0 0C7C 0C60
1692 4809 C5C5 2030 C0F0
1693 4809 C40C 0C70 C0F0
1694 78C9 0C0C 0C0C 0C60

X R(A+1)
X (R(A+1)) INTO B
X A2 = (R(A))/(R(A+1))
X INPUT - 1 = CPCCR
A2 OR B MAR = MAR2
A2 OR B = A2, BHI
A2 - 9 = MIR, SET LCI
IF ADV THEN SET LCI
CARRY - 1 = CPCCR
CHECKOV - 1 = CPCCR
PMI | SET LCI
SE1CCA - 1 = CPCCR
DMI
B L = A2
COMP 16 = SAR
B R = B
166E 4809 C40C 8E3C 0C60
166F 4809 C0C0 8E3C 0C60
1670 2F50 0C0C 0C0C 0C60
1671 4809 0C0C C3C0 20F0
1672 4859 0F4C 801C 0C60
1673 0C0C 0C0C 0C00 C0F0
1674 4809 C40C 0C0C 0C60
1675 2F50 0C0C 0C00 C060
1676 56EC 0C00 0C00 C040

CONTENSIRA - 1 = CPCCR
B L = A2
COMP 16 = SAR, I 15 = LIT
A3 AND LIT = B
B L = B
A2 + B = MIR
IF ADV THEN SET LCI
CARRY - 1 = CPCCR
CHECKOV - 1 = CPCCR
DMI
B R = MIR*B
16 = SAR
SE1CCA - 1 = CPCCR
EOUTPUT - 1 = CPCCR
OPCODE - 1 = MPCR

X TYPE RL LITERAL ADD, (R(A))*H -> R(A)
X SET CC, CARRY AND OV BITS
X (R(A)) INTO E
X ISOLATE *M* FIELD
X *M* INTO MS WORD OF R
X PERFORM ADDITION
X SET THE CONDITION BITS
X (R(A))*H INTO R(A)
X
X TYPE RL LITERAL ADD DOUBLE
X (R(A))*(A+1) + H INTO R(A)*P(A+1)
X SET CC, CARRY, AND OV BITS
X **M* INTO MIR
X ISOLATE *M* FIELD
X (R(A)) INTO MAR2
X TEMP STORAGE
X (R(A)) INTO G
X (R(A)) INTO MS WORD OF A2
X R(A+1)
X (R(A+1)) INTO B
X A2 = (R(A))/(R(A+1))

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0P622:

0P623:



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1695 1E70 0000 007C 00A0
CHECKOV - 1 = CPCH
1696 4F10 00C0 0070 00E0
BHL1 SET LC1 = CPCH
1697 49C4 00C0 0070 00E0
SETCCA - 1 = CPCH
1698 200C 00C0 0070 C060
6*1
1699 4809 00C0 0070 C0F0
B.L = A2
1700 000C 00C0 2030 C0F0
CDMP 16 = SAR
1701 4809 00C4 0070 C0E0
R.R = B
1702 4809 00C0 8070 00F0
A2 R = MIR
1703 4809 00C0 8070 00F0
FOUIPUT - 1 = CPCH
1704 4809 00C0 8070 00F0
ASR
1705 4809 00C0 8070 00F0
B*HAR R = MAR2
1706 4809 00C4 8070 00F0
B = SAR
1707 4809 00C0 0070 C0A0
FOUIPUT - 1 = CPCH
1708 4809 00C4 0070 C0E0
OPCODE - 1 = MPCK
1709 4809 00C0 0070 C0E0
OPCODE631: XFCODE - 1 = CPCH
A2 + AMPCR = AMPCR
1710 4809 00C0 0070 C0E0
DP63F - 1 = AMPCR
1711 4809 00C0 0070 C0E0
STEP
1712 4824 00C0 0070 00F0
EXEC
1713 4809 00C0 0070 C0E0
OP63F1: OP630 - 1 = MPCK
1714 4809 00C0 0070 C0E0
OP630 - 1 = MPCK
1715 4809 00C0 0070 C0E0
OP632 - 1 = MPCK
1716 4809 00C0 0070 C0E0
OP633 - 1 = MPCK
1717 4809 00C0 0070 C0E0
OP630:
LIT AND B = B
1718 4809 00C0 0070 C0E0
15 = LITI 4 = SAR
P = MIR
1719 4809 00C4 0070 C0E0
A3 R = B
1720 4809 00C0 0070 C0E0
LIT AND E = B
1721 4809 00C0 0070 C0E0
REGSTACK - 1 = CPCH
1722 4809 00C0 0070 C0E0
FOUIPUT - 1 = CPCH
1723 4809 00C0 0070 C0E0
SET00 - 1 = CPCH
1724 4809 00C0 0070 C0E0
OPCODE - 1 = MPCK
1725 4809 00C0 0070 C0E0
OP631:
LIT AND B = MIR
1726 4809 00C0 0070 C0E0
15 = LIT
1727 4809 00C0 0070 C0E0
CONTERISRA - 1 = CPCH
1728 4809 00C4 0070 C0E0
B.L = A2 + BHL
1729 4809 00C0 0070 C0E0
COMP 16 = SAR
1730 4809 00C4 0070 C0E0
B.L = B
1731 4809 00C0 0070 C0E0
SETCC - 1 = CPCH
1732 4809 00C0 0070 C0E0
A2 - B = MIR; SET LC2
IF ADV THEN SET LC1
1733 4809 00C0 0070 C0E0
CARRY - 1 = CPCH
1734 4809 00C0 0070 C0E0
CHECKOV - 1 = CPCH
1735 4809 00C0 0070 C0E0
OPCODE - 1 = MPCK
1736 4809 00C0 0070 C0E0
OP631:
1737 4809 00C0 0070 C0E0
1738 4809 00C0 0070 C0E0
1739 4809 00C0 0070 C0E0
1740 4809 00C0 0070 C0E0
1741 4809 00C0 0070 C0E0
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1762 4809 00C0 0070 C0E0
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2000 4809 00C0 0070 C0E0

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14C4 2009 0C40 0030 C0FC  
 14C5 0CFC 0C50 C070 00F0  
 14C6 0009 2C5C 0000 00F0  
 14C7 51C0 0C00 0000 C060  
 14C8 0009 0F41 C070 C0FC  
 14C9 0000 0000 0000 0030  
 14CA 0009 0F45 0000 C0FC  
 14CB 51C0 0C00 0C30 C060  
 14CC 2F30 0C00 C070 C060  
 14CD 0009 0E55 2000 00F0  
 14CE 0CFC 0C00 0000 00E0  
 14CF 4C60 0F00 0F30 C060  
 14D0 0009 0E00 0C80 00F0  
 14D1 2000 0C00 0000 C060  
 14D2 0009 0E01 0030 00F0  
 14D3 0000 0000 C070 C060  
 14D4 0009 0C80 0E30 00F0  
 14D5 2F50 0C00 C030 C060  
 14D6 0009 0F00 0000 20F0  
 14D7 0009 0F00 0000 0010  
 14D8 0009 0E00 0E30 00F0  
 14D9 0000 0C00 0E30 0020  
 14DA 2F50 0C00 0000 C06C  
 14DB 0009 0E00 0000 0060  
 14DC 0009 0E00 0000 0040

14DD 0009 2C55 0000 00F0  
 14DE 0CFC 0C50 0C30 00AC  
 14DF 0009 0C41 0E30 00F0  
 14E0 0009 0C00 0E00 00FC  
 14E1 5000 0C00 0E30 00C0  
 14E2 0009 2C55 0C80 00F0  
 14E3 51C0 0C00 0E00 C06C  
 14E4 0009 0F41 0E20 00F0  
 14E5 0000 0C00 0000 0030  
 14E6 2F30 0C00 0000 0060  
 14E7 0009 0C41 2070 00F0  
 14E8 0C00 0C00 0000 0C2C  
 14E9 0009 0F00 0000 00FC  
 14EA 51C0 0C00 0000 0060  
 14EB 2F30 0C00 0000 006C  
 14EC 0000 0000 0000 00F0  
 14ED 2400 0000 0000 00F0  
 14EE 0009 0000 0000 00F0  
 14EF 0009 0F00 0E1C 00F0  
 14F0 0000 0C00 0000 0010  
 14F1 0009 0C00 0F00 00FC  
 14F2 2F50 0C00 0000 0060  
 14F3 0009 0C00 0000 00FC  
 14F4 2000 0000 0000 C060  
 14F5 0009 0F45 0000 00F0  
 14F6 51C0 0C00 0C30 C060  
 14F7 2F50 0C00 C070 C06C  
 14F8 5050 0C00 C000 C06C

% TYPE RL LITERAL MULTIPLY  
 % R(A+1) X H = (R(A),R(A+1)), SET CC  
 % ISOLATE "A"  
 % TEMP STORAGE  
 % R(A+1)  
 % R(A+1) INTO PAR2  
 % (R(A+1)) INTO B  
 % "H" INTO A2  
 % R(A+1) X H INTO A3  
 % PRODUCT INTO B, MIR  
 % SET THE CONDITION BITS  
 % (R(A+1))  
 % REF FRI  
 % R(A)  
 % (R(A))  
 % TYPE RL LITERAL DIVIDE  
 % (R(A),R(A+1))/H = R(A+1), REMAINDER  
 % INTO R(A), SET CC AND OV  
 % ISOLATE "H"  
 % LEFT JUSTIFY DIVISOR  
 % ISOLATE "A"  
 % R(A) INTO MAR2  
 % STORE R(A)  
 % R(A+1) INTO E  
 % R(A+1)  
 % R(A+1) INTO MAR2  
 % (R(A+1)) INTO B  
 % (R(A),R(A+1))/H  
 % REF FRI  
 % R(A)  
 % REMAINDER  
 % QUOTIENT INTO B, MIR  
 % SET THE CONDITION CODE  
 % R(A+1)  
 % R(A+1) INTO PAR2  
 % QUOTIENT INTO R(A+1)  
 % <ET OV BIT  
 B R = B; IF LCI  
 4 = SARI; 15 = LLI  
 LIT AND 0 = B  
 REGSTACK - 1 = CPCR  
 PHAR L = BR1  
 COMP 8 = SAR  
 BHAR + 1 = B  
 REGSTACK - 1 = CHCR  
 EINPUT - 1 = CPCR  
 A3 AND LIT = A2  
 15 = LIT  
 MULT - 1 = CPCR  
 A3 = B; MIR  
 SEITCCA - 1 = CPCR  
 A3 L = B  
 COMP 16 = SAR  
 B R = MIR  
 ASR  
 REGSTACK - 1 = HARR  
 8 = SAR  
 A3 R = MIR  
 16 = SAR  
 EINPUT - 1 = CPCR  
 OPCODE - 1 = HPCR  
 LIT AND 0 = B  
 15 = LIT; COMP 16 = SAR  
 B L = MIR  
 A3 R = B  
 4 = EAR  
 LIT AND 0 = C  
 REGSTACK - 1 = CPCR  
 BHAR L = BR1  
 COMP 8 = SAR  
 EINPUT - 1 = CPCR  
 R L = A2  
 COMP 16 = SAR  
 BHAR + 1 = B  
 REGSTACK - 1 = CPCR  
 EINPUT - 1 = CPCR  
 A2 OR B = A2; BRIT; SET LCI  
 A2 = (R(A))/R(A+1)  
 A3 - 1 = CPCR  
 PHAR R = HARR  
 8 = SAR  
 A2 = MIR  
 EINPUT - 1 = CPCR  
 A3 = B; MIR  
 BHAR + 1 = B  
 REGSTACK - 1 = CPCR  
 EINPUT - 1 = CPCR  
 CLEAROV - 1 = CPCR













```

1758 2200 0000 0000 0060
1759 4809 0C41 203F 00F0
1750 0000 0000 0000 0020
1751 3808 0000 0000 00F0
1752 26FC 0000 0000 0040
1753 4809 0C40 880C 00F0
1754 1761 0000 0000 0030
1755 4809 0C41 180C 00F0
1756 4849 C65E 0050 00F0
1757 78C9 0000 0000 00F0
1758 1E70 0000 0000 0060
1759 4F1C 0000 0000 0060
1760 4809 1000 0000 00F0
1761 7668 0000 0000 0070
1762 2000 0000 0030 0040
1763 680C 0000 0030 0040
1764 4809 0C41 0000 00F0
1765 0000 0000 0000 00C0
1766 0000 0000 0000 0000
1767 763F 0000 0000 0050
1768 5F90 0000 0000 0060
1769 4809 C640 0C40 00F0
1770 2100 0000 0020 00C0
1771 4809 0000 0000 00F0
1772 4824 0000 0030 00F0
1773 4E5C 0000 0000 0040
1774 4E50 0000 0000 0040
1775 4E50 0000 0000 0040
1776 4E50 0000 0000 0040
1777 2110 0000 0000 0040
1778 4809 0000 0000 00F0
1779 5009 0C41 203F 00F0
1780 4809 0C41 203F 00F0
1781 3808 0000 0000 00C0
1782 212C 0000 0030 0040
1783 4809 0C40 3030 00F0
1784 4809 0C41 100F 00F0
1785 0000 0000 0030 00C0
1786 4809 0C41 100F 00F0
1787 0000 0000 0000 00C0
1788 4849 C65E 0050 00F0
1789 78C9 0000 0000 00F0
1790 4F1C 0000 0000 0060
1791 4809 E00C 0000 00F0
1792 200C 0000 0000 0060
1793 4E50 0000 0000 0040
1794 4E50 0000 0000 0040
1795 2110 0000 0000 0040
1796 4809 0000 0000 00F0
1797 5009 0C41 203F 00F0
1798 4809 0C41 203F 00F0
1799 3808 0000 0000 00C0
1800 212C 0000 0030 0040
1801 4809 0C40 3030 00F0
1802 4809 0C41 100F 00F0
1803 0000 0000 0030 00C0
1804 4809 0C41 100F 00F0
1805 0000 0000 0000 00C0
1806 4849 C65E 0050 00F0
1807 78C9 0000 0000 00F0
1808 4F1C 0000 0000 0060
1809 4809 E00C 0000 00F0
1810 200C 0000 0000 0060

```

```

CONTENTSRA - 1 = CFCR
B L = A2, BHI
COMP 16 = SAR
IF LC2 THEN STEP ELSE SKIP
LS663 - 1 = MPCR
R R = R
24 = SAR
B L = B, A3
COMP 16 = SAR
A2 - B = MIRJ SET LC2
IF ADV THEN SET LC1
CARRY - 1 = CFCR
CHECKOV - 1 = CFCR
A3 = B
SECC - 1 = CFCR
OPCODE - 1 = MPCR
B L = B, CSAR
COMP 8 = SAR
D R = B, A3
C663 - 1 = MPCR
OPCODE671, XFCODE - 1 = CFCR
A2, AMPCR = AMPCR
OP67F - 1 = AMPCR
STEP
EXEC
OP67F: N0TIHP - 1 = MPCR
N0TIHP - 1 = MPCR
OP673 - 1 = MPCR
OP673:
SET LC2
RXMFIELD - 1 = CFCR
B L = B#2
COMP 8 = SAR
EMULIN - 1 = CFCR
B L = MIR
COMP 16 = SAR
A3 = B
CONTENTSRA - 1 = CFCR
B L = A2, BHI
COMP 16 = SAR
IF LC2 THEN STEP ELSE SKIP
LS673 - 1 = MPCR
B R = B
24 = SAR
COMP 16 = SAR
B L = B, A3
A2 - B = MIRJ SET LC2
IF ADV THEN SET LC1
CARRY - 1 = CFCR
CHECKOV - 1 = CFCR
A3 = B
SECC - 1 = CFCR

```

```

07618000 0
07619000 0
07620000 0
07621000 0
07622000 0
07623000 0
07624000 0
07625000 0
07626000 0
07627000 0
07628000 0
07629000 0
07630000 0
07631000 0
07632000 0
07633000 0
07634000 0
07635000 0
07636000 0
07637000 0
07638000 0
07639000 0
07640000 0
07641000 0
07642000 0
07643000 0
07644000 0
07645000 0
07646000 0
07647000 0
07648000 0
07649000 0
07650000 0
07651000 0
07652000 0
07653000 0
07654000 0
07655000 0
07656000 0
07657000 0
07658000 0
07659000 0
07660000 0
07661000 0
07662000 0
07663000 0
07664000 0
07665000 0
07666000 0
07667000 0
07668000 0
07669000 0
07670000 0
07671000 0
07672000 0
07673000 0
07674000 0
07675000 0
07676000 0
07677000 0

```



```

178E 238C 68C0 C000 006C
1790 9809 0C46 0C30 09F0
1791 2F5C 0003 0030 0060
1792 66E0 0003 0000 0040
1793 9809 0C41 0800 40FC
1794 00FC C0C0 FC00 0030
1795 9809 0C40 9830 09F0
1796 788C 0C03 0C00 0050

CONTENTS#N - 1 = CPCR X (RCH) INTO B
B + 1 = MIR X (RCH) + 1
EOUTPUT - 1 = CPCR
OPCODE - 1 = HPCR
L5673: B L = B, CSAR
      C OMP 8 = SAR
      R R = B, A3
      C673 - 1 = HPCR

1797 4E5C 0C00 0C00 004C
1798 4E5C 0C03 0000 0040
1799 4E50 0C00 0C00 0040
179A 4E50 0C00 0030 0040
179B 4E50 0C00 0000 0040
179C 4E50 0C00 0030 0040
179D 4E50 0C00 0000 0040
179E 300C 0C00 0C00 0040
179F 0000 0C00 0000 0040
1784 792C 0C00 0000 005C
1777 777C 0000 0000 6050
1771 773C 0000 0000 6000
175F 764C 0000 0000 005C
1752 7520 0C03 0000 005C
174C 746C 0000 0000 000C
1737 734C 0000 0000 005C
1724 726C 0000 0030 0050
170F 7100 0C03 0000 0050
1702 702C 0000 0030 0050
16FC 6FE0 0000 0000 000C
16AD 50CC 0000 0030 0050
164C 6030 0C03 0000 0050
16AB 586C 0000 0000 0050
16AA 5A0C 0000 0030 0050
1647 6A9C 0C03 0C00 0000
1648 6850 0C03 0000 0050
1647 576C 0000 0030 0050
1646 6570 0000 0030 0050
1645 648C 0000 0000 0050
1642 644C 0C03 0000 0000
16DA 623C 0C00 0000 0050
1509 6020 0000 0000 0050
1508 5EE0 0000 0000 0050

OPCODE70: NOTIMP - 1 = HPCR
OPCODE71: NOTIMP - 1 = HPCR
OPCODE72: NOTIMP - 1 = HPCR
OPCODE73: NOTIMP - 1 = HPCR
OPCODE74: NOTIMP - 1 = HPCR
OPCODE75: NOTIMP - 1 = HPCR
OPCODE76: NOTIMP - 1 = HPCR
OPCODE77: FAULT - 1 = HPCR

TEND
END

```



1507 50AD 0000 0C10 0C5C  
1504 506C 00C0 0C90 0000  
1573 5AA0 0000 0030 0050  
1572 58FC 0000 0000 0050  
1571 579C 0000 000C 0050  
1570 573C 00C0 0000 0050  
1560 56FC 0000 0C00 000C  
1550 52E0 0000 0000 0050  
1549 5220 0000 0000 0050  
1524 5200 00C0 0C00 0050  
1523 5200 0000 0C00 0000  
14F5 50FC 00C0 0000 0050  
14F3 506C 00C0 0000 0050  
14F2 4F5C 0000 000C 005C  
14EE 4F1C 0000 0C00 0000  
14B2 404F 0000 0070 005C  
14B1 4C50 00C0 0000 0050  
14B0 40E0 0C00 0070 005C  
14AF 482C 00C0 0070 0050  
14AC 4AEC 0000 000C 0000  
1470 495C 00C0 0C00 0050  
146F 4820 00C0 000C 0050  
146E 47CC 0000 0C00 0050  
146D 470C 0C00 0C70 0050  
146A 46C0 0000 000C 0000  
1436 456C 00C0 0000 005C  
1435 4450 0000 0C00 005C  
1434 4400 0000 0C50 0050  
1433 4320 0000 000C 005C  
1430 4320 00C0 000C 005C  
13FF 41FC 0000 0C00 0050  
13FE 40EC 0000 000C 0050  
13FD 4090 0C00 0000 0050  
13FC 3FFC 0000 0C00 005C  
13F9 37BC 00C0 000C 0000  
13B2 3E60 00C0 0C00 0050  
13B1 300C 0000 000C 005C  
13B0 302C 0000 0C00 0050  
13AC 3AEP 00C0 0000 0000  
1274 396F 00C0 000C 0050  
1270 3800 0000 0C00 0050  
136E 371C 0000 0C00 0050  
136B 3600 0000 0C00 0000  
1328 353C 0000 000C 0050  
1324 3300 0000 0C00 005C  
1329 338C 0000 0C00 0050  
1328 328C 0000 000C 0050  
1225 3270 00C0 0C50 0000  
12FA 3180 0000 000C 0050  
12F7 305C 0000 0C00 005C  
12F4 2EAC 0000 0C00 005C  
1274 2E10 0000 0050 0050  
1274 2E10 0000 0050 0050  
1273 2E10 0000 0C00 005C  
1258 2F10 0000 0C00 0050  
1255 2F10 0000 0C00 0050  
1250 2F10 0000 0C00 0050  
1240 2F10 0000 000C 0050  
120C 2F10 0000 0C50 0050  
1207 2F10 0000 000C 005C









01.20 C300 0000 0000 0040  
01.2A C20C 0000 0000 00C0  
01DE F15C 0000 0000 0040  
01DD F00C 0000 0000 0040  
01DC F0C0 0000 0000 0040  
01DD F0EC 0000 0000 0040  
01DD F0A0 0000 0000 00C0  
015E EAD0 0000 0000 0040  
015C E85F 0000 0000 0040  
0158 E5A0 0000 0000 00C0  
0100 E410 0000 0000 0040  
01FF E270 0000 0000 0040  
01FE E120 0000 0000 0040  
01FD E00C 0000 0000 0040  
01FA 0FC0 0000 0000 00C0  
0179 0C0C 0000 0000 0040  
0077 044C 0000 0000 0040  
0076 079C 0000 0000 0040  
0073 075C 0000 0000 00C0  
0119 050C 0000 0000 0040  
0118 042C 0000 0000 0040  
0117 0200 0000 0000 0040  
0115 015C 0000 0000 0040  
010E 004C 0000 0000 0040  
00BE 0E30 0000 0000 0040  
00BD 2000 0000 0000 0040  
00BC 20F0 0000 0000 0040  
01B9 C880 0000 0000 00C0  
0032 C900 0000 0000 0040  
0031 C710 0000 0000 0040  
0030 C560 0000 0000 0040  
002F C320 0000 0000 0040  
002C C2E0 0000 0000 00C0  
00D5 C100 0000 0000 0040  
00D4 BF9C 0000 0000 0040  
00D3 BEBC 0000 0000 0040  
01D2 B05C 0000 0000 0040  
00CF B010 0000 0000 00C0  
00BC BC60 0000 0000 0060  
0097 B430 0000 0000 0040  
0096 B700 0000 0000 0040  
0095 B40C 0000 0000 0040  
0094 B40C 0000 0000 0040  
0093 B20C 0000 0000 0040  
0092 B00C 0000 0000 0040  
0091 B38C 0000 0000 0040  
0090 B0C0 0000 0000 0040  
0088 B0C0 0000 0000 0040  
0087 AEF0 0000 0000 0040  
0086 A50C 0000 0000 00C0  
0085 AC00 0000 0000 0040  
0084 AA3C 0000 0000 0040  
0083 A91C 0000 0000 0040  
0082 A72C 0000 0000 0040  
0081 A66C 0000 0000 00C0  
0080 A5DF 0000 0000 00C0  
0079 A30C 0000 0000 0040  
0078 A360 0000 0000 0040  
0077 A1F0 0000 0000 00C0



0419 A19C 00C0 0000 00C0  
0420 A120 00C0 0070 0040  
0405 A000 00C0 0070 0040  
0900 9F8C 00C3 0070 0040  
090C 9E7C 0000 0000 0040  
090A 9D00 00C0 0070 0040  
0907 9U90 00C3 0070 00C0  
0998 99EC 00C0 0020 0040  
0989 9A4C 00C3 0070 0040  
0938 9880 00C3 0000 0040  
0935 987C 00C0 0000 00C0  
0962 97FC 00C0 0030 0040  
0960 970C 0000 0000 0040  
095F 9620 00C0 0000 0040  
095C 95EC 0000 0000 00C0  
0934 9570 0000 0030 0040  
0932 9420 0000 0020 0040  
0931 9340 00C3 0000 0040  
092E 930C 0000 0070 00C0  
0909 90F0 00C0 0000 0040  
0900 90CC 00C3 0040 0040  
08FE 90FC 0000 0070 0040  
08A7 8A8C 00C0 0030 0040  
089E 8FC0 00C0 0000 0040  
0880 8U80 00C3 0070 0040  
086C 9C8C 00C0 0000 0040  
0898 88EC 00C0 0030 0040  
0888 88A0 0000 0030 00C0  
0890 216C 0000 0000 0040  
0670 8800 00C0 0070 0040  
087A 37CC 00C0 0020 00C0  
07FF 8420 0000 0070 0040  
07FE 82CC 00C3 0000 0040  
07ED 822C 0000 0000 0040  
07FB 812C 00C3 0030 0040  
07FA 809C 00C0 0000 0040  
07E9 7FFC 00C0 0030 0040  
07E3 7F80 00C3 0070 00C0  
07EF 351C 0000 0030 0040  
07EG 7EFC 00C3 0020 0040  
07E7 7E80 0000 0000 00C0  
07E5 777C 00C0 0000 0040  
07E4 7700 0000 0000 0040  
07E3 7000 00C0 0030 0040  
0730 7C30 00C3 0070 0040  
073C 7E60 0000 0020 0040  
0738 7A90 00C0 0000 0040  
0739 7A3C 00C3 0000 0040  
0738 7880 00C0 0030 0040  
0737 77F0 00C0 0000 0040  
0735 7500 00C0 0030 0040  
0734 74F0 00C0 0000 0040  
0733 73E0 0000 0020 0040  
0720 7320 0000 0000 00C0  
0724 7E3C 00C0 0000 0040  
0722 700C 00C0 0070 0040  
0721 7240 00C0 0030 0040  
071E 720C 0000 0070 00C0



0600 7000 0000 0000 0040  
060C 5F80 0000 0000 0040  
060B 5C9C 0000 0000 0040  
060A 600C 0000 0000 0040  
0607 509C 0000 0000 0000  
0604 6C00 0000 0000 0040  
060E 6000 0000 0000 0000  
060C 790C 0000 0000 0050  
0609 7900 0000 0000 0050  
0608 7940 0000 0000 0050  
0687 799C 0000 0000 0050  
0636 7980 0000 0000 0050  
0685 797C 0000 0000 0050  
06B4 796C 0000 0000 0050  
06B3 76EC 0000 0000 0050  
06B2 749C 0000 0000 0050  
06B1 7210 0000 0000 0050  
0680 6F9C 0000 0000 0050  
06AF 6440 0000 0000 0050  
06AE 53F0 0000 0000 0050  
06AD 5010 0000 0000 0050  
06AC 56AC 0000 0000 0050  
06AB 565C 0000 0000 0050  
06AA 568C 0000 0000 0050  
06A9 524C 0000 0000 0050  
06A8 4E00 0000 0000 0050  
06A7 4E00 0000 0000 0050  
06A6 4E40 0000 0000 0050  
06A5 4E30 0000 0000 0050  
06A4 419C 0000 0000 0050  
06A3 4670 0000 0000 0050  
06A2 4670 0000 0000 0050  
06A1 420C 0000 0000 0050  
06A0 3F6C 0000 0000 0050  
069F 3A9C 0000 0000 0050  
069E 368C 0000 0000 0050  
069D 3220 0000 0000 0050  
069C 2A50 0000 0000 0050  
069B 2A4C 0000 0000 0050  
069A 2A3C 0000 0000 0050  
0699 238C 0000 0000 0050  
0698 1E2C 0000 0000 0050  
0697 1710 0000 0000 0050  
0696 133C 0000 0000 0050  
0695 0F50 0000 0000 0050  
0694 0B7C 0000 0000 0050  
0693 00E0 0000 0000 0050  
0692 F830 0000 0000 0040  
0691 F27C 0000 0000 0040  
0690 E050 0000 0000 0040  
068F E53C 0000 0000 0040  
068E DF7C 0000 0000 0040  
068D D100 0000 0000 0040  
068C C86C 0000 0000 0040  
068B C66C 0000 0000 0040  
068A C290 0000 0000 0040  
0689 BCC0 0000 0000 0040  
0688 B58C 0000 0000 0040  
0687 A10C 0000 0000 0040





0686 A690 00C0 0C00 C040  
0685 A16C 00C0 0000 0040  
0684 704C 00C0 0000 0040  
0683 982C 0000 0C00 0040  
0682 959C 00C0 0C0C 0040  
0681 220C 00C0 0C00 0040  
0680 9770 00C0 0000 0040  
067F 7E60 00C0 0070 0040  
067E 7190 00C0 0030 0040  
067D 6000 00C0 003C 0040  
067C 8700 0000 000C 0040  
067B 8700 0000 000C 0040  
067A 64F0 0000 0C00 0040  
0679 64F0 00C0 002C 0040  
0678 618C 00C0 0070 0040  
0677 6280 00C0 0000 0040  
0676 66E0 00C0 0070 0040  
0675 9E50 00C0 007C 0040  
0674 5050 0000 000C 0040  
0673 5B5C 0000 0C70 0040  
0672 585F 00C0 0C70 0040  
0671 5B0C 00C0 0C70 0040  
0670 5AB0 00C0 000C 0040  
066F 5A6C 00C0 002C 0040  
066E 5A1C 00C0 0C0C 0040  
066D 633C 00C0 0000 0060  
066C 6330 00C0 0C00 0060  
066B 586C 00C0 0000 0040  
066A 5930 00C0 0000 0040  
0669 586C 00C0 0C70 0040  
0668 5810 0000 003C 0040  
0667 56E0 00C0 0070 0040  
0666 5330 00C0 005C 0060  
0665 227C 00C0 0030 0040  
0664 3700 0000 000C 0040  
0663 3700 0000 000C 0040  
0662 5E50 00C0 007C 0060  
0661 5E50 00C0 000C 0060  
0660 5E50 0000 0C70 0060  
065F 5C4C 00C0 000C 0040  
065E 50A0 00C0 000C 0040  
065D 5050 00C0 0C00 0040  
065C 305C 00C0 0C70 0040  
065B 3C4C 00C0 007C 0040  
065A 4FFC 0000 0C0C 0040  
0659 4FFC 00C0 0C0C 0040  
0658 5050 00C0 0C70 0040  
0657 50F0 00C0 0000 0040  
0656 5800 00C0 000C 0060  
0655 50FC 0000 0070 0040  
0654 580C 00C0 0070 0060  
0653 4E20 00C0 0070 0040  
0652 4DFC 00C0 0C0C 0040  
0651 61EC 00C0 000C 0060  
0650 50E0 0000 0C7C 0060  
064F 31CC 0000 000C 0060  
064E 6000 00C0 000C 0060  
064D 60E0 00C0 0C0C 0060  
064C 47B0 00C0 0C0C 0060  
064B 60E0 00C0 0030 0060



046F 46F0 C003 0020 C040  
046D 51C0 0000 0000 C060  
0469 46FC 0000 C000 C040  
0467 51CC 0000 0000 C060  
0464 46FC C000 0000 C040  
0462 51CC 0000 0000 C060  
0461 50FC C000 0000 C040  
0459 46FC 0000 0000 C060  
0457 4690 05C0 C000 C040  
0456 4650 C0C0 0000 C040  
0455 4580 C0C0 0000 C040  
0452 4540 0000 C000 C060  
044A 50E0 0000 0000 C060  
0444 4440 0000 0000 C040  
0442 51C0 0000 0000 C060  
043E 4440 0000 0000 C040  
043C 4440 C000 0000 C040  
043A 51CC C000 0000 C060  
0436 50FC C000 0000 C060  
0431 43CC 0000 0000 C040  
0430 43CC 0000 0000 C040  
042F 437C 0000 0000 C040  
042E 4310 0000 0000 C040  
042B 4200 0000 0000 C060  
0425 44CC 0000 0000 C040  
0424 4250 0000 0000 C040  
041F 40CC 0000 0000 C060  
041E 40CC 0000 0000 C060  
0415 4330 0000 0000 C060  
0410 4160 0000 0000 C040  
0406 4330 0000 0000 C060  
0400 6650 C000 C000 C040  
03F0 66E0 C000 C000 C040  
03E3 3F70 0000 0000 C060  
03D5 66E0 0000 0000 C040  
02C8 3F70 0000 0000 C060  
02BE 4E5C C000 C000 C040  
02B0 3DC0 0000 0000 C040  
029C 3DE0 C000 0000 C040  
0289 3BB0 C000 C000 C040  
02AC 66E0 C000 0000 C040  
02A2 3F70 0000 0000 C060  
028E 66E0 0000 0000 C040  
0283 3F70 0000 0000 C060  
0276 4E50 0000 0000 C040  
0275 3990 0000 0000 C040  
0274 3F60 0000 0000 C040  
0271 3F30 0000 0000 C060  
025E 3E20 C000 0000 C040  
0257 41E0 0000 0000 C060  
0249 51E0 0000 0000 C060  
0240 50E0 0000 0000 C060  
0210 61EC 0000 0000 C060  
0214 60E0 C000 0000 C060  
020F 60E0 0000 0000 C060  
0205 50FC C000 0000 C040  
0201 5B00 0000 0000 C060  
02F0 2F30 0000 0000 C060  
02EC 2F30 0000 0000 C060



02E9 2F3C 00F0 00D0 0060  
02E6 2F3C 00F3 00D0 0060  
02E3 2F3C 00D3 00D0 0060  
02E0 2F3A 00F3 00F0 006C  
02D0 5E5C 00F3 00F0 0060  
02DC 5E5C 00F0 00D0 0060  
02DD 5E5F 00F0 00D0 0060  
02DA 5E5F 00F0 00F0 0060  
02DB 5E5F 00F0 00F0 0060  
02DB 5E5C 00F0 00D0 0060  
02C8 5E5C 00D3 00F0 006C  
02C5 5E5C 00F0 00F0 0060  
02C2 5E5C 00D0 00D0 0060  
02BA 2F50 00F0 00D0 0060  
02B1 2F50 00F0 00D0 0060  
029C 2F3C 00F0 005C 0060  
0294 2F50 00D0 00D0 0060  
028F 2F50 00D0 00D0 0060  
028C 2F5F 00F0 00D0 0060  
0289 2F5C 00F0 00D0 0060  
0286 2F5C 00F0 00D0 0060  
0283 2F5C 00F0 00D0 0060  
0281 566C 00F3 005C 004F  
027E 591C 00D3 00D0 0040  
0275 591C 00D3 00D0 0040  
0270 5E5C 00F3 00D0 0060  
0230 2F30 00F0 00D0 006C  
023C 51C0 00D0 00D0 0060  
0236 2F30 00D0 00D0 0060  
0230 51C0 00D0 00D0 0060  
0216 216F 00F3 00D0 0040  
0215 21F0 00D0 00D0 0040  
0213 2180 005C 00D0 0040  
020C 216C 00D0 00D0 0040  
020C 21F0 00D0 00F0 0040  
0209 21FA 00F0 00F0 0040  
0208 216C 00C0 00F0 004C  
0205 2090 00D3 00D0 0040  
0203 218C 00D0 00D0 0040  
01FB 2F5C 00D0 00F0 006C  
01EA 1E40 00D0 00C0 0040  
01E9 1EFC 00D0 00D0 004C  
01E1 566C 00D0 00D0 004C  
01DA 666C 00C3 00D0 0040  
0192 1940 00C0 00D0 0040  
0141 27FC 00D3 00D0 0040  
013C 194C 00D0 00F0 006C  
0129 169C 00D0 00D0 0040  
01DC 194C 00F0 00D0 006C  
00F7 0FB0 00F0 00D0 0040  
00F2 0FBC 00F0 00D0 004C  
00ED 0F7C 00D0 00C0 0040  
00EC 0F2C 00F3 00D0 004C  
00E9 0ED0 00D0 00D0 0040  
00B5 0B70 00F0 00D0 0040  
0092 0960 00F0 00D0 0040  
0077 0790 00D0 00D0 0060  
006E 0790 00C0 00D0 0060



CC1C 0810 C0C0 007C 0040  
 CC26 081C 0000 0000 0060  
 CC50 097C 00C0 0030 006C  
 CC5A 087C 00C3 0030 0060  
 CC59 0550C C0C0 003C 0040  
 CC51 5CFC 00C0 0030 0040  
 CC50 081C 00C0 000C 0060  
 CC49 051C 00C0 000C 0060  
 CC46 05EC 00C3 0070 0040  
 CC42 0510 00C0 000C 0060  
 CC41 0460 C7C0 0030 0060  
 CC16 060C 0000 007C 004C  
 CC15 1540 0000 0020 004C  
 CC12 1000 F0C0 0070 0040  
 CC2F 181C 00C7 0030 0040  
 CC2C 187C 00C0 C730 0040  
 CC29 1A4C 00C0 0070 004C  
 CC26 162C 00C0 000C 004C  
 CC23 1790 00C0 000C 004C  
 CC20 036C 00C0 0030 0040  
 CC1D 08F0 C000 0000 0040  
 CC1A 048C 0000 0030 0040  
 CC14 048C 0000 0000 0040  
 CC11 0000 0000 000C 0040  
 CC0A 002C 0000 003C 0040  
 CC07 06C0 0500 0030 0040

P ERRORS. 7714 CARDS. 36055 IOWENS.  
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