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EXPERIMENTATION AND DESIGN FOR A COMPUTER TO COMPUTER FIBER OPTIC DATA LINK

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NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

EXPERIMENTATION AND DESIGN
FOR A
COMPUTER TO COMPUTER FIBER OPTIC DATA LINK

by

Roland Daly Blocksom, Jr.

December 1975

Thesis Advisor: G. L. Sackman

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by

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

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December, 1975

ABSTRACT

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I. INTRODUCTION

A. OBJECTIVES

From the Corning announcement of a 20 dB/Km cable attenuation in 1970 to the recent announcement of experimental fiber optic cable materials with losses as low as 1-2 dB/Km , data communication applications using fiber optics has been expanding much like that experienced with the advent of the transistor in the 1950's. Much of the basic research for fiber optic systems including LED's (Ref. 1), detectors (Ref. 2), and the fiber cables themselves (Ref. 3), is complete and well known. Major commercial and military laboratories such as NELC, NRL, AFAL, BELL, CORNING, NIPPON ELECTRIC, AEG-TELEFUNKEN and others are turning out new design ideas such as the multi-terminal data bus, towed and moored sonar surveillance arrays, replacement of data carrying coaxial cables in aircraft (NELC A-7 ALOFT program), color multiplexing and commercial telephone land-line replacement (Ref. 4,5,6,7).

The object of this research was to apply basic fiber optic technology to a practical engineering application. The application selected was an attempt to link two microcomputers through a fiber optic medium.

A microcomputer laboratory facility was utilized in the link development. Two Intel Corporation Intellec 8 microcomputer development systems were used. Each system differed in configuration.

Although a high speed computer to computer link was not achieved, a demonstratable system involving microcomputer to

remote I/O device was achieved. Preliminary design for the high speed link is also included.

The work necessary to achieve an operational link included: a preliminary literature survey of fiber optics technology and state-of-the-art applications; study and familarization with the Intel microcomputer (hardware and program software); study of the ASR-33 teletype; and design, fabrication and test of an optical system to interface computer and peripheral device.

Documentation on the configuration status and modifications to the two microcomputers was not readily located creating some initial confusion. For that reason, all details of connections made and procedures followed in the demonstration are presented.

B. FIBER OPTICS AS A TRANSMISSION MEDIUM

The quantity of information that can be carried over a transmission channel is dependent on its frequency; the higher the frequency, the greater the channel capacity. the frequency of light is approximately 1000 times greater than the shortest radio waves, thus making this transmission medium a highly desirable and exploitable source for communications links (Ref. 8).

Fiber optic data transmission offers a potentially superior method of transmitting very high speed digital data (using standard IC logic components) as compared to conventional electrical wire systems. The ability of a pulse to retain its energy distribution, to propagate at a uniform rate, and not to reflect back to its source are primary areas of concern in high frequency applications. Fiber optical lines offer, as a minimum, RFI/EMI/noise immunity, total electrical isolation, transmission security,

low cross talk, no ringing, high environmental temperature capabilities, and extremely wide bandwidths.

Attenuation losses have been the major disadvantages of this transmission medium. Pulse dispersion due to varying velocities of propagation through discontinuities in glass also becomes a major disadvantage when discussing and designing digitally coded systems. The data-rate capability of a fiber optic bundle is determined by its dispersive and mode characteristics. A multi-mode fiber has a theoretical bandwidth/Km of 20-100 MHZ while the single mode fiber extends to 10 GHZ. A 1 GHZ bandwidth is equivalent to a 2000 Megabit capability. When talking of avionics or shipboard enviroments involving lengths of less than 300 M, the data rate is significantly higher.

Considerable effort has been expended over the past decade to harness the power and high frequency characteristics of light. Specifically, fiber optical cables or transmission lines have been developed for application in both analog and digital data links.

C. RECENT APPLICATIONS IN FIBER OPTICS

Fiber optic systems are generally regarded as being in a test bed stage at present. Many research and development facilities are building experimental systems and taking a hard look at trade offs. The following paragraphs indicate the current state-of-the-art in military and commercial applications.

The Naval Electronics Laboratory Center is regarded by most DoD fiber optics technologists as the 'leading lab' in applied research for fiber optic systems. However, through a tri-service group of experts, the military labs are sharing the job of applying technology to military

requirements. NELC currently has programs developed or in development in the avionics, shipboard, and underwater acoustic array areas.

As early as three years ago, NELC installed and operated a successful voice data link (ship phone circuit) aboard the cruiser USS LITTLE ROCK. The system linked six areas together carrying highly classified data (Ref. 9).

In the data bus area, NELC has been actively involved in a multi-terminal data bus concept (Ref. 4). They demonstrated a successful five terminal 5 Mb/s link early in 1974 using commercial components. This system was considered to be a prototype for an avionics data bus. The link was unidirectional and thus unsatisfactory in terms of their initial requirements. Further research is aimed at trading off complex techniques and achieving a bi-directional data flow. One current idea being actively pursued is that of 'color multiplexing'. This technique is a carrier frequency multiplexing in the optical spectrum.

Meanwhile, NELC has replaced conventional twisted wire pair connections between on board computers and pilot displays in the A-7 aircraft. The A-7 program (called ALOFT for Aircraft Light Optical Fiber Transmission) is currently planned for in-flight testing at the Naval Weapons Center ,China Lake, early next year. the current plan is for replacement of 302 twisted wire cables with 13 fiber optic cables (Ref. 9).

Other NELC applications include a TV transmission system on a Boeing 720 test bed with a follow on installation in USS KITTY HAWK for transferring CIC data to pilot ready rooms. All NELC applications are not aircraft oriented. Several programs exist today which are involved in tethering sonar arrays and moored surveillance systems.

Much of the problem in these areas relates to enviromental and physical cable stresses. At-sea prototype tests are being run presently. The NELC underwater cable programs are being done in conjunction with Corning, Simplex, and ITT. More details of these systems is unavailable in this report due to classification.

The Naval Sea Systems Command (NAVSEA) is developing a new system (Ref. 10) which wires together electronic systems on warships. The Shipboard Data Multiplex System (SDMS) multiplexs signals from radar, sonar, and missile systems onto 20 channels in 5 dispersed cables to route data throughout the ship. The data transfer needs will include voice and other wideband signals and could handle up to 95 % of all shipboard electronics needs. Rockwell International Autonetics won the competitive bid with twisted wire pair; however, it is significant that the RCA bid was for a fiber optics implementation.

The USAF is also interested in avionics fiber optics applications with their fly-by-wire systems and balloon over-the-horizon radar application (Ref. 11). Marconi-Elliot Avionics Systems of Kent, England is linking 3 aircraft computers to flight control systems in the YC-14 (medium STOL candidate). The data is serial format at 250 Kb/s transmitted by GaAs LED's through low loss multi-mode fiber and detected by p-i-n photodiode. The success of tests will determine further fiber optic applications possibly for engine control systems at a later date. RADC is looking at the radar balloon application. Essentially, an over-the-horizon radar will be balloon mounted and launched to 12,000 Ft (4 Km). Radar data transfer will be through a fiber optic tether. Since the fiber cable will be used, heavier microwave components can be eliminated and interference reduced.

The US Army Electronics Command is working on 3 major systems: a main trunking system up to 60 Km long (with repeaters); an 8 Km downlink to a command post; and a local communications link (to 1000 Ft) replacing coaxial 26-pair cable. The Army will utilize Corning's graduated-index cable for the first two applications (4 to 9 dB/Km) and possibly ITT's step-index 20 dB/Km cable for the 26-pair replacement (Ref. 9).

The latest commercial fiber optic applications include a Bell Canada affilliate analog system and Japanese point-point telephone microwave replacement, control systems use, and computer to computer links (Ref. 12,13).

Bell-Northern Research has announced the analog system for voice, high speed data, and color TV studio quality signal transmission. The system has a 15 MHZ bandwidth with data rates to 1.5 Mb/s. Systems components include a high radiance double hetero-structure GaAlAs LED, multi-mode 15 dB/Km fiber, and a p-i-n photodiode in a TO-18 header. The system also incorporates a unique splicing facility involving a stainless steel tube with index matching fluid inside. The cable is merely cut, ends butted together in the tube, and the tube ends crimped. The insertion loss is less than 1 dB using a 100 micron core cable.

Three Japanese teams are involved in fiber optic applications to upgrade the major power companies communications systems: (1) Nippon Electric and Sumitomo Electric Ind. Ltd. are developing a PCM optical system to transmit control data; (2) Hitachi Ltd and Hitachi Cable Ltd. are developing telemetry systems; and (3) Fujitsu Ltd. and Furukawa Electric are concentrating on high-speed optical picture transmission and computer to computer links. In a remarkable demonstration of the fiber optics cable ability to withstand high noise and interference, Nippon

Electric ran a 2.2 Km SELFOC cable next to a 150 KV power cable with error free operation at 7.8 Mb/s.

The applications mentioned are only to illustrate the current interest and wide applications, especially military, of fiber optics technology today. These applications are far from inclusive.

D. COMPUTER TO COMPUTER LINK DEVELOPMENT

1. Functional Data Flow

Figure 1. illustrates the functional block diagram of the demonstrated link (microcomputer to peripheral device). Although the demonstration involved only a simplex operation from System A to TTY-B, the reverse (microcomputer B to TTY-A) works exactly the same. This link operated at 110 baud. With an additional CRT on System B, the link speed would have been 1200 baud.

Figure 2 illustrates the high speed computer to computer link utilizing a TDMX scheme operating at a data rate of kilobits per second. The link requires an interrupt capability which has not yet been developed.

Figure 3 is the conceptual multi-terminal data bus (computers as terminals) utilizing wavelength multiplexing (Ref. 4). The concept of the multi-terminal system is very similar to the two computer high-speed link. Major changes would include transmitter modifications, modified systems software to handle interrupts, polling, and data format variations. In addition, bi-directional couplers remain to be fabricated and tested. At the present time, the PDP-11 computer is connected to the Intellec 8 system via an opto-isolator package (off the shelf). The computer to computer link operates at 1200 baud.

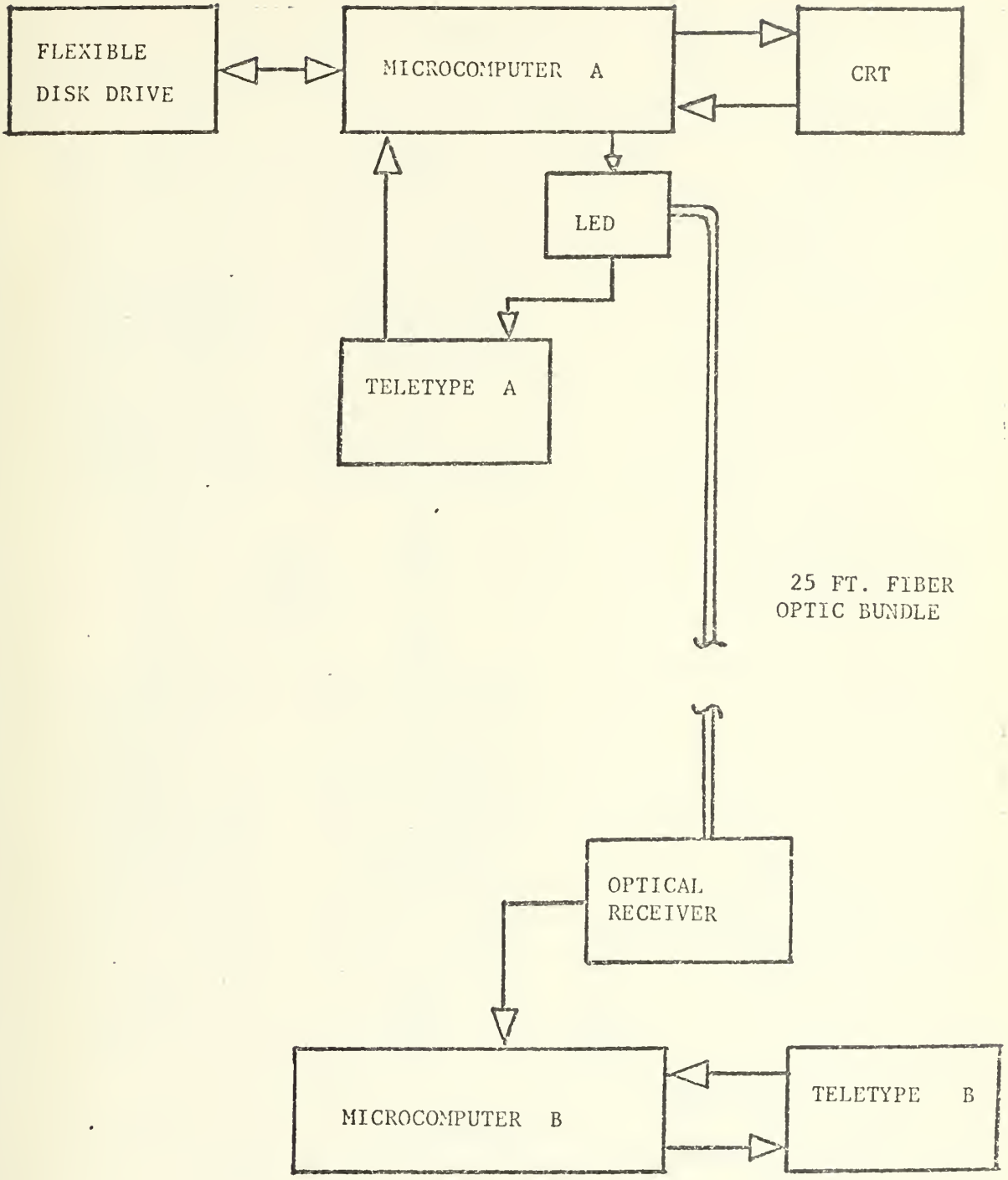


FIGURE 1.
OPTICAL LINK DEMONSTRATION
SIMPLEX MODE

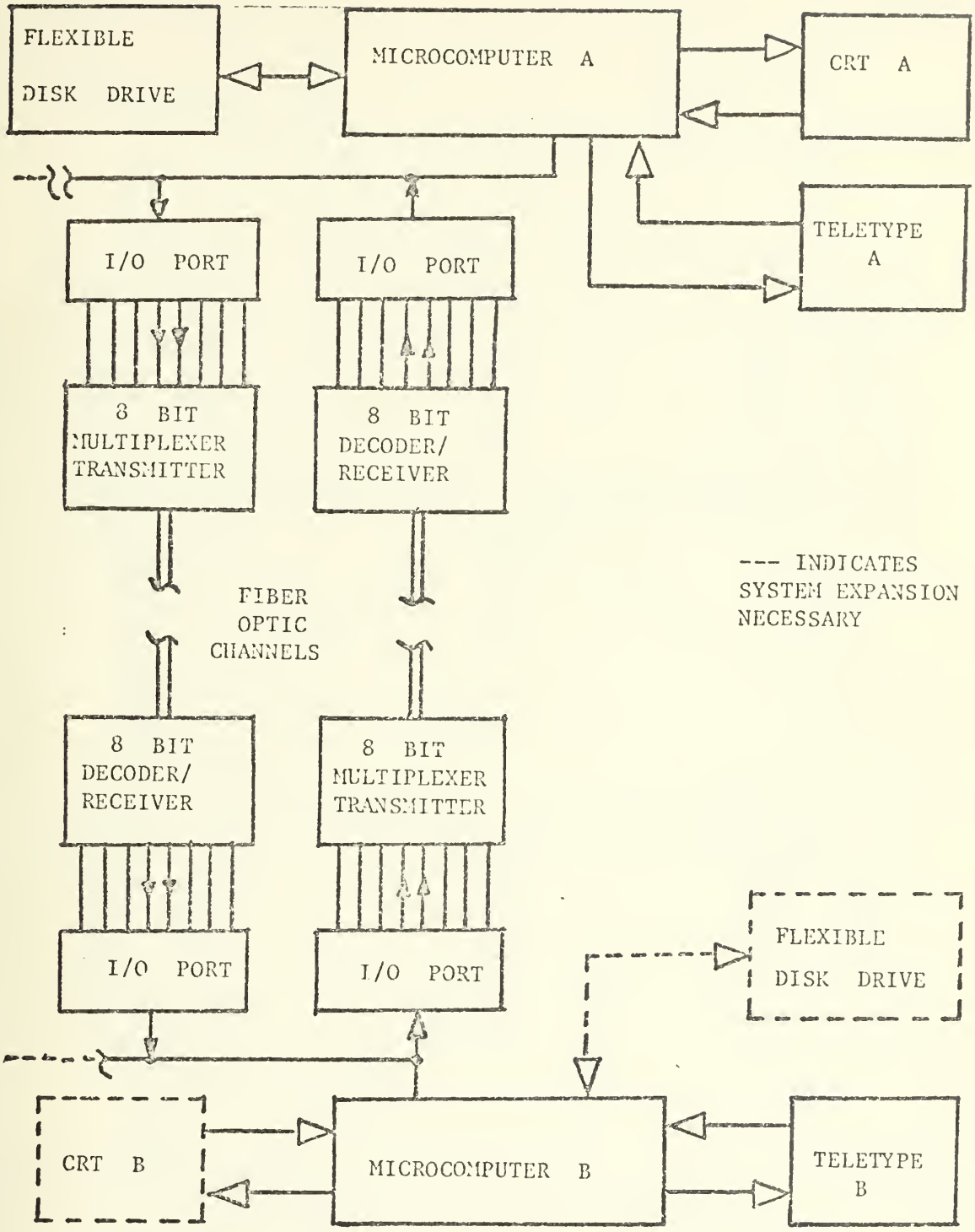


FIGURE 2.

COMPUTER TO COMPUTER HIGH SPEED

LINK CONCEPT

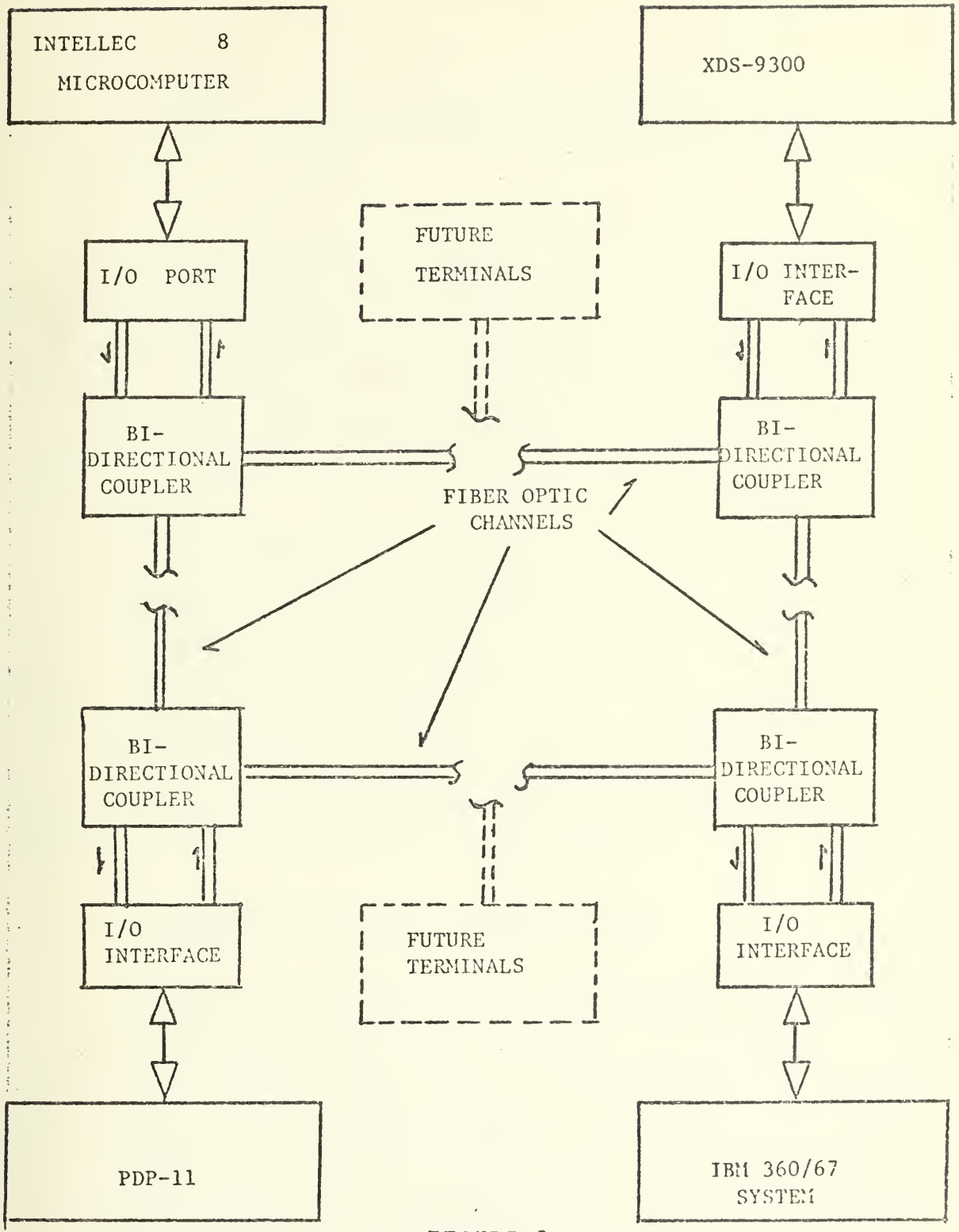


FIGURE 3.

MULTIPLE COMPUTER DATA LINK (WAVELENGTH MULTIPLEXING)

II. DEVELOPMENTAL COMPUTER FACILITIES DESCRIPTION

A. HARDWARE FACILITIES

The Computer Science Group at the Naval Postgraduate School has acquired a developmental system of three Intellec 8/MOD 8 micrccomputers, with assorted peripherals which is presently located in Spanagel Hall room 519. The Intellec 8 is a development prototype of Intel's MCS-8 system. The system functional block diagram of the development configuration is shown in Figure 4. Specifications, functional system modules, and first level theory of operation are contained in Reference (14). Two of the developmental systems were used in the link demonstration. The third system was dedicated to computer science class usage. The microcomputer operates 8-bit parallel with inverted TTL compatible output, has the capability for 8x8 bit input ports and up to 24x8 bit output ports. The development system has facilities to permanently store programs on Read-Only-Memory (ROM) chips.

1. Development System A Configuration

System A was considerably more complete than System B. The basic configuration is shown in Figure 5. The console has a mother board which holds printed circuit cards for PROM, ROM, RAM, Input/Output Output, CPU, and Front Panel Display Controller. System A has two I/O cards and one output card at present. An externally wired Input/Output facility and the first I/O card facilitate use of a high speed paper tape reader and the two peripheral displays (TTY, CRT). The second I/O card was added for interfacing the PDP-11 computer in another laboratory not

relating to this work. Both I/O cards have a switch added to control the data rate between 110 baud or 1200 baud. Both switches on the I/O cards are 110 baud in the forward position. The external I/O board was added for student projects.

The top port on the external I/O board is dedicated to the high speed paper tape reader; Ports 0 and 1 are dedicated to the teletype function; Port 3 output is available for output device connection; and Port 3 input is not connected. All pin connections are 16 pin DIP compatible. Figure 6 is a detailed mapping of the external I/O board connections.

The CRT device is a standard alpha/numeric display with full duplex operations at baud rates from 110 Bps- 2400 bps. The data rate selection is accomplished by three switches on the rear panel. The Full Duplex/Half Duplex switch is set to FDX, the 110/150 switch to 110, and the rotary switch to 1 for 110 Bps or 8 for 1200 Bps. The CRT output is a voltage level device which must be converted to an RS-232 EIA standard current loop for connection to the computer (I/O board).

Teletype operations are handled directly by the I/O card rather than using an interface unit and controller separately. The basic unit for TTY operations on the I/O board is the Universal Asynchronous Receiver/Transmitter (UART). The UART converts serial input bit streams to parallel 8-bit ASCII code output for use by the computer; similarly it converts the output from 8-bit parallel to serial. Details on the UART are contained in the Link design section. The teletype input is in a current loop form and must be converted to a voltage (serial) coding by a transistor circuit prior to receipt at the UART.

The final hardware component utilized in system A was the flexible disk drive and is self explanatory.

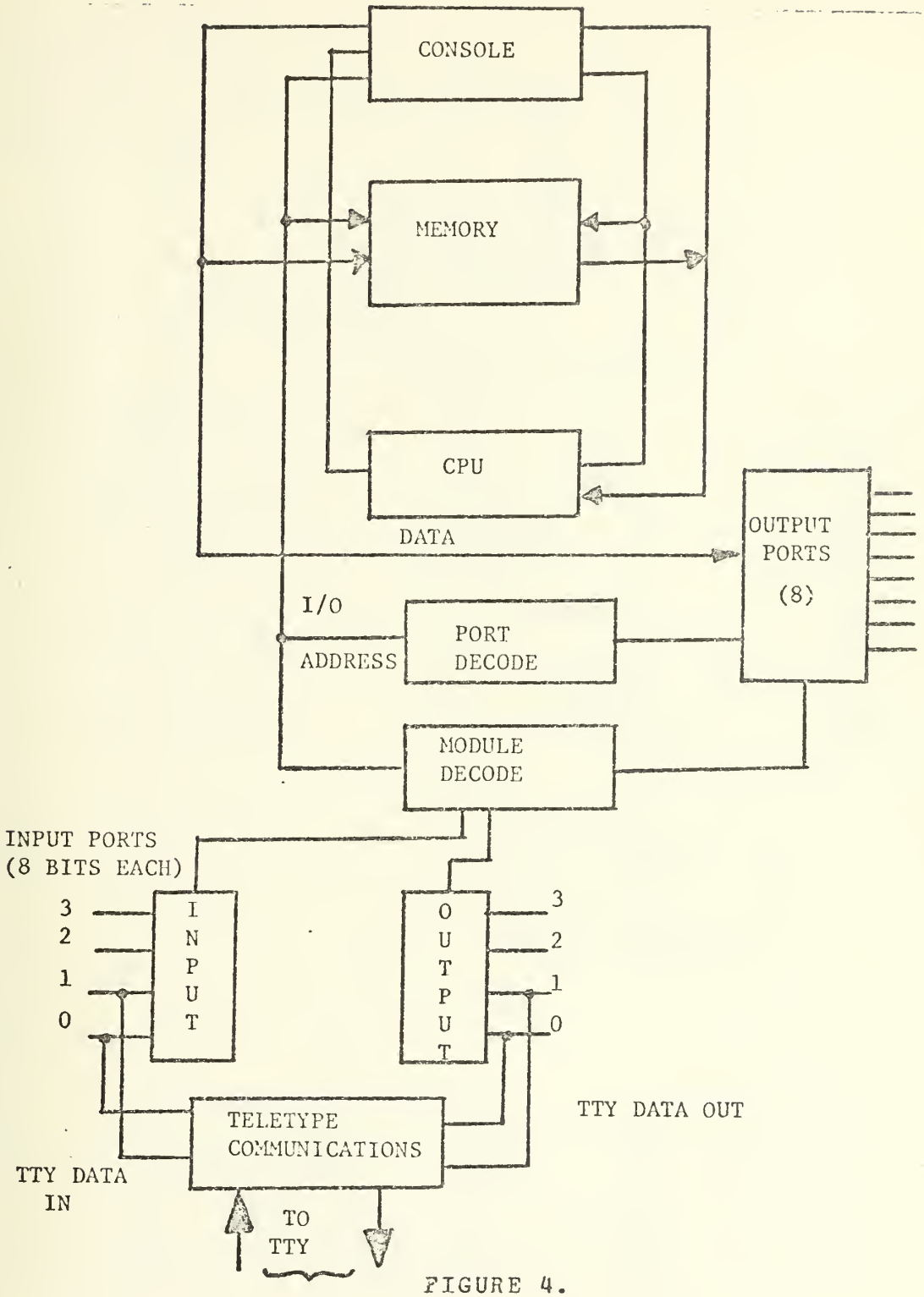
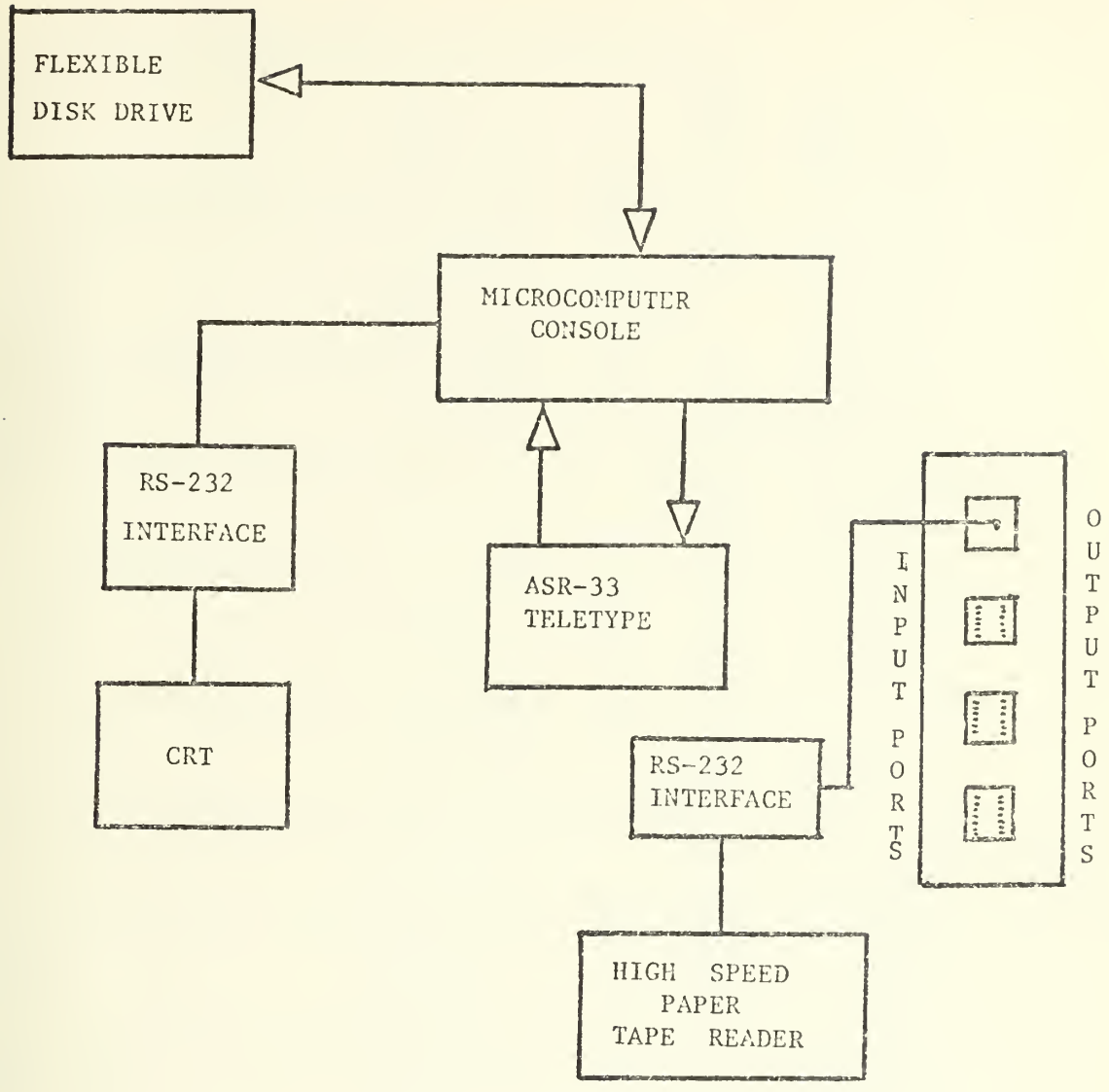


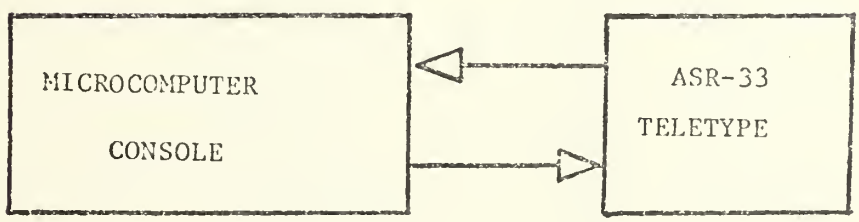
FIGURE 4.

SYSTEM FUNCTIONAL BLOCK

DIAGRAM



(a)



(b)

FIGURE 5.

(a) SYSTEM A CONFIGURATION, (b) SYSTEM B CONFIGUPATION

	INPUT PORT 0/4		INPUT PORT 1/5		INPUT PORT 2/6		INPUT PORT 3/7	
	SOURCE	DESTIN	SOURCE	DESTIN	SOURCE	DESTIN	SOURCE	DESTIN
LSB 0	J4 2	2	J4 11	6	J4 20	10	J4 29	14
1	3	3	12	7	21	11	30	15
2	4	21	13	25	22	29	31	33
3	5	22	14	26	23	30	32	34
4	6	4	15	8	24	12	33	16
5	7	5	16	9	25	13	34	17
6	8	23	17	27	26	31	35	35
MSB 7	9	24	18	28	27	32	36	36

	OUTPUT PORT 8/C		OUTPUT PORT 9/D		OUTPUT PORT A/E		OUTPUT PORT B/F	
	SOURCE	DESTIN	SOURCE	DESTIN	SOURCE	DESTIN	SOURCE	DESTIN
LSB 0	J5 2	2	J5 11	6	J5 20	10	J5 29	14
	(SAME AS ABOVE)		(SAME AS ABOVE)		(SAME AS ABOVE)		(SAME AS ABOVE)	
MSB 7	9	24	18	28	27	32	36	36

*THE PINS MARKED SOURCE REFERENCE THE I/O BOARD PIN NUMBERS IN THE INTELLEC ITSELF. THE PINS MARKED DESTIN DENOTE THE PIN NUMBERS AT THE I/O CONNECTOR AT THE REAR OF THE INTELLEC.

NOTE: +5 V IS AT THE I/O BOARD ON PINS 1, 10, 19, AND 28, BUT IS NOT BROUGHT OUT TO THE EXTERNAL CONNECTOR (ALTHOUGH IT IS BROUGHT UP TO THE CONNECTOR). BY CONVENTION, CONNECT +5 V TO EXTERNAL CONNECTOR PIN 1, WHEN +5 V IS REQUIRED EXTERNALLY (THIS REQUIRES A SINGLE WIRE AT THE EXTERNAL CONNECTOR TO PIN 1). GROUND IS ON PINS 37, 38, 39, AND 40 OF J5 AT THE I/O BOARD AND IS BROUGHT OUT TO PIN 37 OF THE EXTERNAL CONNECTOR.

FIGURE 6.

INTELLEC 8/80 I/O BOARD TO EXTERNAL PIN MAPPING*

2. Development System B Configuration

System B is a 'bare bones' configuration as shown in Figure 5(b). The major component of interest in this system was the I/O board no. 1. The board is identical to that discussed in system A. The I/O board in system B allowed access to the computer through the teletype facilities directly. The computer could also be accessed via the front panel by entering assembly language commands in Hexidecimal format. Procedures for doing this approach are described in Ref.(15).

B. SYSTEM SOFTWARE FACILITIES

The Intellec 8 system includes a monitor (SBOS) and a file handling system. The assembler software is not included. Programs may be written in PL/M, (Ref. 16), a high level language or in assembly language. Programs must be loaded by paper tape or manually through the front console (in Hexidecimal format). System B does not have a flexible disk or resident file handler but has facilities for PROM.

In loading a PL/M program, it must first be compiled under a two-pass system resident on the school's IBM 360/67 computer facility; output is a punched deck in EBCDIC format which must be converted to ASCII format on the XDS-9300 complex. The EBCDIC punched deck and 9300 control program are loaded in the card reader and sense switch 6 on the computer console set. A canned routine will prompt the user through the necessary steps to get a paper tape output (Hexidecimal format).

The paper tape program is loaded onto the Intellec 8 system through the resident disk control program (CP/M)

(Ref. 17). It may now be manipulated (edited) using macro-instructions (Ref. 18). PL/M programming is relatively straight forward and similiar to Fortran in flexibility. It uses a free form format and is especially designed for the 8-bit Intel MCS-8 microcomputer family.

System B does not have a disk unit and must be programmed in assembly language (Intel 8008/8080 version) Instructions are loaded from address and data register controls on the front panel (in hexidecimal format). The system does not enjoy the EDITOR feature although editing can be accomplished through console entered commands such as display memory, fill memory, etc. A complete Intellec 8 system instruction repetoire is contained in (Ref. 14).

III. COMPUTER TO PERIPHERAL DATA LINK

A. DESIGN CONSIDERATIONS

1. Constraints

Several constraints limited the design flexibiltity for the computer to computer link. Chief among these was the unavailability of input/output access ports (8 bit parallel) on system B. This factor meant the necessary fabrication of an external input/output panel wired as shown in figure 6. In addition, to communicate 8 bit parallel meant multiplexing and demultiplexing over the fiber-optic cable. Early in the design process it was determined to achieve an operational link as simply and quickly as possible. The facilities of the Universal Asynchronous Receiver Transmitter (UART) were taken to advantage in the multiplexing/demultiplexing function. However, this advantage limited the data rate achievable to 1200 Baud. Further, since system B had only a TTY interface, the data rate was limited to 110 Baud.

A second constraint determined at the outset of the project was to keep design simple and achieve an operational system in steps. Rather than completely redesign a receiver unit for the link a survey of four systems involving similiar concepts were examined for usage. Unfortunately none were optimum and the receiver turned out as a hybrid. A corrollary to this constraint was use of commercially available components.

The third constraint involved not engineering considerations but time. The development facility was not

dedicated to this project solely but shared with two other thesis project efforts, and in addition, to class projects in the computer science curriculum. This constraint was the most troublesome since it involved setting up/securing link components on a frequent basis.

2. Design Approach

A preliminary study of the reference manual for the microcomputer, and in particular the I/O board, showed that communication with the UART (controller) required receiver output at computer compatible TTL logic levels. To transmit intelligence over the fiber optic cable a modulator was necessary which was compatible with the TTY interface to the microcomputer. Figure 7 illustrates over-all factors which were considered and investigated in designing this link.

Measurements of logic levels were taken at various circuit points on the I/O board and checks made to ensure the TTY had a 20 mA current loop as specified in the ASR-33 teletype reference manual (Ref. 19). Results of the measurements were consistent with those determined beforehand. The system was tested in the laboratory with precision test equipment prior to interfacing to the microcomputer system.

The configuration used for testing the receiver circuit consisted of a function generator (using a square wave) driving an LED in a 20 mA current loop at a frequency of 110 HZ. The receiver was tested both with and without the fiber optic channel to illustrate differences in signal levels and wave forms. Figure 8 defines the design/test configuration.

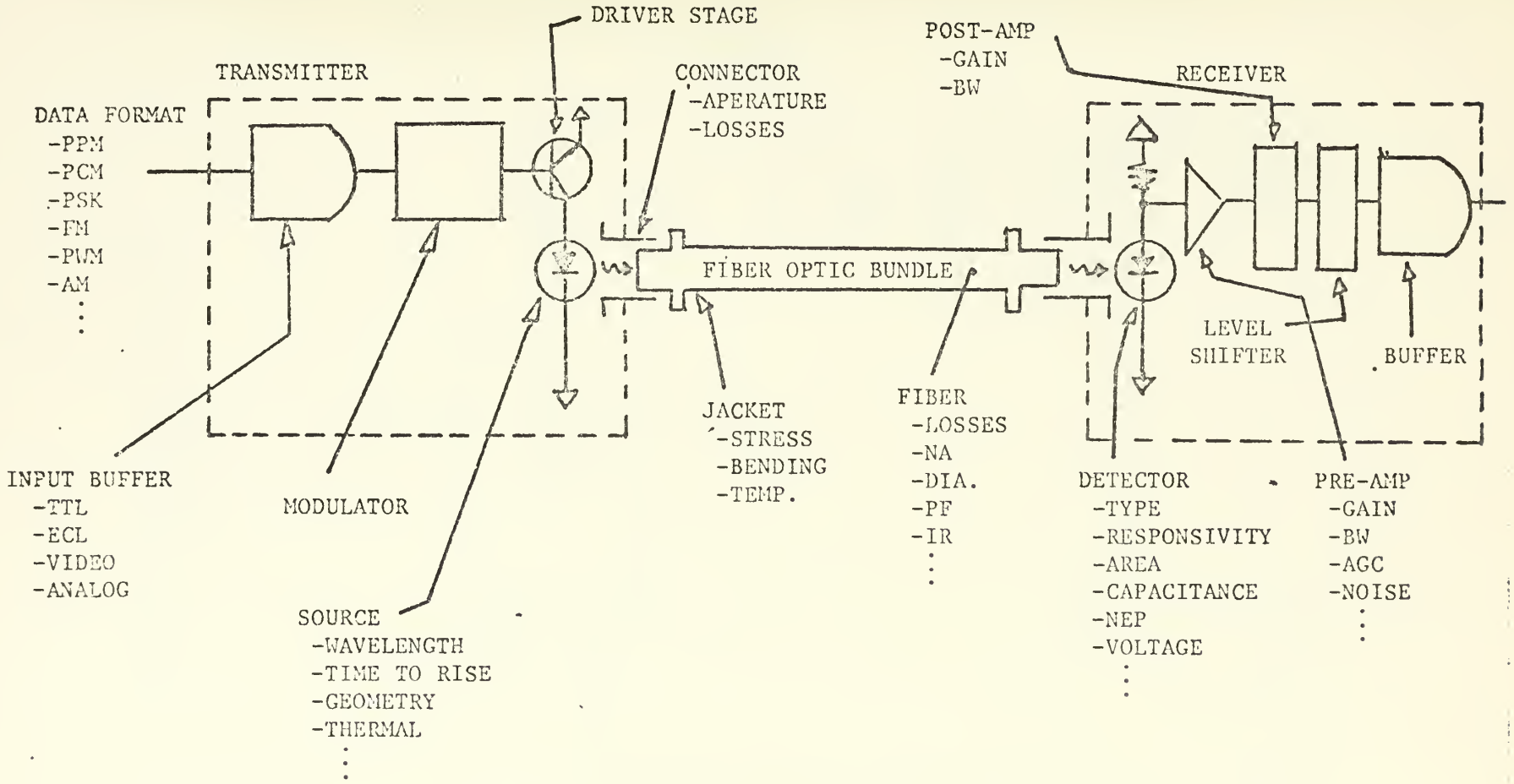


FIGURE 7.
OVERVIEW OF A FIBER OPTIC DATA SYSTEM

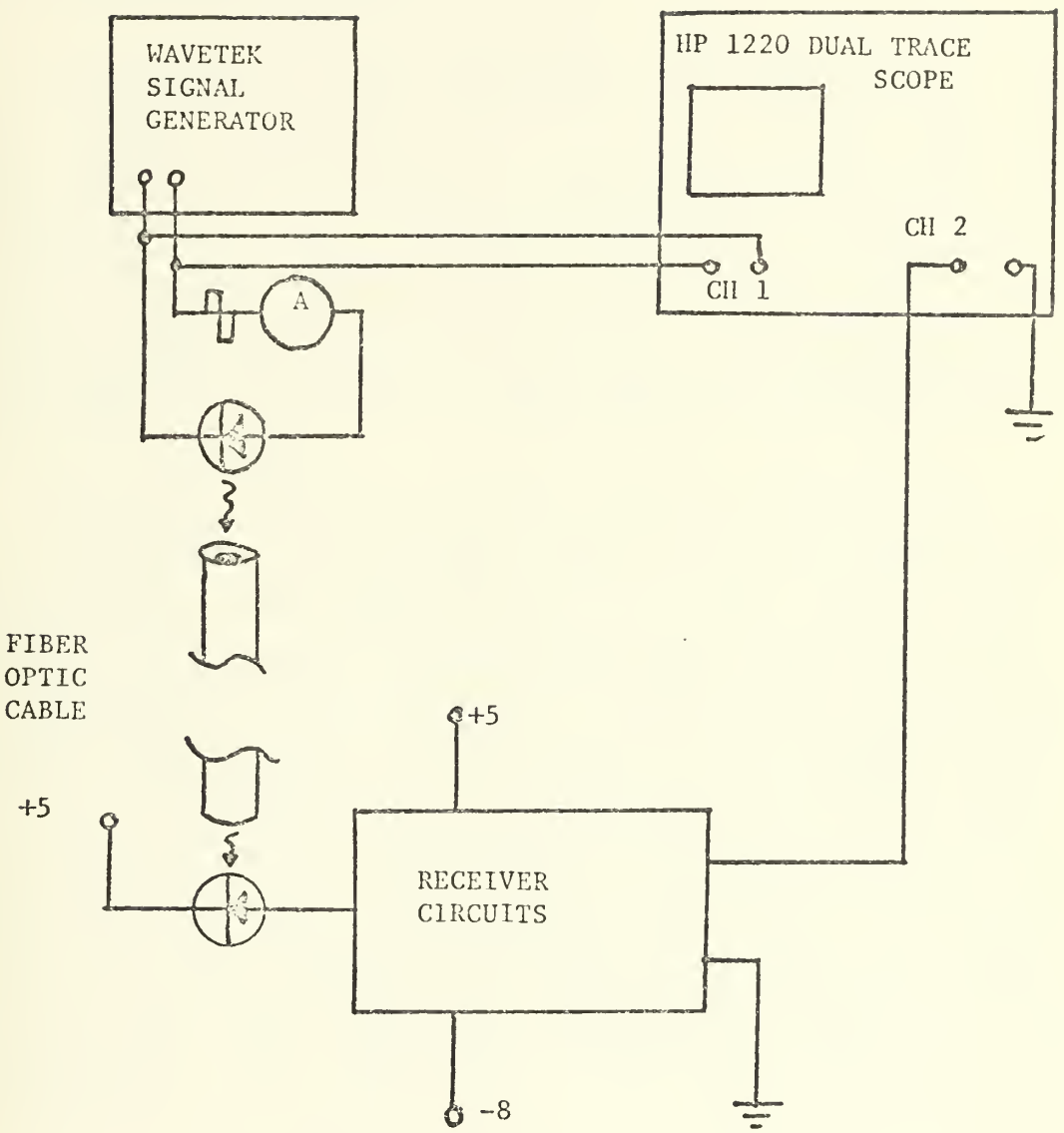


FIGURE 8.

DESIGN AND TEST CONFIGURATION

B. DETAILED LINK DESIGN

1. Transmitter Design

The design for the transmitter was simplistic. The ASR-33 teletype operates on a 20 mA current loop for keyboard receive and transmit. A commercially available LED was selected for use as the transmitter. A Spectronics SE-5450-2 Gallium Arsenide LED operating in the near infra-red was chosen. The peak emission wavelength was 935 nanometers. Table I details the major optical/electrical characteristics. No further driver circuit was required.

The LED connection into the ASR-33 current loop is shown in figure 9. An extension plug was made to facilitate experimentation. The extension was a CINCH JONES female receptacle with 8 leads running to a male CINCH JONES plug. The 8 intermediate wires were cut, stripped, and reconnected by using double female ended standard logic designer board connectors. The LED was inserted in series at wire number three. This connection placed the LED in the TTY send loop. When utilizing a special PL/M program (written by another student) the LED was connected in series with lead number six. This placed the LED in the TTY receive loop. In both configurations the LED was modulated through the microcomputer.

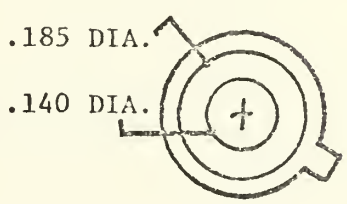
As previously mentioned, the PL/M program allowed a CRT to drive the teletype and subsequently the LED. The significance of the program was due to configuration peculiarities in system A. In order to use the ASR-33 teletype as the I/O device on system A, several plugable DIP pin connectors needed to be

TABLE I.

SE-5450-2 LED OPTICAL/ELECTRICAL CHARACTERISTICS

PARAMETER	TYPICAL VALUE	TEST CONDITION
OPTICAL POWER	1.5mW	I_f = 100 mA
BEAM ANGLE	12 DEGREES	SEE NOTE 1
FORWARD DROP	1.7 V	I_f = 100 mA
REVERSE BREAKDOWN	6 V	I_r = 10 uA
RADIATION RISE TIME	0.7 uSec	
PEAK WAVELENGTH	935 nm	I_f = 100 mA
FORWARD CONTINUOUS CURRENT		
25 DEG AMBIENT	100 mA	
25 DEG CASE	750 mA	
MAXIMUM TEMPERATURE	-65 to +100 DEG. C	

NOTE 1. THE ANGLE BETWEEN 3 dB INTENSITY POINTS



TO-46 CASE

1. CATHODE
2. NC
3. ANODE

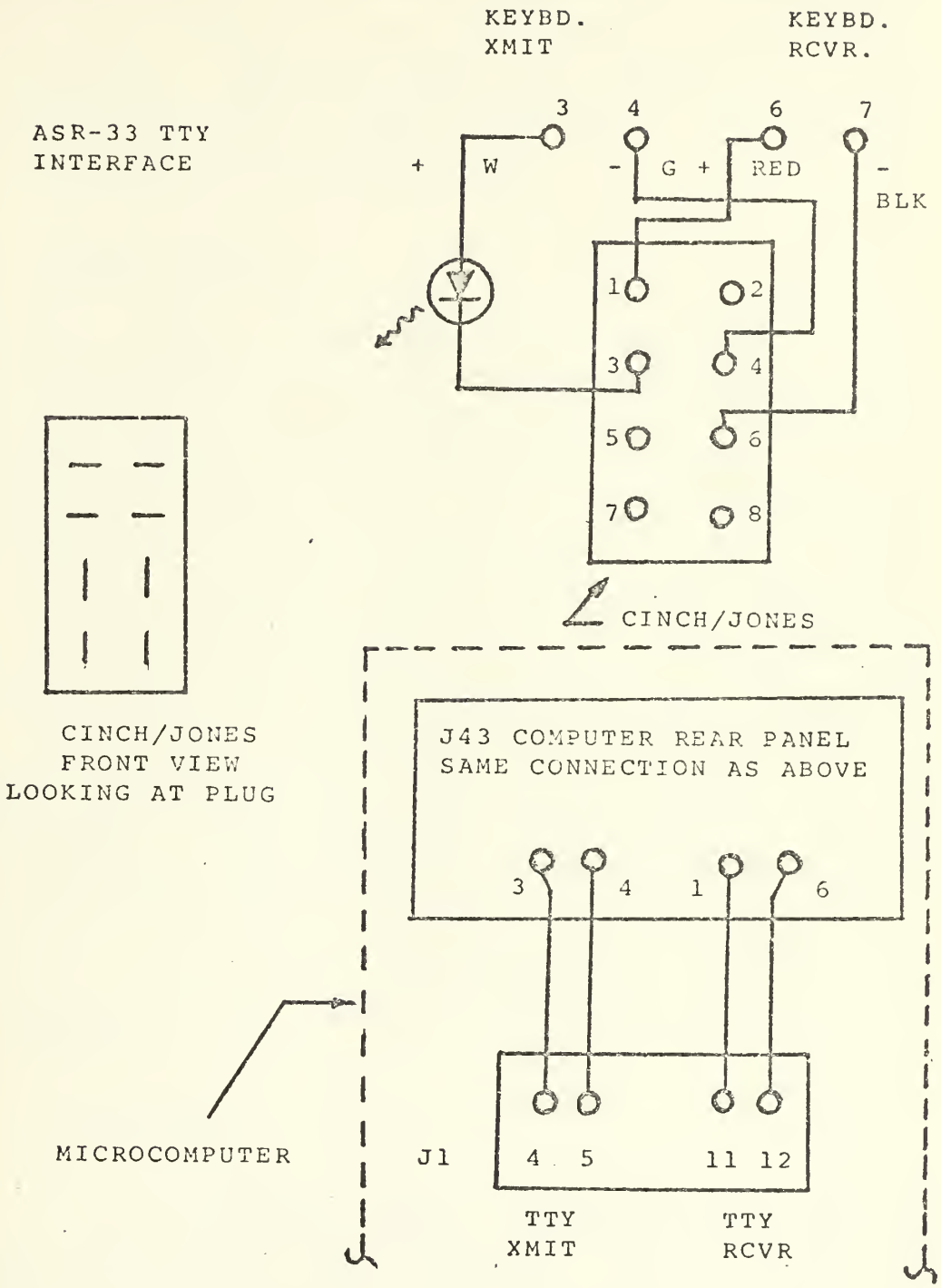


FIGURE 9.

ASR-33 TTY/LBD TRANSMITTER

INTERFACE

disconnected on the microcomputer printed circuit boards. these were disk connections, and I/O card no. 2 connections. This procedure required time and resulted in total dedication of the I/O to the teletype. This was not desirable for other users convenience.

2. Receiver Design

Four design approaches were considered for a receiver that could be constructed from reasonably common discrete or IC components and be responsive to the chosen transmitter. The four design approaches included: (1) an NELC data-bus receiver (Ref. 4) ; (2) an IBM receiver designed for the A-7 ALOFT program (Ref. 6) ; (3) a Naval Undersea Center receiver design for a deep- submergence vehicle control system (Ref. 20) ;and (4) design approaches from several previous Theses involved with fiber optic systems (Ref. 21,22). The ultimate factors in selection of a design approach for the receiver rested in the characteristics of an available photodetector, and the required voltage level to drive a signal to the teletype. Functionally, the receiver looked as shown in figure 10.

The following sections describe the details of the receiver design.

a. Detector

A p-i-n-3/D Planar Silicon Photodiode was available for use as the detector. The device was manufactured by United Detector Technology Inc., Santa Monica, Ca. Specifications from marketing brochures are shown in Figure 11 (optical/electrical characteristics) and Figure 12 (spectral response). The p-i-n-3/D had a spectral response commensurate with the GaAs LED and also was low in junction capacitance/noise characteristics.

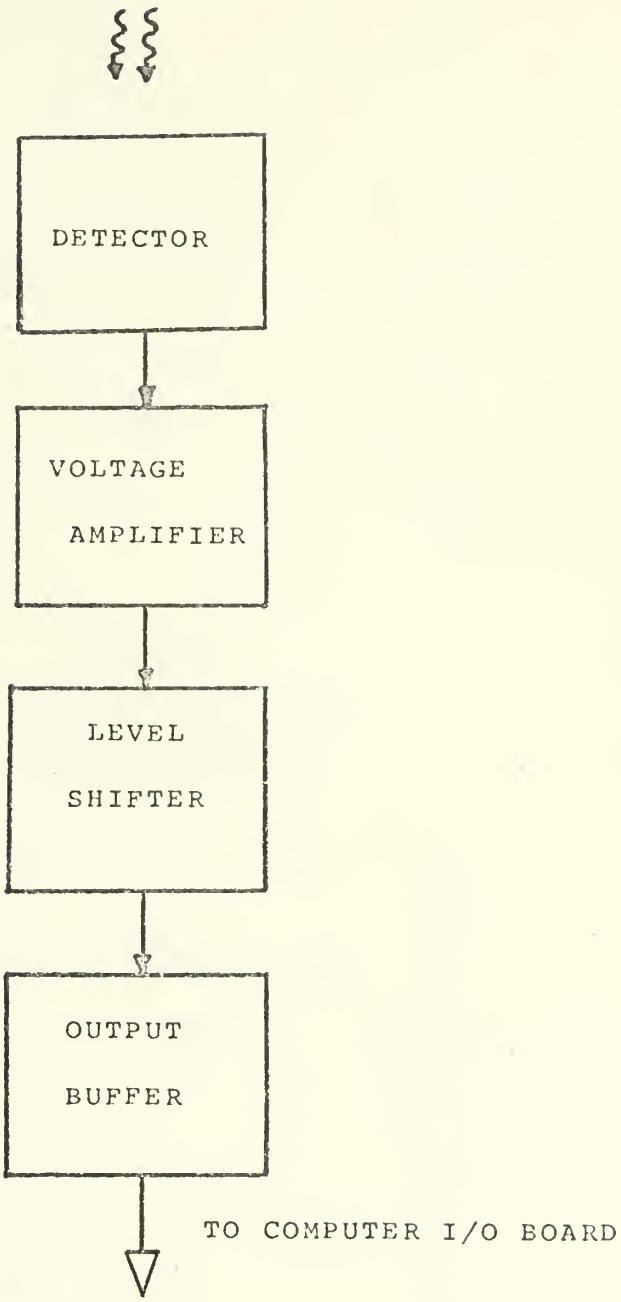


FIGURE 10.
RECEIVER FUNCTIONAL
BLOCK DIAGRAM

RESPONSIVITY (10 VOLTS,850NM)	0.4
CAPACITY (10 VOLTS)	10
(50 VOLTS)	6
DARK CURRENT (10 VOLTS)	0.02
NEP (AC, 1 KHZ, 0.85u)	2×10^{-13}
RESPONSE TIME (67%)	15
BREAKDOWN VOLTS (10uA)	50
ACTIVE AREA	0.032
ACTIVE SIZE	0.050x.100

FIGURE 11.
OPTICAL/ELECTRICAL
CHARACTERISTICS

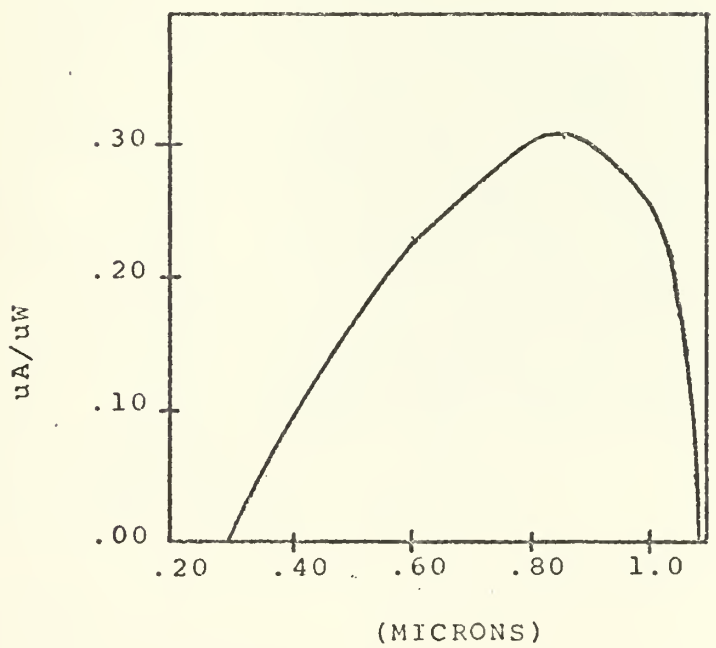
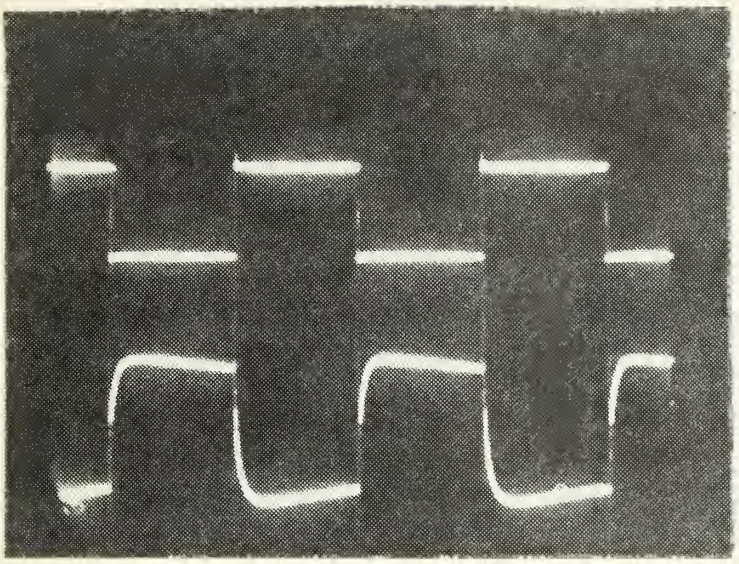


FIGURE 12.
SPECTRAL RESPONSE

b. Pre-Amplifier

The output of the photodiode was in the microvolt range and was not measured due to sensitivity of standard laboratory equipment used. The output of the receiver was chosen to be greater than +2.2 VDC and less than +5 VDC. This factor required a high gain, low noise amplifier. The amplifier chosen was a linear integrated circuit, the uA 741 frequency compensated operational amplifier. Two stages were cascaded to achieve a +2.2 VDC level.

Prior to deciding on the u/a 741 arrangement, a two-stage cascoded video amplifier circuit was built and tested. An RCA linear amplifier (RCA CA 3018A) was utilized . This amplifier had a theoretical frequency response plot good from 6 KHZ to 11 MHZ at the 3 dB points. In designing the amplification stage too much emphasis was placed on gain (i.e. because of the extremely low input voltage) and the lower 3 dB point was not correctly seen until the circuit was tested. Figure 13 is the output waveform of the first stage CA 3018A with and without the fiber optic cable. Noise is considerable in the output as well as some severe ringing. As expected, the signal did not hold below 1 KHZ. Figure 14 is the output of the two stage cascaded operational amplifier and Figure 15 is the two stage amplifier/detector circuit schematic.



WITHOUT FIBER
OPTIC CABLE

SCALE:
200 mV/VERT. DIV

50 usec/HORIZ. DIV

WITH FIBER
OPTIC CABLE

SCALE:
10mV/VERT. DIV

50 usec/HORIZ. DIV

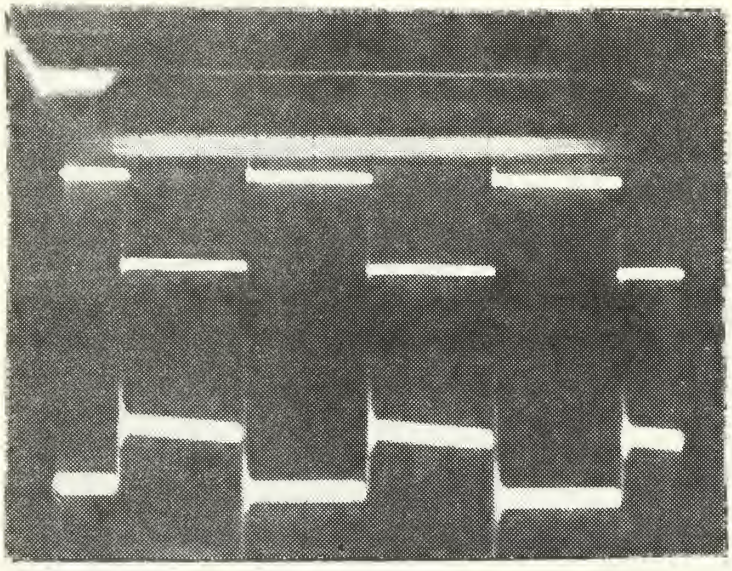
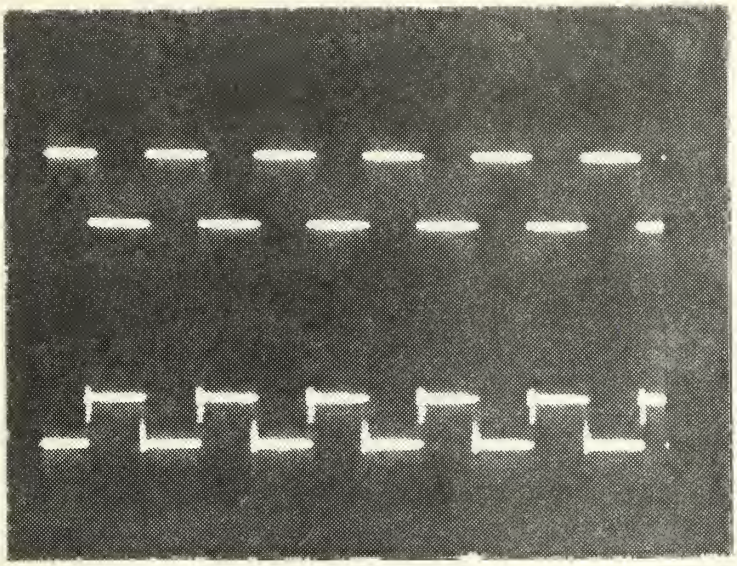


FIGURE 13

CA 3018A OUTPUT WAVEFORMS



STAGE ONE OUTPUT
(WITH CABLE)

TOP: INPUT
1V/VERT. DIV
BOTTOM:
100mV/VERT. DIV

TIME (BOTH)
5msec/HORIZ. DIV

STAGE TWO OUTPUT
(WITH CABLE)

TOP: INPUT
1V/VERT. DIV
BOTTOM:
1V/VERT. DIV

TIME (BOTH)
5msec/HORIZ. DIV

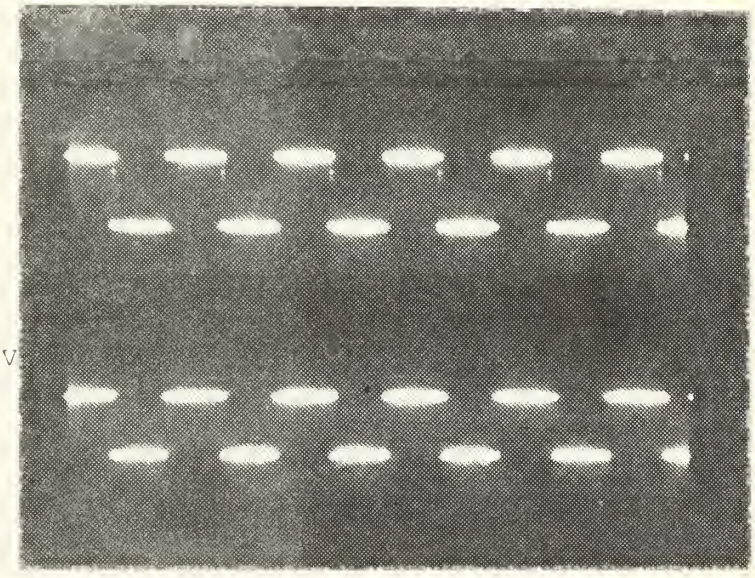
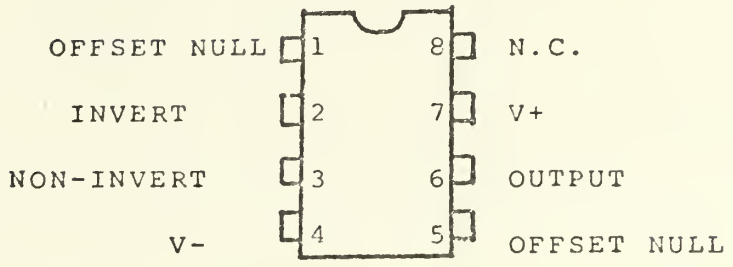


FIGURE 14

TWO STAGE VIDEO AMPLIFIER uA 741 OUTPUT WAVEFORMS

MINIDIP CONNECTION
(TOP)



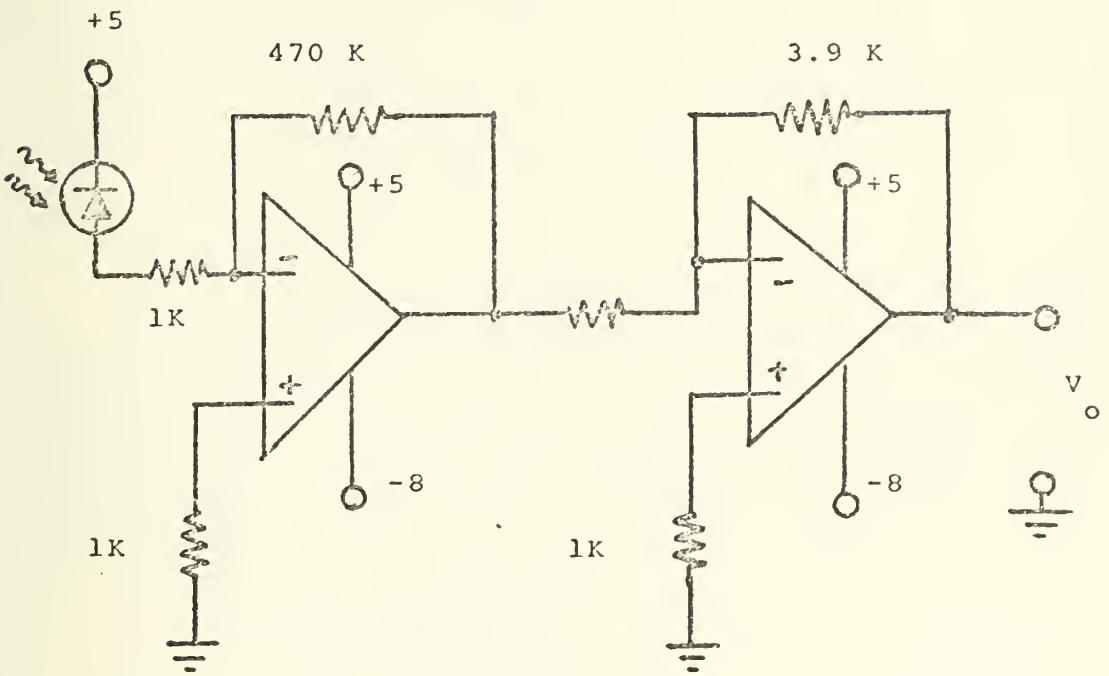


FIGURE 15

TWO STAGE AMPLIFIER/DETECTOR CIRCUIT

The input to the first stage was unobservable with the equipment ranges available. A detector output equal to the lowest value on the minimum scale of the oscilloscope was assumed (0.2 mV/div). The amplifier output was assumed 0.7 VDC or equivalent to that required to turn on a silicon transistor. The overall gain of the amplifier required was 3500. The first stage was designed with a gain of 470 and the second with a gain in the vicinity of 30. This gave an overall theoretical gain of 14,000. The output voltage level of the second stage was 0.5 VDC. The actual gain was considerably reduced in the first stage to approximately 1000 and in the second stage to 3. The reasons for the discrepancy between theoretic and actual gain was not investigated.

During the amplifier design, a 0.47 uF capacitor was utilized between stages as dc blocking. This component latter was replaced by a straight wire since it effectively differentiated the input waveform and didn't allow a sufficient pulse duration to actuate a mechanical relay on the teletype.

c. Level Shifter

The output of the second op-amp was sufficient (under signal conditions) to turn on a switching transistor combination. Figure 16 is the level shifting circuit.

Output of the level shift circuit was determined by measuring the output of the UART in system B under no-load/load conditions with an oscilloscope on dc level setting. Commands to the computer in the form of display memory locations were executed and the resulting scope

pattern examined. The level for a logic '1' (or high) from the UART was +2.2 VDC and +5 VDC under load/no-load respectively. The logic level '0' (or low) was 0.8 VDC under both conditions. The output of the level shifting circuit was set for a level greater than +2.2 but not to be more than +5 VDC.

The second transistor acted merely as an inverter since the signal at Q1 was 180 degrees out of phase with the input. As an additional buffer precaution, a 7405 Hex inverter stage was added with two stages, one inverted, one in phase. This proved unnecessary in the link demonstration. The completed receiver schematic is shown in figure 17.

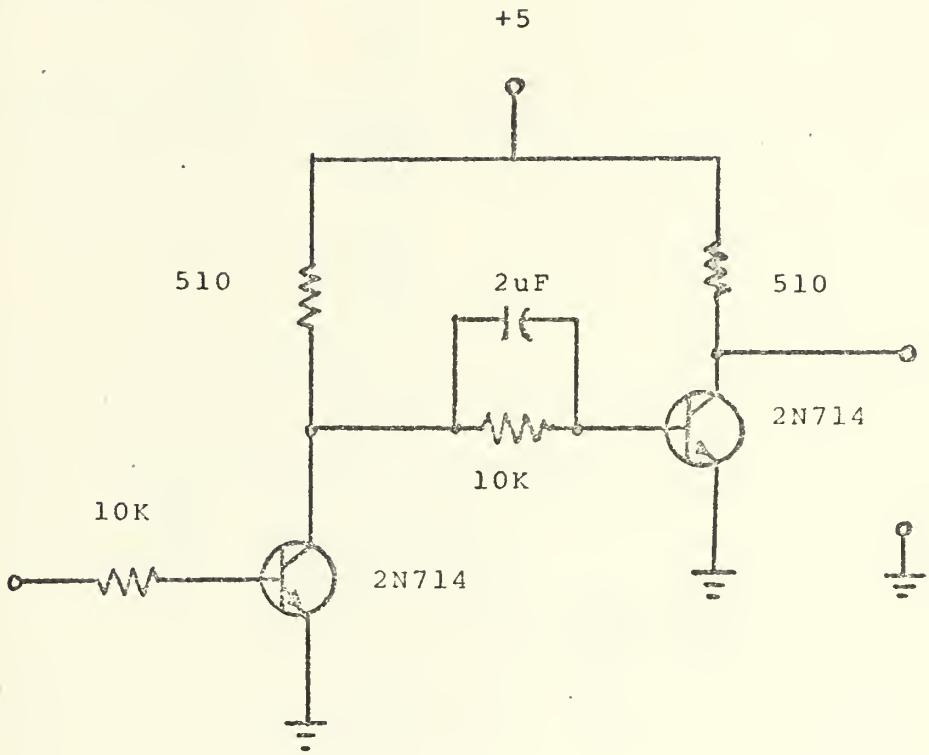


FIGURE 16
LEVEL SHIFT CIRCUIT

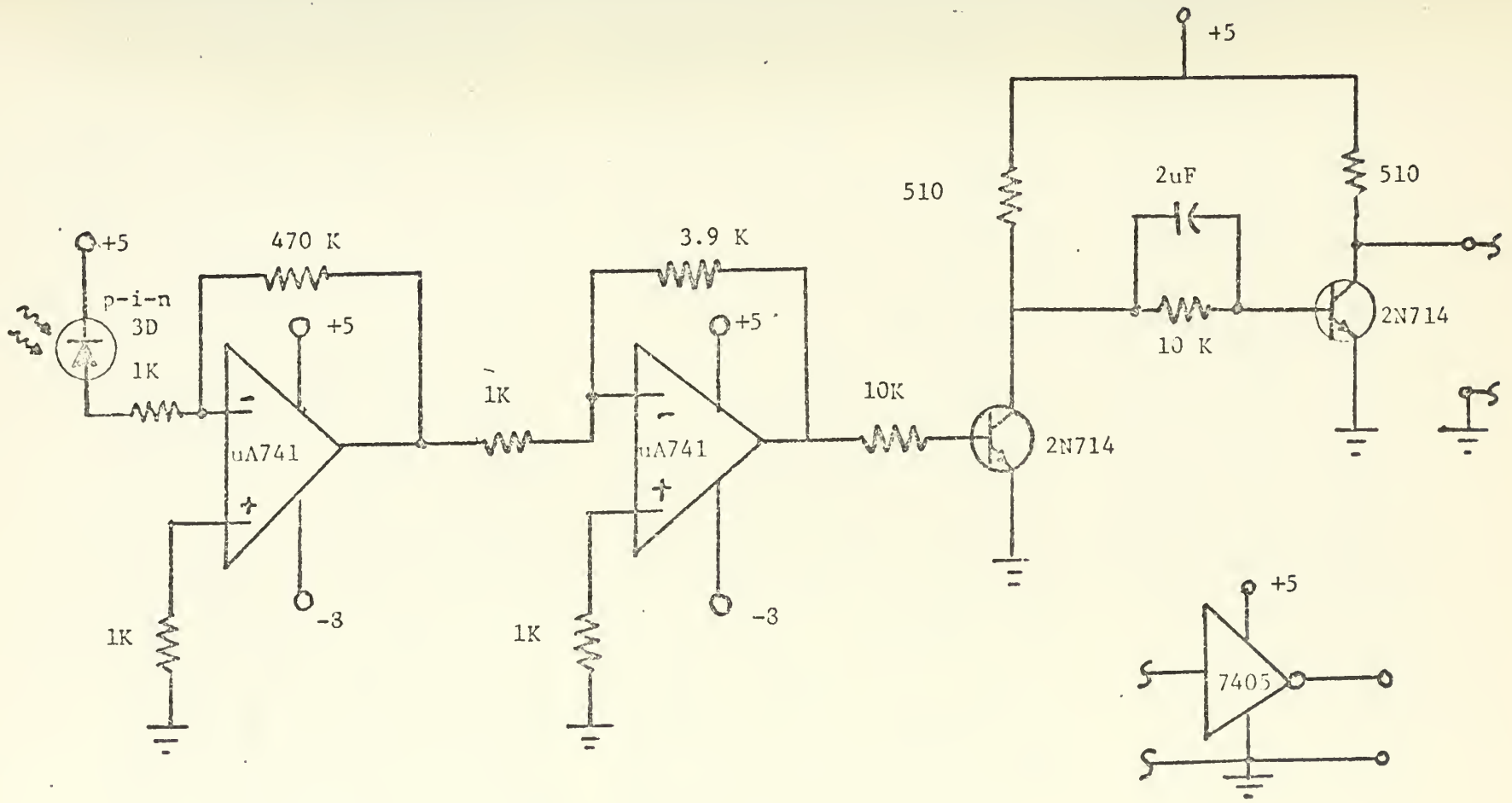


FIGURE 17.
RECEIVER SCHEMATIC

3. System B Computer To Receiver Interface

The key element in achieving a workable data link was the interface between the receiver and the controlling circuits . The I/O board in the microcomputer contains two functions needed in the interface: (1) the UART, and (2) the voltage-current conversion circuit.

The UART is an MSI circuit that allows a parallel-serial conversion and back again at logic levels compatible with TTL integrated circuits. The asynchronous nature of the UART does not require locking into system timing; only the beginning and end of words must be distinguishable. The interface must, of course, have equal timing at each end. Figure 18 is an illustration of the serial data format for 100 WPM, ASR-33 8 level teletype code. The 0.47 uF capacitor previously mentioned in the amplifier coupling was sufficient to perturb this timing so that the interface did not work properly at first.

Essentially the UART parallel loads a shift register and clocks out the data serially (or vice-versa). The parallel output is then latched onto the I/O ports. In addition to data conversion, the UART does considerable housekeeping such that a complex MSI chip is required. The UART utilized in system B was an AY-5-1012 (General Instruments). Five other pin compatible UART's are: (1) S1883 American Microsystems, (2) 2536 Signetics, (3) COM 2502 Standard Microsystems, (4) TMS 6012 Texas Instruments, and (5) TR 1602 Western Digital. The UART comes in a 40 pin DIP package. Pin functions are shown in figure 19 and are self explanatory.

THE START BIT IS ALWAYS A ZERO

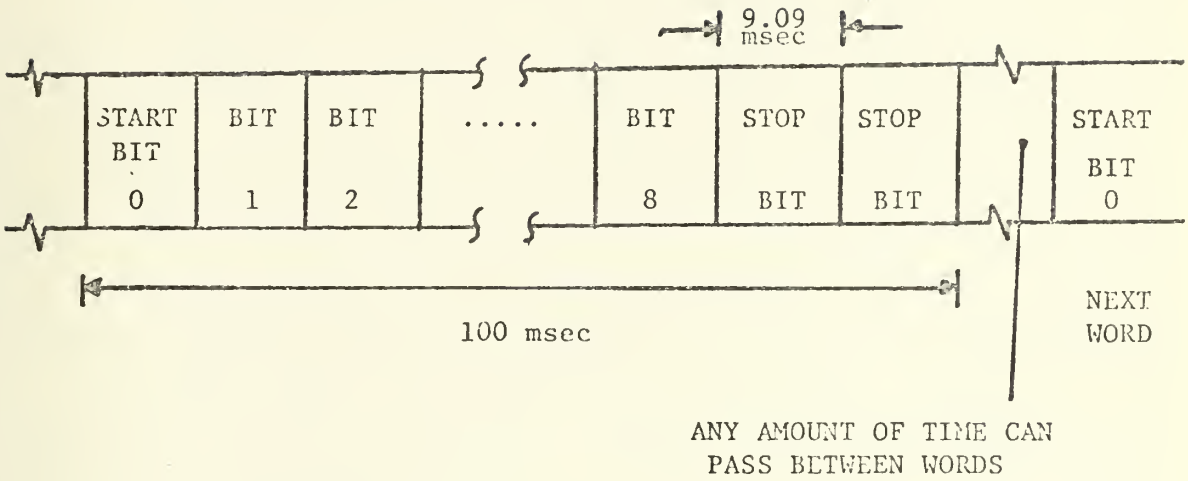


FIGURE 18

SERIAL DATA FORMAT FOR

ASR-33 TELETYPE

PIN	1	+5V	PIN	21	RESET
	2	-12V		22	NC
	3	GROUND		23	STROBE
	4	ENABLE		24	NC
	5	NC		25	SERIAL DATA OUT
	6	MSB		26	LSB
	:	ASCII PARALLEL		:	ASCII
	:	OUTPUT		:	INPUT
	12	LSB		32	MSB
	13	PARITY		33	NC
	14	FRAMING		34	+5V
	15	OVERRUN		35	GROUND
	16	X ENABLE		36	+5V
	17	CLOCK		37	+5V
	18	STROBE RESET		38	GROUND
	19	STROBE		39	GROUND
	20	SERIAL INPUT DATA		40	CLOCK

FIGURE 19

UART PIN CONNECTIONS

The second part of the I/O board of interest is the output voltage-current code conversion circuit. This circuit takes the serial UART output voltage level and converts it to a 20 mA on-off current loop in a two transistor circuit. The circuit is shown in figure 20. When there is no data on the line pin 25 of the UART is high logic at +5 VDC. The base of Q4 is +0.7 VDC and Q4 is on. The transistor on state provides a current path for +5 VDC through R15/R16 to ground putting the base of Q4 essentially at +4 volts and a saturation condition. The -9 VDC reference is felt through R12/R18 and the teletype load impedance generating a 20 mA current in the loop. This condition signifies a stop or mark condition. The reverse condition occurs for a space or zero signal condition. Q3 is off and Q4 is reverse biased. The collector of Q4 is at -9 VDC and no current flows in the teletype loop.

The receiver output was connected to the UART side of R9 in figure 20. This allowed computer A to interface teletype B.

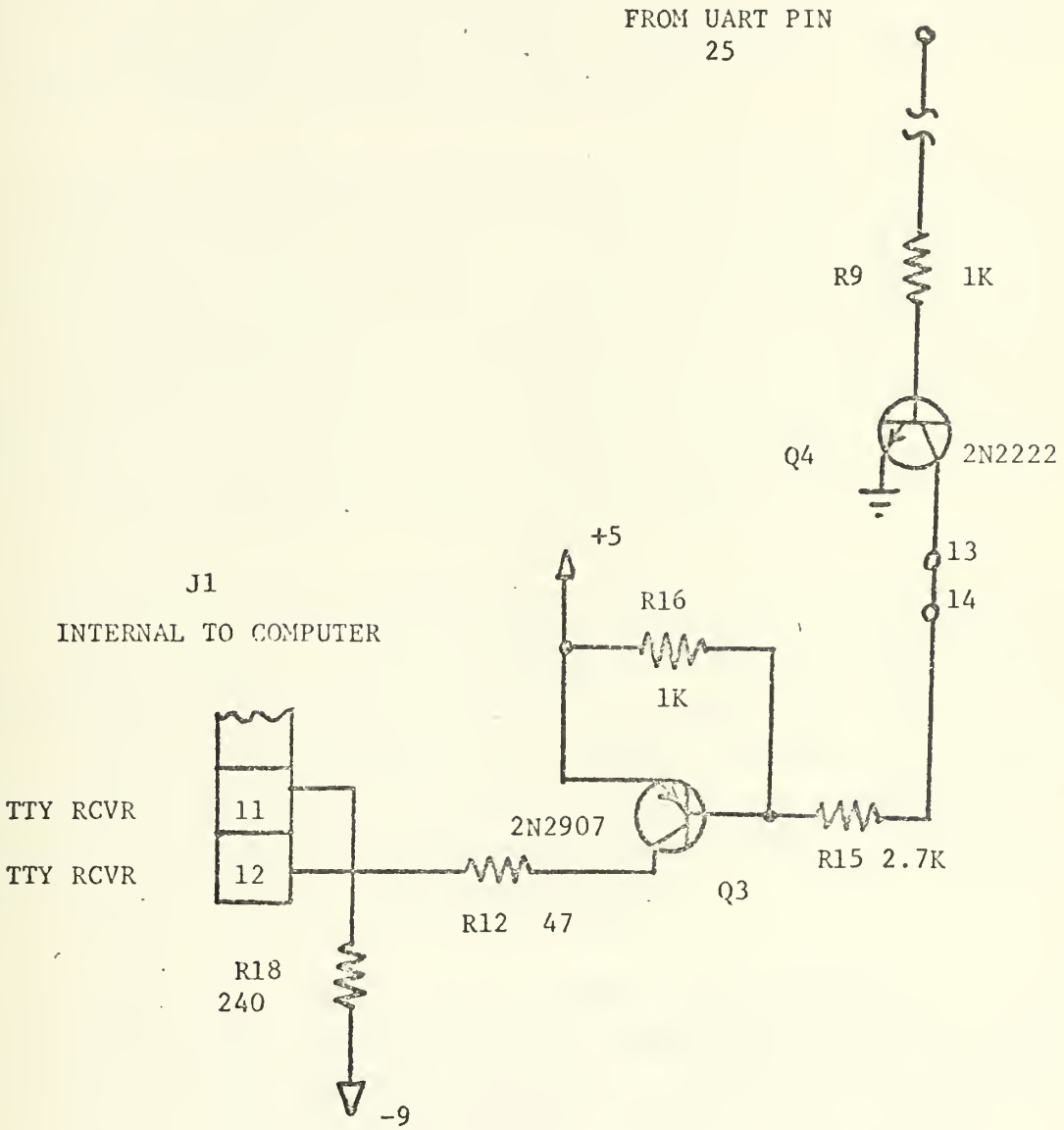


FIGURE 20
VOLTAGE-CURRENT CONVERTING
CIRCUIT

C. LINK DEMONSTRATION PROCEDURES

The following instructions detail the component interfaces and steps which must be followed to effect a working demonstration link between computer A and remote teletype B through the fiber optic cable.

The LED transmitter was inserted into the CINCH/JONES extension at lead number 3. The teletype on system A was plugged into the female side of the CINCH/JONES and the male side of the CINCH/JONES was inserted into an interface cable to the computer through I/O board number 2. The CRT was connected to the computer through a EIA-RS-232 standard interface via the back panel of the computer on J43. This jack connects directly to I/O board number 1.

The receiver was connected to the remote peripheral via I/O board number 1. The receiver output was connected to the UART side of R9 and pin 25 on the UART was lifted from its circuit. The receiver was supplied through two voltage supplies (+5,-8 VDC) and circuit ground was connected to computer B chassis. This ground must be properly made or the teletype will not function properly.

The 25 Ft. fiber optic bundle was coupled to the LED and the photodiode using a plastic sheathing slightly larger in diameter than either component. The coupling proved to be of little problem since the LED had a 12 degree cone which focused it's output.

System A was brought up by the following procedure: (1) flexible disk SBOS #1 was inserted into the drive and power applied; (2) the CRT was turned on and set at the proper baud rate. This was accomplished by setting the 110/150 switch to 110 and the rotary switch to 1 on the rear panel. In addition the FDX/HDX switch must be at FDX.

On system A two baud rate switches on I/O boards 1 and 2 must be set in the forward position for 110 baud; (3) microcomputer A was turned on and teletype A set to LINE; (4) the reset switch on the front panel of computer A was pressed to actuate the system bootstrap program. Correct procedure results in the display of an ''>A'' at the top margin on the CRT; (5) the program file name was typed in on the CRT (P11 GARB.AGE) and carriage return hit. This activates program P11. The program will then prompt the user with a choice of options. The options to request are default:N, I/O ports CRT:0, TTY:1, CRT echo:Y, and TTY echo:1. Both the CRT and TTY can transmit to each other at this point. The LED will be modulated dependent on which number lead it is in on the CINCH/JONES extension.

System B was activated by merely turning on the computer on switch and setting the teletype B to LINE position. Transfer of data from system A to teletype B is now possible.

IV. HIGH SPEED LINK DESIGN CONSIDERATIONS

A. DESIGN APPROACH

There are two approaches which are fairly simple to implement in achieving a high speed data link through the use of fiber optics. The most straight forward method is to design 8 identical LED modulator circuits (simply a properly biased switching transistor with an LED in the collector circuit) connected to each pin of the external extension of the I/O ports on system A. The major disadvantage of this approach is the need for 8 identical receiver circuits and 8 fiber bundles. Single fibers could be used but a controlled enviroment must be effected so that the light may be collimated and focused onto the fiber. The second method would utilize a Time Division Multiplex (TDMX) scheme operating at the maximum microcomputer clock rate of 800 KHZ. The present receiver circuit could not handle this frequency without redesign. The maximum frequency of the present receiver circuit is 50 KHZ. Figure 21 is the hardware system required to implement this scheme.

The multiplexer portion of the circuit was breadboarded in the laboratory; operation was successful. The design of the multiplexer circuit required a clock, a 9312 IC multiplexer, and a modulo 8 ripple counter. The counter was constructed from 1 and 1/2 74107 dual JK Master/Slave Flip-Flops. The circuit schematic is shown in figure 22. Two receiver circuits for full duplex operation are required. In addition two fiber bundles are required.

The element necessary to make this link work is an interrupt routine in the computer. The Intel microcomputer

has a built in interrupt facility which was not investigated in detail in conjunction with this research. However, an effort is currently in process by a student in the Computer Science Curriculum to develop the required interrupt. Once an interrupt is generated, the processor treats the incoming code or instruction 'jammed on' the main data bus like any other fetched instruction (Ref.14). There are some restrictions which are detailed in the reference manual. The interrupt code necessary would be a 'jump to' instruction at a particular memory location. The memory location would contain a preset set of instructions to allow data acceptance on a specified data I/O port and then route that data to memory. The routine would also acknowledge data receipt to the sending computer. These programs are not presently written.

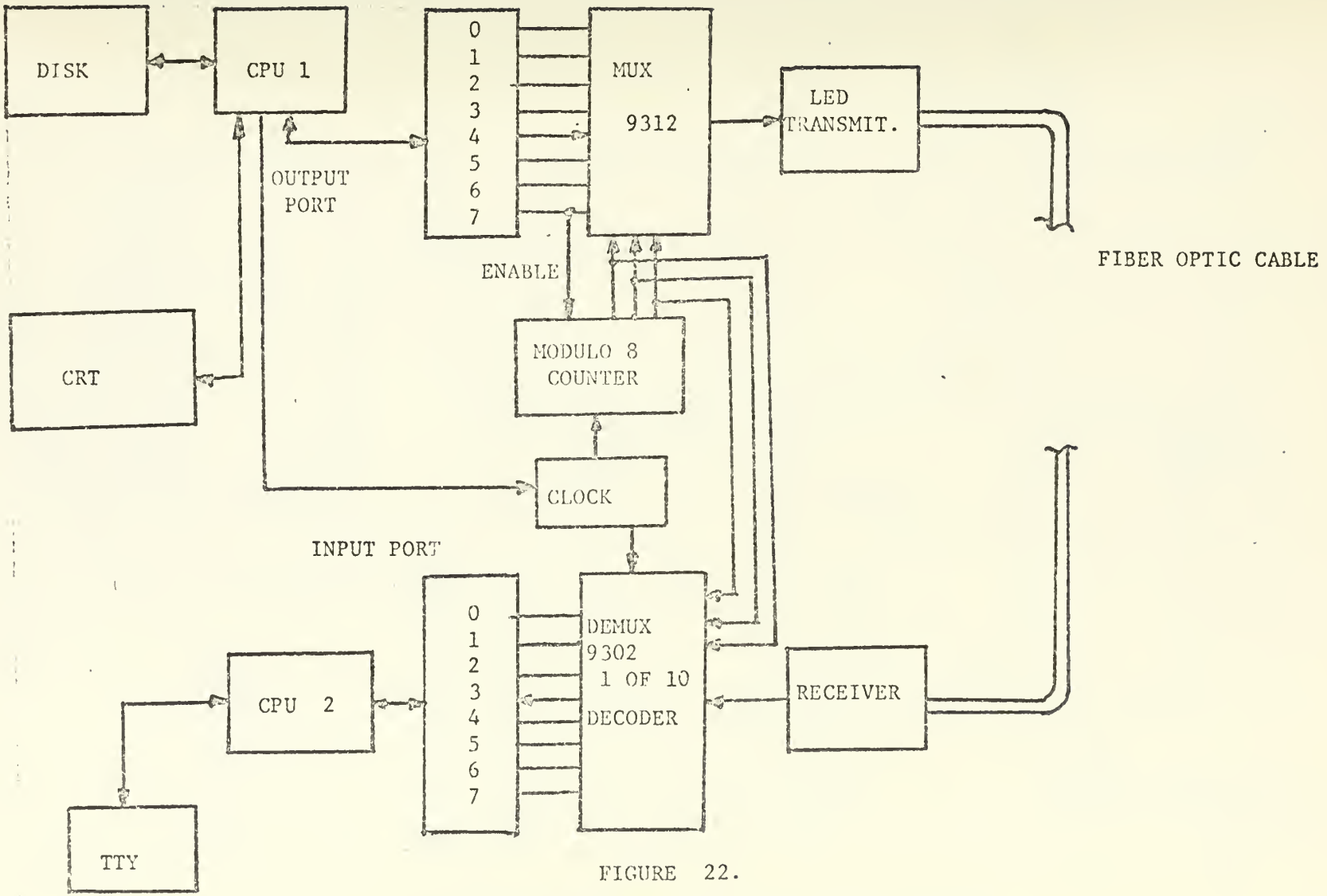


FIGURE 22.

HIGH SPEED COMPUTER TO COMPUTER LINK HARDWARE

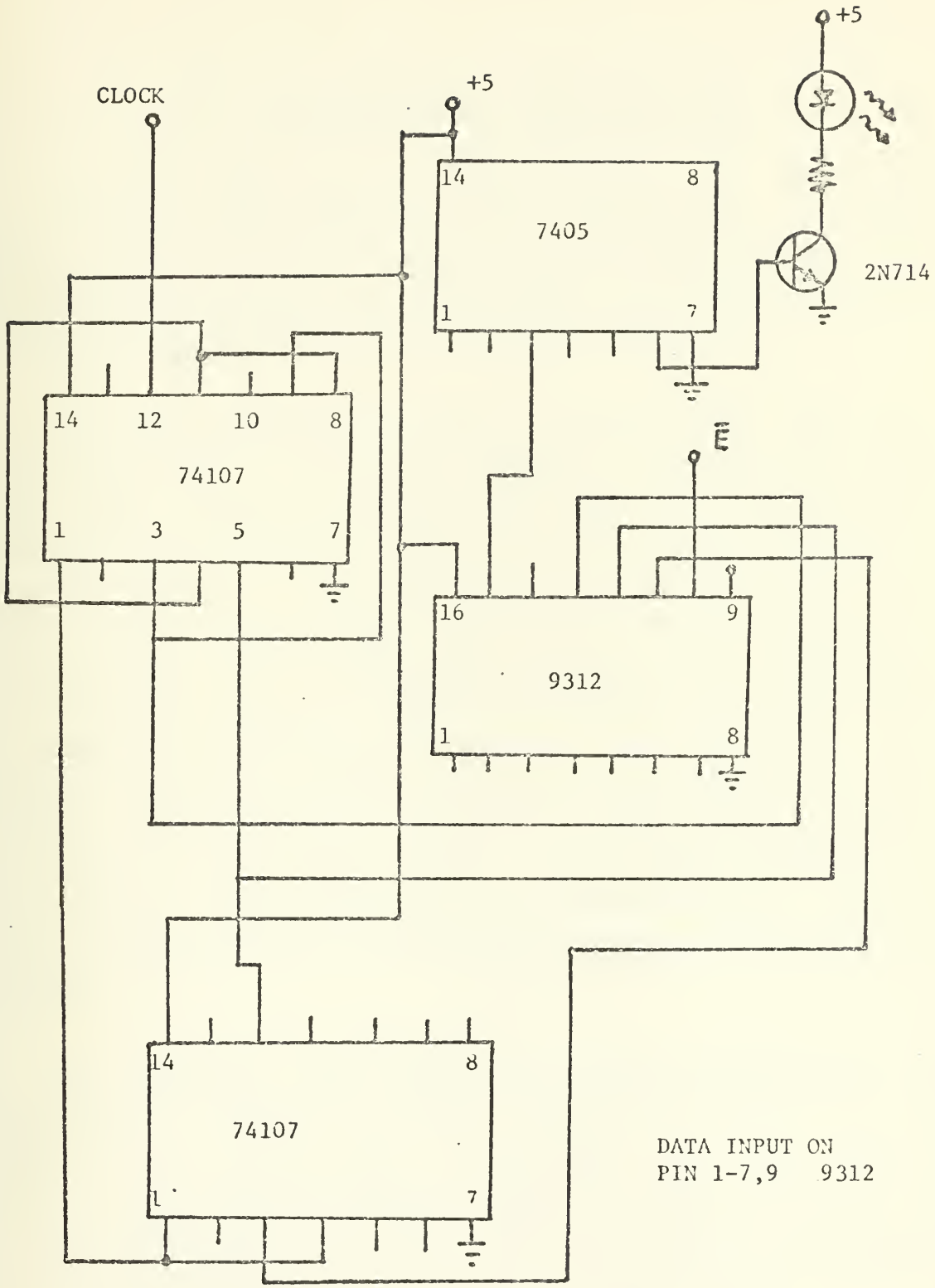


FIGURE 22.

HIGH SPEED LINK SCHEMATIC

V. CONCLUSIONS AND RECOMMENDATIONS

A basic link between a microcomputer and a peripheral I/O device has been designed and demonstrated. The high speed computer-computer link was not accomplished since the design and realization of an interrupt capability for the Intellec 8 was beyond the scope of this research.

The work accomplished herein is prelimianry and is a necessary part of any future attempt to demonstrate a high speed link. Elements of the system are off-the-shelf and commercially available. The basic theory of each portion of the fiber optic link is well known and documented. The fiber optic cable itself may be the singular exception; however, most work in this area is dedicated to improvement of materials, cheaper production methods, and new methods for coupling the fiber to the source and detector. The coupling problem is being attacked in many quarters and is devoted mainly to finding methods to couple multiple sources and detectors to single fibers. Fiber optic technology is here to stay. The applications are numerous and of extreme value to the military in the design of future communications systems.

The facilities and technology base are available at the Postgraduate School to become heavily involved in the explosion of fiber optic technology. An asset to this factor is the availability of research personnel and the relative proximity to NELC. NELC is a respected leader in this new technology and could make considerable knowledge and experience known to researchers in this field.

The Computer Science Group at the Postgraduate School

has considerable expertise in computer systems software architecture and development. A working group of the CSG and the Electrical Engineering Department should be established to investigate methods in which the school can further participate in state-of-the- art developments and applications. As a more near term recommendation, efforts should be made to complete the high speed link and then to develop the techniques for linking multiple computer systems as outlined herein.

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