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Petite Amateur Naval Satellite Spacecraft Digital Control System: A Hardware Design

by

John Douglas Ashe
Lieutenant, United States Navy
B.S., University of Tennessee, 1984

Submitted in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL

March 1993

ABSTRACT

This thesis provides the foundational hardware design for the Digital Control System of the Petite Amateur Navy Satellite (PANSAT). The design implements a multitasking operating system to provide store and forward communications. This design contains "pair and a spare" technology to provide redundancy for space operations. Addresses necessary for software design are discussed and examples of initializing commands for the more complex sections are given. CMOS technology was used throughout the design to minimize the power requirements. RS422 protocol was used on all communications lines to lessen the impact of noise. The M80C186 microprocessor coupled with an 82C55 Programmable Peripheral Interface are the cornerstone of the design. All peripheral sections, Telemetry, Memory, and Communications are designed to be controlled by the M80C186 via the 82C55. Since the mission of PANSAT may be changed slightly before the launch of the vehicle, the hardware design contained in this document is engineered to be upwardly compatible where possible.

C.1

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I. INTRODUCTION

A. GENERAL

The heart of the Petite Amateur Navy Satellite, (PANSAT) is the Digital Control System (DCS). The DCS is comprised of two control boards, the Primary Control Board (PCB) and the Secondary Control Board (SCB). These control boards contain the necessary electronic equipment to collect Spread Spectrum communications traffic from ground stations, interpret the data stream, and respond to any commands the spacecraft receives. Traffic not specifically addressed to the DCS is stored and forwarded. This control unit is able to operate autonomously while in a low earth orbit. Tasking will be moderate to heavy with the majority of operations being concerned with the collection of telemetry and power bus control.

B. REDUNDANCY

Redundancy is incorporated into this design by using two control boards. The DCS normally operates under the unilateral control of the Primary Control Board (PCB). The Secondary Control Board operates along side the PCB but has no effect on the DCS power system or the satellite communications equipment . Figure 1 shows a block diagram of the functional relationship between the two control boards.

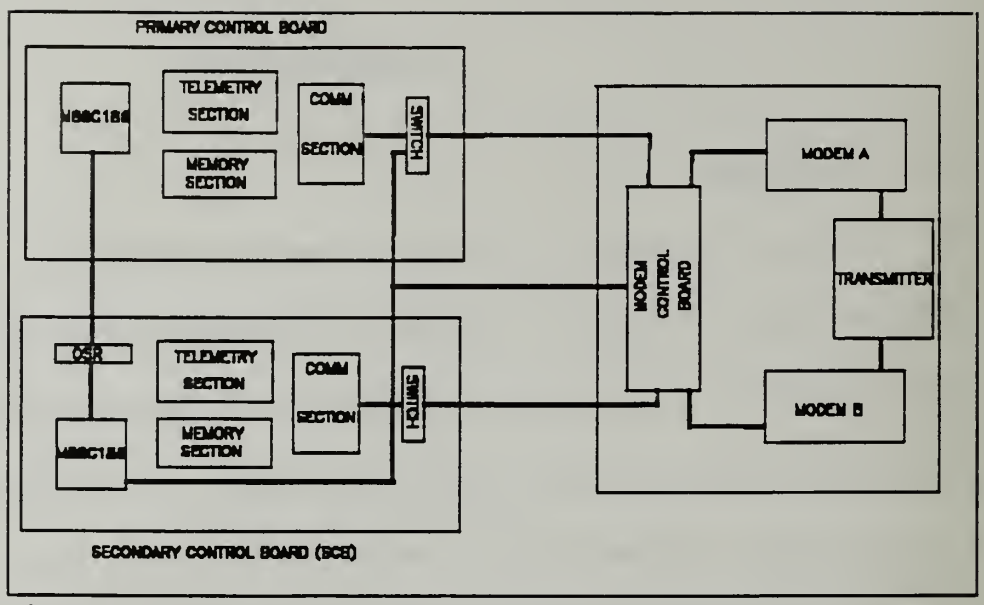


Figure 1 Primary Control Board, Secondary Control Board Inter-relationship

The power system of the spacecraft, the battery, solar panels and voltage regulator cannot be controlled by two competing control boards. The design incorporates hardware which allows the various control signals to be switched into their respective circuits.

The PCB and the SCB are almost identical in design. Each board is designed to operate autonomously and to control the spacecraft systems unilaterally. By design, the SCB is programmed to determine which board is in control of the spacecraft. This implies that the software operating system for the SCB must have an additional routine to make this decision. The only physical difference in the two boards is a few pull up resistors and an Octal Latch. The microprocessor is the same on both boards. Both boards have the same quantity of memory, their own telemetry transducers and Analog

to Digital Converters (A/D). A more detailed discussion of the differences in hardware can be found in Chapter IV.

C. DESIGN REQUIREMENTS OF A CONTROL BOARD

The mission of PANSAT requires that the microprocessor be capable of handling multiple tasks. It is possible that during certain times while orbiting the earth, the microprocessor will be required to monitor telemetry, transmit a message to earth, receive a message from earth and adjust the voltages on the solar panel arrays, all at the same time. A system capable of performing several operations simultaneously had to be developed.

There are a significant number of telemetry sampling points. The system requires a large memory to store collected data from these points. Combine this data requirement with the need to store a large number of messages and the necessity for a large quantity of memory is apparent. This design incorporates four Mbytes of memory. The DCS is implemented in a way which allows the microprocessor to address beyond one Mbyte of memory. Accordingly, a method of addressing via some peripheral control device was developed.

D. DESIGN IMPLEMENTATION OF A CONTROL BOARD

A multitasking operating system for PANSAT was developed. This system allows the microprocessor to preform several tasks simultaneously. The microprocessor and it's peripherals carry out the mission of the satellite, which is to dependably collect and forward Spread Spectrum message traffic from amateur stations around the world. The

hardware configuration developed in this thesis is designed to take advantage of multitasking software.

E. SCOPE OF THESIS

Chapter II is a description of the design for the PCB and SCB bus control circuitry. The control boards are required to access several peripherals. These peripherals require a programmable peripheral interface (PPI) be coupled with the microprocessor to operate correctly. In Chapter II, implementation of the PPI is discussed in detail, with hardware implementation and software initialization described.

Chapter III describes the implementation of the memory system. The M80C186 cannot address greater than one Mbyte of memory without external support. By placing memory into 512 Kbyte blocks and treating them as peripherals, the PPI can be used to implement a paging system. This design is described in detail in Chapter III with schematics of the design located in Appendix A.

Telemetry collection is critical to the operation of the spacecraft. Chapter IV details the design of the telemetry section. The microprocessor is required to control the voltage regulation system of PANSAT based on voltage readings of the various busses throughout the spacecraft. It must make real time adjustments to provide a consistent operational environment.

PANSAT is designed to be a store and forward communications satellite. In Chapter V, the communications section is described. This section is implemented using Advanced Micro Devices' 85C30 Serial Communications Controller (SCC). The chapter

describes the communications section from the microprocessor up to the modems. The SCC and the RS422 protocol it uses to communicate with the modems is described.

II. BUS CONTROL CIRCUITRY DESIGN

A. GENERAL

The Bus Control Circuitry consists of the microprocessor and peripheral devices needed to control the various subsections of the control boards. The M80C186 coupled with an 82C55 Programmable Peripheral Interface were selected to be the cornerstone of the bus control design. The design and implementation of these devices are described in the following sections.

B. DESIGN IMPLEMENTATION OF A CONTROL BOARD

1. Intel M80C186 CHMOS High Integration 16-Bit Microprocessor

a. Reasons for the Selection of the M80C186

Intel's M80C186 microprocessor, shown in Figure 2 was selected from a large offering of commercially available devices. Some important reasons for the selection of this device were:

1. Proven architecture
2. High Radiation tolerance
3. Low power consumption
4. Compatible with design requirements of PANSAT
5. Development tools in hand

6. Personnel with hardware and software experience with the M80C186

7. Capable of supporting a multitasking environment

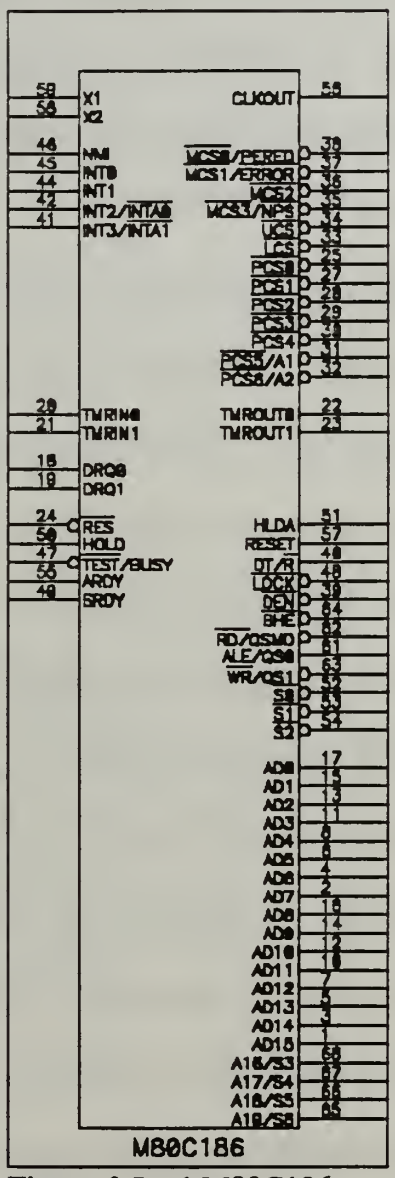


Figure 2 Intel M80C186
Package Pin Out

The PANSAT design required a moderately fast device capable of operating in a real time mode. The 10 MHz M80C186 microprocessor performs effectively in this task.

b. Desirable Features

Intel developed the M80C186 to replace it's family of 8086 devices. [Ref.1: p. 24-25] The M80C186 uses an 8086 microprocessor, but requires very few peripheral support devices. In fact, the more useful peripheral devices are implemented on the chip. This highly integrated device has the following features which were used in the design implementation.

(1) Clock Generator Circuit. Three internal 16-bit clocks are available. This feature is used to perform two critical tasks. Two of the timers are used to produce the asynchronous pulse width modulated signal for the voltage regulator circuit. Timer C is used on the SCB as a watchdog timer to determine when to assume control of the spacecraft.

(2) Two Independent Direct Memory Access (DMA) Channels. This feature is used extensively by the communications section. The actual transmission of data is performed at 1200 baud. This is very slow compared to the frequency of the M80C186. By using the DMA, the microprocessor does not have to wait for the data to be transmitted. It will initiate the transmission, or reception and continue with other tasking. This is discussed in greater detail in Chapter V.

(3) Programmable Interrupt Controller. A multitasking environment requires the microprocessor to perform several tasks at once. This feature simplified the design of the telemetry section. Chapter IV discusses this feature in more detail.

(4) Programmable and Peripheral Chip Select Logic. The M80C186 has six peripheral chip select lines and six memory select lines. This feature dramatically simplified the design of the memory section and is discussed in much greater detail in the memory chapter. The peripheral chip select lines are not used as extensively. Peripheral Chip Select 0 (PCS0) is the only line incorporated into this design. It is used to enable the Programmable Peripheral Interface chip.

(5) Programmable Wait State Generator. The wait state generator simplifies the bus read and write operations. It allows the 82C55 Programmable Peripheral Interface (PPI) to be operated with the M80C186 without any supporting delay circuitry.

(6) Direct Addressing Capability to One Mbyte of Memory and 64 Kbytes of I/O Space. Although the microprocessor is a 16-bit device, it has twenty address lines available. The 80C186 can address directly up to one megabyte of memory. This minimizes the quantity of logic required to address above 64 Kbytes. Several other features are available on this device, however, they were not used for the initial implementation of the design.

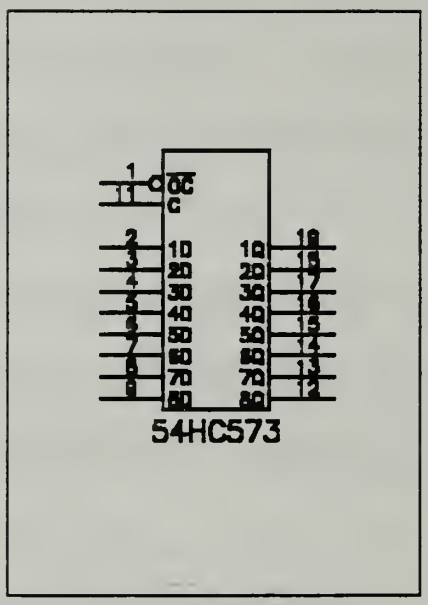


Figure 3 Address Latch

2. 54HC573 Octal Latch [Ref. 2: p. 3-320]

The 54HC573 Octal Latch, shown in Figure 3, was selected to provide address latching because of the following characteristics:

1. V_{CC} = +5V
2. Typical Propagation Delay: 13 ns
3. Operational Temperature Range: -65°C to +150°C
4. Compatible with bus oriented systems

The M80C186 uses twenty address lines to access memory and Input/Output

(I/O). The first sixteen of these lines are also used for data lines after the first time period. To ensure stable addresses were available for memory and peripheral devices, the address must be latched. Three 54HC573 Octal Latches were used to implement this portion of the design (See Appendix A, Drawing One). The chip enable on this device was connected to the M80C186 via the Address Line Enable (ALE) pin. When the microprocessor places the desired address onto the Address/Data (A/D) Bus, the ALE line will go active causing the HC573 to latch the address. The HC573's are implemented in parallel to ensure full twenty bit addresses are available. The address is placed on the Latched Address (LA) Bus. All peripheral devices will access addresses via the LA Bus.

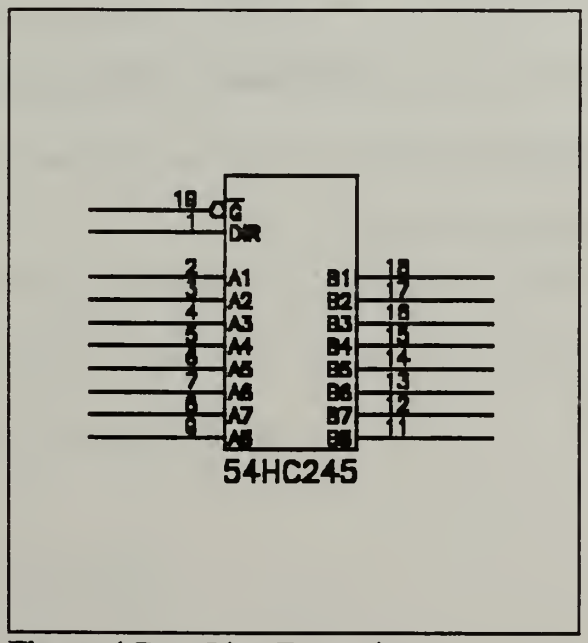


Figure 4 Data Line Transceiver

3. M54HC245A Octal Tri-State Transceiver [Ref. 2: p. 3-226]

The M54HC245A Octal Tri-State Transceiver, shown in Figure 4, was selected for this tasking because it has the following desirable characteristics:

1. V_{CC}= +5 V
2. Typical Propagation Delay: 13 ns
3. Compatible with bus oriented systems

Data lines from the M80C186 are connected to two HCS245 Transceivers (The HCS245 was selected because of it's high speed and high reliability). These buffer the outputs from the microprocessor, preventing overloading on the output pins of the M80C186. All peripheral devices are connected on the Buffered Data (BD) lines with the exception of the Am85C30 Serial Communications Controller. The Am85C30 design implementation is discussed in Chapter V.

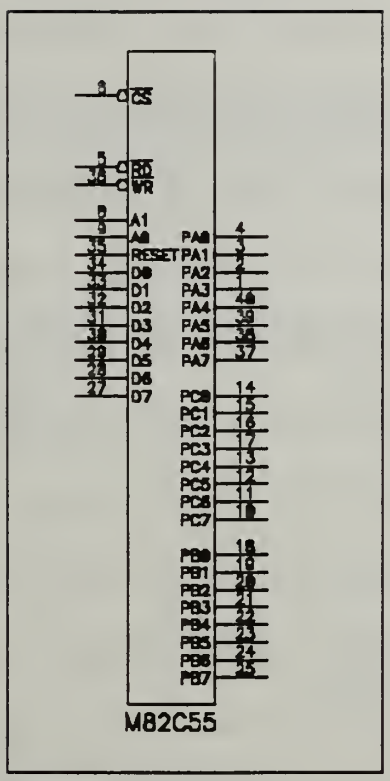


Figure 5 82C55 PPI

4. 82C55 Programmable Peripheral Interface (PPI) [Ref. 3: p. 3-124]

The Intel 82C55 PPI, whose pinout is given in Figure 5, was selected for PANSAT use for the following reasons:

1. Low Power CHMOS
2. High Speed, designed for operations with the M80C186
3. Extended Temperature Range

4. 24 Programmable I/O Pins

a. General

Control of peripheral devices is accomplished via the 82C55 PPI. A method of controlling a significant number of peripheral devices was necessary. The telemetry requirements required several multiplexers as well as an A/D converter to be controlled by the microprocessor. The M80C186 only has six peripheral control lines, while the 82C55 can be used to control up to 64 peripheral devices.

PANSAT requires four Mbytes of memory. The M80C186 can directly address only one Mbyte. The implementation of the 82C55 included a method of paging in blocks of memory. The memory design is discussed in detail in Chapter III.

Intel's 82C55 PPI was selected for the task of interfacing peripherals because of it's compatibility with the M80C186. Functionally it is a programmable, general purpose I/O component interface. Its configuration can be controlled via software. The total number of required external logic devices can be minimized by using the PPI.

b. Initializing the PPI

Programming the PPI is accomplished via a series of write commands to control registers. PCS0 is programmed to be active during any I/O operation. This M80C186 pin is connected to the "chip enable" pin on the 82C55. Write commands or read commands to the first one Kbyte of I/O space results in this pin being active. Table

2.1 below lists the addresses of the various ports and control registers of the PPI. The 82C55 can be programmed to operate in several configurations. The configuration most suitable for PANSAT operations is Mode 0. Mode 0 is the basic input/output mode of the 82C55. It provides for simple input and output operations for each of it's three ports. No handshaking is required for any of these operations.

TABLE 2.1 PROGRAMMING ADDRESSES FOR PPI [Ref. 3: p. 3-125]

A1	A0	RD	WR	CS	Input Operation (Read)
0	0	0	1	0	Port A-Data Bus
0	1	0	1	0	Port B-Data Bus
1	0	0	1	0	Port C-Data Bus
1	1	0	1	0	Control Word-Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus-Port A
0	1	1	0	0	Data Bus-Port B
1	0	1	0	0	Data Bus-Port C
1	1	1	0	0	Data Bus-Control Word
					Disable Function
X	X	X	X	1	Data Bus-3-State
X	X	1	1	0	Data Bus-3-State

In Mode 0, several pin function configurations are available. One of these is control word #2 (42H) and it was selected as the most suitable for the design requirements. To program the PPI to operate in Mode 0, control word #2, control word #2 must be written into the control register, at absolute I/O address 03H. This line up

will allow the 80C186 to operate it's peripheral devices and should only be necessary when the system initializes.

TABLE 2.2 PERIPHERAL CONTROL ADDRESSES

A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0	Description of Peripheral Device
0	0	0	0	0	0	0	0	ICL7115
0	0	0	0	0	0	0	1	Memory Block 0
0	0	0	0	0	0	1	0	Memory Block 1
0	0	0	0	0	1	0	0	Memory Block 2
0	0	0	0	1	0	0	0	Memory Block 3
0	0	0	1	0	0	0	0	Memory Block 4
0	0	1	0	0	0	0	0	Memory Block 5
0	1	0	0	0	0	0	0	Memory Block 6
1	0	0	0	0	0	0	0	Serial Communications Controller
0	0	0	0	0	0	1	1	Operational Status Register

Intel's Programmable Peripheral Interface is used to control several peripherals on board PANSAT. Mulitiplexers to align current to Temperature Detecting Diodes (TDD), multiplexers to align signals to the A/D Converter, several blocks of memory and the Serial Communication Controller. Table 2.2 lists the word which must be written to Port C to control the various peripherals.

PANSAT does not require any more peripherals at present. With the 82C55, up-grades to the design can be accomplished with ease. Simply adding the control lines

and adding a few lines of code to the operating system will place another peripheral device on line. This form of control also simplifies the software requirements. Peripheral control is performed via two possible I/O addresses. Port A or Port C of the PPI.

III. MEMORY SECTION

A. GENERAL

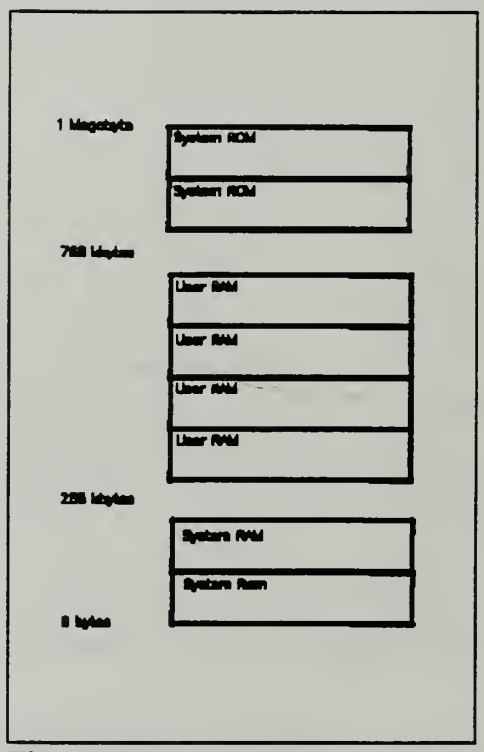


Figure 6 Memory Map

The Memory Section of the Digital Control System has many functions, all of them critical to the operations of the satellite. Memory is used to store telemetry, message traffic and operating code. Read Only Memory (ROM) and Random Access Memory (RAM) make up PANSAT's memory. ROM provides a permanent storage area for the Operating System. RAM is used for two primary purposes, to store the

operating system and to temporarily store telemetry and message traffic. The operating system is copied into low RAM whenever the M80C186 resets. Because RAM is much faster this increases the overall operating speed of the system. Memory is organized as shown in Figure 6, the memory map.

The Memory Section of the Control Board consists of four megabytes of storage. There is 256,000 bytes in ROM and 3.5 Mbytes are in static RAM. The ROM is used for permanent storage of the operating system while the RAM is split into two types, system RAM and user RAM. The system RAM is used by the operating system for computer control/programming. The remaining three Mbytes of RAM are used for bulk storage of telemetry data and message traffic. A detailed schematic of System ROM, System RAM, and Mid-Range RAM are given in Appendix A.

B. SYSTEM ROM

1. Design Requirements

The Operating System is stored in 256 Kbytes of System ROM which contains all the necessary software for the satellite to begin communicating with the Master Station. PANSAT cannot operate without system ROM. Since this section of the system is critical, some redundancy had to be incorporated into the design. To provide the necessary redundancy, switchable ROM was designed. After each system reset, the microprocessor boots up on ROM which was not enabled prior to the reset. Any revisions to the Operating System following launch will be temporary, since the

ROM can only be programmed prior to launch. This requires that the Operating System be updated after every reset.

2. Design Implementation

System ROM has a permanent storage capacity of 256 Kbytes. To implement ROM for each Control Board four WS27C010Ls were used. Two of these chips provide the required 256 Kbytes. However, the System ROM design incorporates a standby spare section. This standby section is identical to the on line section. The reset circuit of Figure 7 determines which section is in standby and which is not.

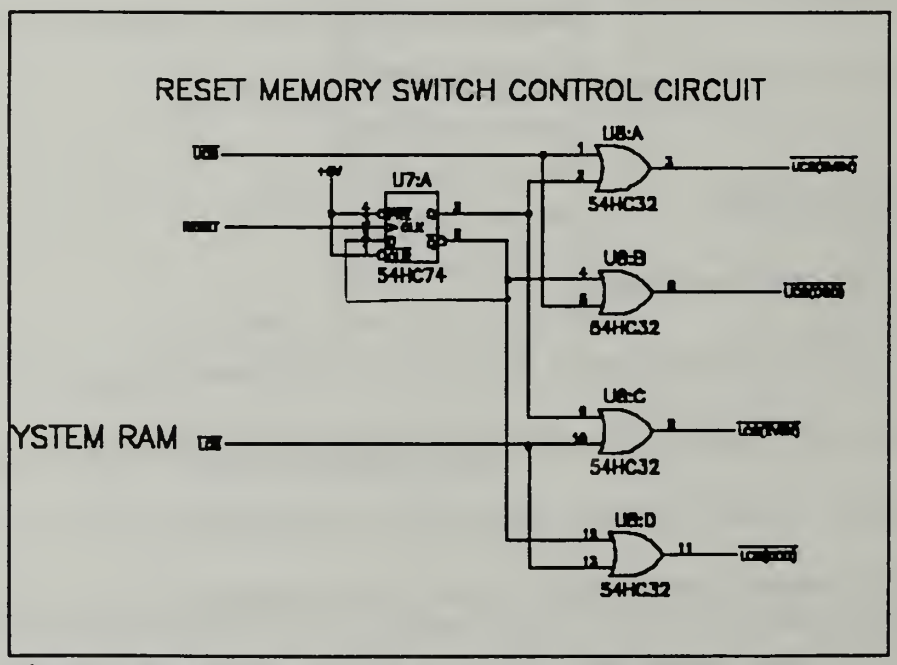


Figure 7 Reset Circuit

a. Reset Circuit Design Implementation

Failure of system ROM may result in the loss of a control board. With this in mind a Reset Section, shown in Figure 7 was designed. This section causes the

system ROM to be switched whenever the microprocessor undergoes a reset. This ensures that PANSAT will not be degraded in a significant manner with the loss of a section of system ROM. All devices used to build the Reset Circuit must be radiation hardened to ensure a single event upset does not cause a ROM switch during normal operations of the Digital Control System (DCS). The Reset Circuitry shown in Figure 7 is also used to reset the System Ram.

Several companies have developed a number of radiation hardened devices which meet the requirements of the PANSAT design. The following were used in the design of the Reset Circuit (Devices in the schematic reflect the prototype design which uses Commercial Chips vice the MilSpec Chips).

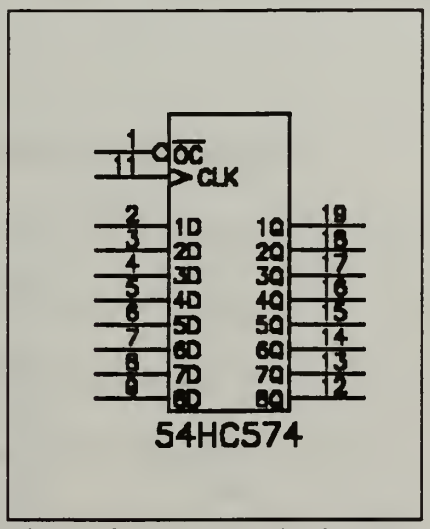


Figure 8 HCTS74MS Pin Out

(1) HCTS74MS High Reliability, Radiation Hardened, High-Speed CMOS/SOS Octal-D Flip-Flop [Ref. 4: p. 12-32]. The HCTS74MS shown in Figure 8 was selected for the reset circuitry for the following reasons:

1. Radiation hardened to 200K rads
2. Single Event Upset Immunity typically $2x10^{-9}$ errors/bit-day
3. Latch-up free under transient radiation
4. Transient upset > 10^{10} rads/sec, 20 ns pulse
5. Typical propagation delay = 21 ns
6. V_{cc}=4.5 to 5.5 V C_L= 50 pF, T_A=25°C
7. Wide operating temperature range: -55 to +125°C

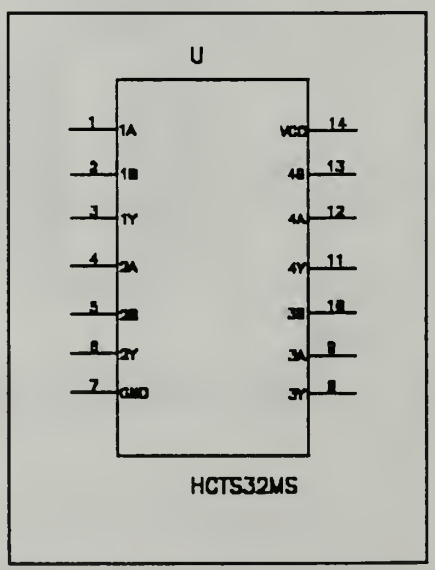


Figure 9 HCTS32MS Pin Out

(2) HCTS32MS, High Reliability, Radiation-Hardened, High-Speed CMOS/SOS Quad 2-Input OR Gate [Ref. 4: p. 12-20]. This device, shown in Figure 9 was selected for numerous applications in the DCU design, including the reset circuit, the following reasons:

1. Radiation hardened to 200K rad
2. Single Event Upset immunity typically $2x10^{-9}$ errors/bit-day
3. Latch-up free under transient radiation
4. Transient upset > 10^{10} rads/sec, 20 ns pulse
5. Temperature -55 to +125°C
6. V_{cc}=4.5 to 5.5 V

b. ROM Chip Design Implementation

Waferscale Integration Incorporated's ROM chip was selected to implement this section. Each chip has 128 x 8 Kbytes of read only memory. This section was designed to allow the microprocessor to address either words or bytes of memory. This is accomplished via the circuit given in Figure 14. Branch High Enable (BHE), a control pin on the M80C186 is tied to the Chip Select 2 (CS2) pin on the ROM chip. The Latched Address 0 (LA0) pin of the HC573 Octal Latch is connected to the CS2 line on the lower bank of ROM chips. The design is further illustrated in Appendix A.

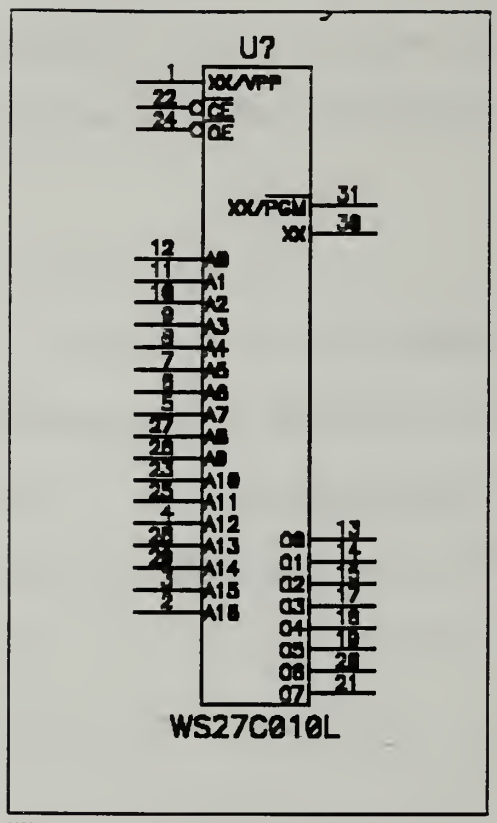


Figure 10 EPROM Package Pin Out

(1) WS27C010L, 128 x 8 Kbyte Erasable Programmable Read Only Memory (EPROM) [Ref. 5: p. 3-93]. This device, shown in Figure 10, is a high performance CMOS device. It is electrically programmable and UV erasable. Some of the desirable characteristics of this chip are listed below.

1. Access time = 100 nanoseconds
2. V_{cc} = 5.0 V
3. I_{cc} = 60 mA (when active),

4. Power Consumption per chip ≃ 300 mW (when active)

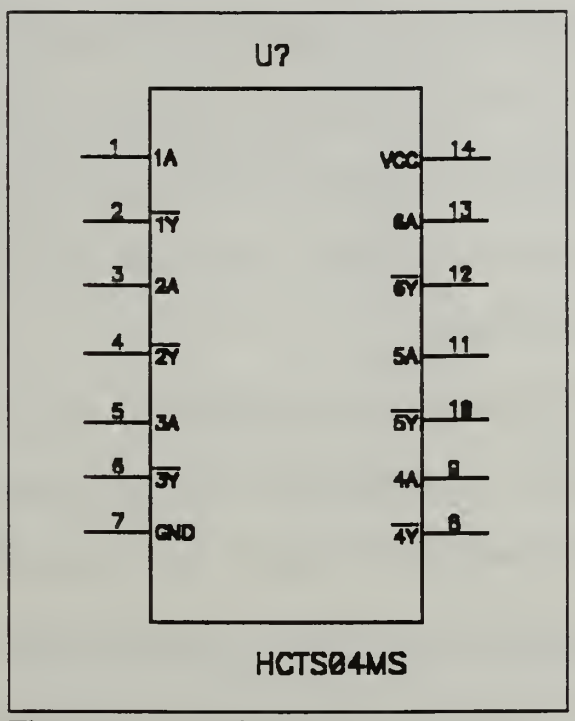


Figure 11 HCTS04MS Hex Inverter

(2) HCTS04MS High Reliability, Radiation Hardened, High-Speed CMOS/SOS Hex Inverter [Ref. 4: p. 12-16]. The device, shown in Figure 11 and used in the memory chip select circuit of Figure 14, was selected for the following reasons:

1. V_{CC}= +5 V
2. Propagation Delay = 12 ns
3. Radiation Hardened to 200 K rad
4. Cosmic ray upset immunity = 2 x 10^{-9} errors/bit/day

3. Programming the M80C186 for System Read Only Memory Operations

Addressing of ROM is accomplished directly via the M80C186 microprocessor. As discussed and shown earlier in the Memory Block Diagram, Figure 6, the ROM addresses are "logically" located in the upper 256 Kbytes of addressable memory. To read data stored in this section of memory, the ROM chips must be enabled. The "chip enable" pin of the WS27C010L is tied to the Upper Chip Select (UCS) line of the M80C186 via reset circuitry.

UCS is programmed to be active whenever an address above C0000H is used. Programming of the UCS is accomplished by entering the lower address of upper memory into the "Upper Memory Chip Select" (UMCS) Register. This allows the upper memory block size to be defined by the user. The possible block sizes and the values required in the UMCS necessary to define those sizes are listed in Table 3.1.

The Digital Control System microprocessor has an upper memory block of 256 Kbytes. The value C038H is written into the UMCS register when the system is initialized. The location of the UMCS register is dependent on the location of the Control Block.

TABLE 3.1
UPPER MEMORY CHIP SELECT REGISTER VALUES [Ref. 1: p.24-78]

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1 KBYTE	FFF8H
FF800	2 KBYTE	FFB8H
FF000	4 KBYTE	FF38H
FE000	8 KBYTE	FF38H
FC000	16 KBYTE	FC38H
F8000	32 KBYTE	F838H
F0000	64 KBYTE	F038H
E0000	128 KBYTE	E038H
C0000	256 KBYTE	C038H

The M80C186 Control Block is defined at initialization. The microprocessor Control Block is a sequence of registers which have a beginning address defined by the user. The absolute address of the Relocation Register for this design is defined as 20FFH in the addressable I/O space (This address is the default address whenever the microprocessor is reset). The Relocation Register is also located in the Control Block, but it is offset FEH from the starting address. This implies the starting block of the Control Block is at FF00H in I/O space. Upon initialization of the system FF00H is written into absolute address 20FFH.

The UMCS register address is in the Control Block at offset A0H. The absolute address is FFA0H in the I/O space. Whenever the microprocessor initializes,

it will write C038H to FFA0H. Upon completion of the above steps, the UCS line will be active for addresses above C0000H.

The UCS line from the microprocessor is tied to an HCTS32MS "OR" gate. This signal is logically combined with the output of a D type Flip-Flop to provide switching capability to the System ROM.

C. SYSTEM RANDOM ACCESS MEMORY (RAM)

1. General

Read Only Memory is used to permanently store the Spacecraft's Operating System. Although the ROM flown in PANSAT is very fast, it is slow in comparison to RAM. To enhance the overall system operations, the first action the microprocessor will carry out after a reset is the loading of system RAM. The Operating System located in ROM will be moved to the lower 256 Kbytes of RAM. This software is designed to be upwardly compatible with any revisions transmitted after the launch of the spacecraft. Whenever a reset occurs, these new revisions will be lost and it will thus be necessary for the Earth Station to intervene to bring the system back on line in the pre-reset configuration. System RAM is also the location of all interrupt vectors. These vectors are loaded from ROM after a reset.

2. Design Requirements

The design of System RAM is almost identical to that of the System ROM. 256 Kbytes is required. Since system RAM is also critical to PANSAT operations,

redundancy was designed into this section. The only difference in the two designs is the type of Memory Storage Device.

When a reset occurs the ROM/RAM Reset circuit, shown in Figure 7, will toggle the enable line to the system RAM chips. This will ensure that after any Reset, the next reboot will be on the System RAM chips which were not operating when the reset generating event occurred. This precaution will prevent a loss of control board redundancy if a RAM chip in System RAM fails (Note: Time out of the SCB control assumption routine should allow enough time for a system reset of the Primary Control Board).

3. Design Implementation

System RAM is comprised of four MSM8128S/J Monolithic CMOS SRAM. Although only two devices are necessary to provide 256 Kbytes of RAM, there are four chips per control board flown as system RAM. This provides the reset capability necessary to prevent the loss of a control board when system RAM fails. The reset circuitry is the same circuit used for ROM and comprises the same chips.

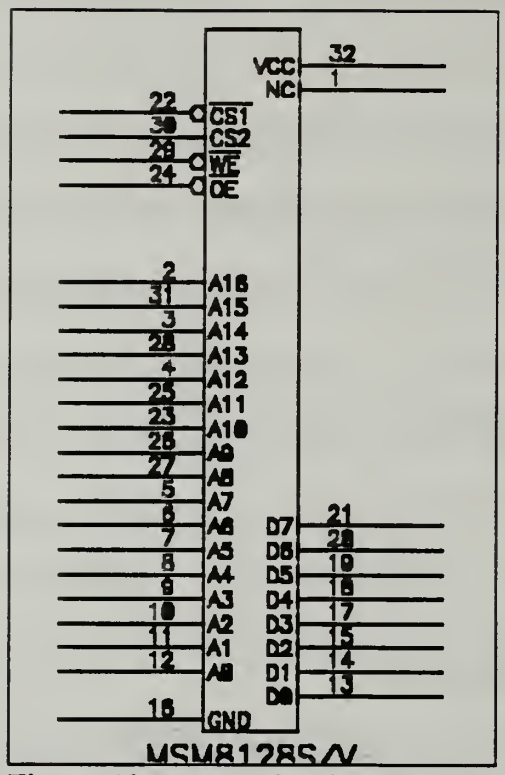


Figure 12 RAM Chip Pin Out

a. MSM8128S/J 128K x 8 CHMOS SRAM [Ref. 6: p. 2-69]

This Mosaic device , the pin out of which is given in Figure 12, was selected to serve as the static RAM on board PANSAT because it has the following useful characteristics:

1. Access time = 85 nanoseconds
2. V_{cc} = 5.0 V
3. Power consumption in standby = 10μW
4. Power Consumption per chip (when active) = 75 mW

b. HCTS74MS (see B.2.a.1)

The HCTS74MS was selected for use in this section of the circuit because of it's excellent characteristics. These characteristics are listed in section B.2.a.1.

c. HCTS32MS (see B.2.a.2)

The HCTS32MS high reliability "or" gate was selected because of it's excellent characteristics. The list of these characteristics is given in section B.2.a.2.

Note: The Schematic Diagram of the System RAM is located in Appendix A.

4. Programming the M80C186 for System Random Access Memory Operations

System RAM is logically located as the low 256 kbytes of memory as shown in Figure 6. The Chip Enable lines from the RAM chips must be enabled when the microprocessor addresses one of these lower addresses. The M80C186 does this using the Lower Chip Select (LCS) line. The characteristic behavior of this output is similar to the UCS discussed previously.

LCS is active over a range of addresses which must be defined by the user. The lowest address is 0H. This address can never be changed. The upper address of the LCS active region can be programmed by writing one of the allowed values, listed below in Table 3.2, into the Lower Memory Chip Select Register (LMCS).

TABLE 3.2 LMCS PROGRAMMING VALUES [Ref. 1: p.24-79]

Upper Address	Memory Block Size	LMCS Value (Assuming R0=R1=R2)
003FFH	1 KBYTES	0038H
007FFH	2 KBYTES	0078H
00FFFH	4 KBYTES	00F8H
01FFFH	8 KBYTES	01F8H
03FFFH	16 KBYTES	03F8H
07FFFH	32 KBYTES	07F8H
0FFFFH	64 KBYTES	0FF8H
1FFFFH	128 KBYTES	1FF8H
3FFFFH	256 KBYTES	3FF8H

The LMCS Register is located in the Control Block at offset A2H. The control board has 256 Kbytes of system RAM. Therefore, the upper address must be programmed to 3FFFFH. This is accomplished by writing 3FF8H to the LMCS at absolute address 0FFA2H. After system initialization is completed, the LCS line will be active for any addresses between 00000H and 0FFA2H.

The LCS line from the microprocessor is tied to an HCTS32MS "OR" gate. This signal is logically combined with the output of a D type Flip-Flop to provide switching capability to the System RAM. All interrupt vectors, the operating system and system subprograms reside in the System RAM.

D. USER RANDOM ACCESS MEMORY (Mid-Range Memory)

1. Design Requirements

Mid-Range memory is the location for bulk storage of data. This region is used as a "Mail Box" for any message traffic and as a location to store excess telemetry data. To ensure adequate storage for any future requirements of PANSAT, 3.5 Mbytes of Static RAM is installed on each Control Board as shown in Figure 13. The M80C186 is capable of directly addressing only 1 Mbyte of memory. To allow the microprocessor to use the extra memory, the 82C55 Programmable Peripheral Interface (PPI), in conjunction with six blocks of 512 Kbytes of random access memory was used.

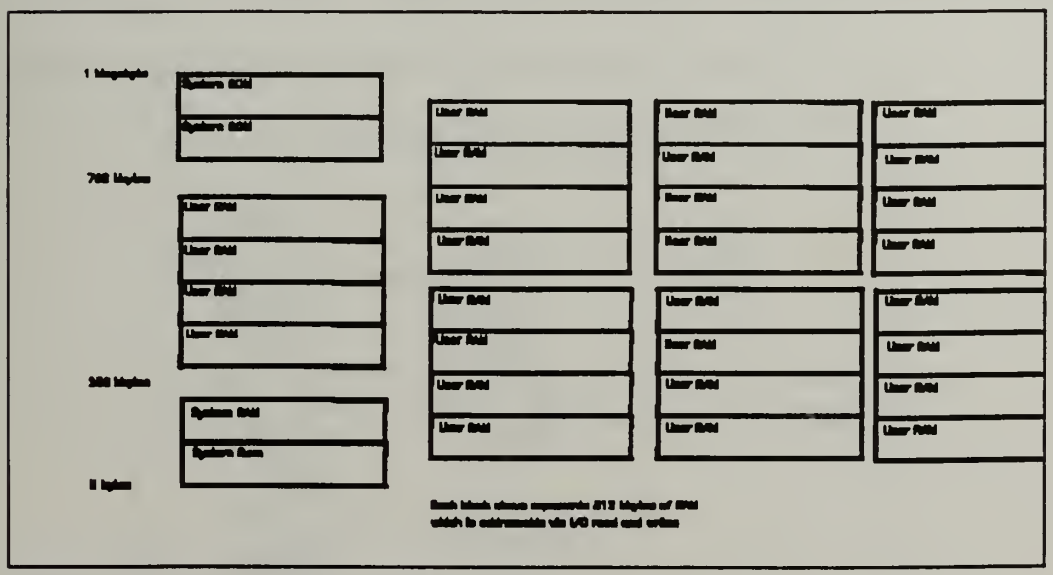


Figure 13 Paged Memory Block Diagram

2. Design Implementation

a. 82C55 PPI Operations with the Memory Section

The PPI allows the middle region of RAM to be accessed via an I/O port specifically Port C of the 82C55. Memory blocks are comprised of 512 Kbytes of random access memory. Six blocks provide three Mbytes of additional RAM. These blocks are addressed via the PPI. This allows the microprocessor to determine which of the six blocks of memory it needs to activate to access a specific memory location. If each block is later defined for a specific task, i.e. "User Mailbox", then this will add only the write to port C at the beginning of an operation. In other words, as long as the microprocessor does not need to shift to another block of RAM, there will be no increase in the time required to complete a specific operation.

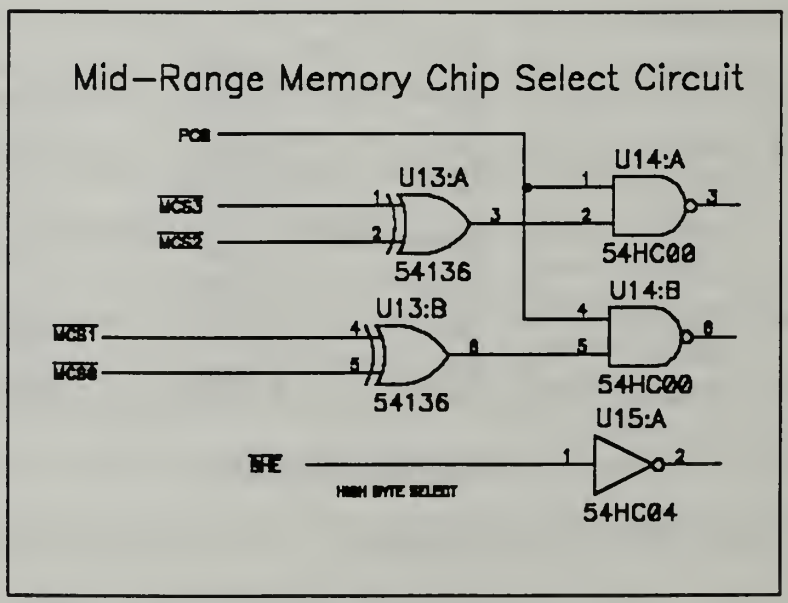


Figure 14 Memory Chip Select Circuit

b. Address Selection Circuitry

Logical switching between blocks of memory and between memory chips is accomplished using the M80C186 Mid-Range Memory Chip Select lines and the PPI. A logical combination of these signals is used to enable the various RAM chips. This selection circuit is shown in Figure 14. The devices used to implement this section are listed below:

(1) MSM8128S/J (see C.3.a.). Mid-range memory uses the same chip as the system RAM. It was selected because of it has several excellent characteristics. These characteristics are listed in section C.3.a.

(2) INTEL 82C55A Programmable Peripheral Interface. The PPI again proved to be very useful for interfacing peripherals. In this section it is used to control several blocks of memory. The physical characteristics of this devices are listed in Chapter II, section D.4.a.

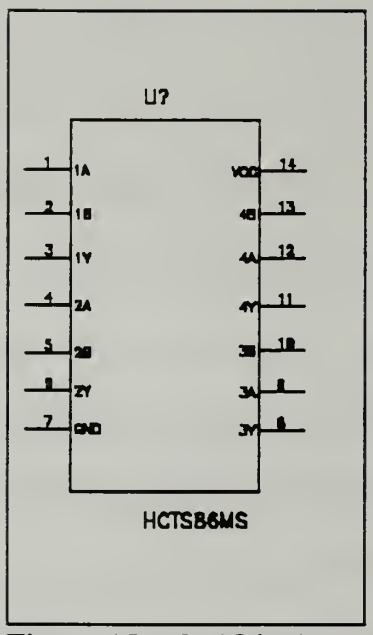


Figure 15 HCTS86MS
Package Pin Out

(3) HCTS86MS High Reliability, Radiation-Hardened, High-Speed, CMOS/SOS Quad 2-Input Exclusive-OR Gate [Ref. 4: p. 12-21]. This device, whose pin out is given in Figure 15, was selected because it has the following characteristics:

1. V_{CC}= +5V
2. Radiation Hardened to 200 kilo rads
3. Cosmic ray upset immunity = 2 x 10^{-9} errors/bit-day
4. Propagation Delay = 21 nano seconds

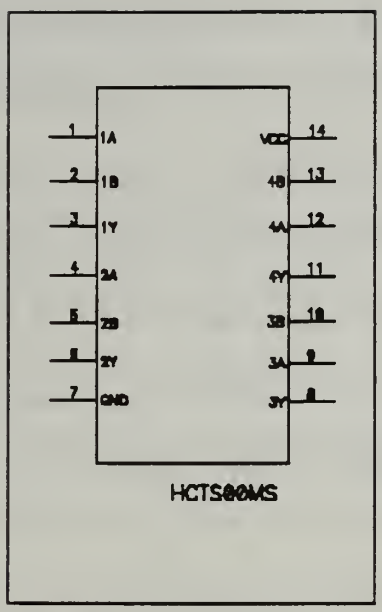


Figure 16 HCTS00MS
Package Pin Out

(4) HCTS00MS High Reliability, Radiation Hardened, High-Speed CMOS/SOS Quad-2 Input NAND Gate [Ref. 4: p. 12-25]. The HCTS00, given in Figure 16, was selected for because it has the following characteristics:

1. V_{CC}= +5V
2. Radiation Hardened to 200 kilo rads
3. Cosmic ray upset immunity = 2 x 10^{-9} errors/bit-day
4. Propagation Delay = 21 nano seconds

(5) HCTS04MS High Reliability, Radiation Hardened, High Speed CMOS/SOS Hex Inverter [Ref. 4: p. 12-16]. The HCTS04 discussed in section B.2.b.2 was also used in this section.

3. Programming the 82C55 PPI for Mid-Range Memory Operations

After system initialization, the PPI will already be in Mode 0, Control Word #2 (for a more detailed explanation see the discussion concerning the 82C55 in Chapter II). In this configuration, the 82C55 will have Port A active as a latching output. Port C will be active as a latching output, and Port B will be active as an input. The microprocessor will write one of the control bytes shown in Table 3.3 to Port C to activate a specific block of memory. Port C has the absolute address of 0002H in I/O space.

TABLE 3.3 CONTROL WORD FOR ACCESS TO MEMORY BLOCK

Contrl Word	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0	Memory Block Selected
2	0	0	0	0	0	0	0	1	Memory Block #0
3	0	0	0	0	0	0	1	0	Memory Block #1
4	0	0	0	0	0	1	0	0	Memory Block #2
5	0	0	0	0	1	0	0	0	Memory Block #3
6	0	0	0	1	0	0	0	0	Memory Block #4
7	0	0	1	0	0	0	0	0	Memory Block #5
8	0	1	0	0	0	0	0	0	Memory Block #6

4. Programming the M80C186 for Mid-Range Memory Operations

After the microprocessor selects which block of RAM it needs to access, it will then retrieve the data. This requires the correct RAM chip to be enabled. The chip enable line of each device is connected to one of four middle memory chip select lines

on the M80C186 via the logic circuit shown in Figure 14. The four select lines are MCS0-MCS3. Each of these lines can be programmed to be active for various size blocks of memory.

Mid-Range Memory Select Lines are programmed to be active beginning at a specific address. They are also programmed to be active for a specific size block of memory. After the microprocessor is initialized, it must program these lines. The size of the memory block is controlled in the MPCS Register. This register is located in the Control Block at absolute address FFA8H (An offset of A8H from the beginning of the Control Block). Table 3.4 indicates which word generates which block size.

TABLE 3.4 MPCS PROGRAMMING VALUES [Ref. 1: p.24-79]

Total Block Size	Individual Select Size	MPCS Bits 14-8
8 Kbytes	2 Kbytes	0000001B
16 Kbytes	4 Kbytes	0000010B
32 Kbytes	8 Kbytes	0000100B
64 Kbytes	16 Kbytes	0001000B
128 Kbytes	32 Kbytes	0010000B
256 Kbytes	64 Kbytes	010000B
512 Kbytes	128 Kbytes	100000B

To implement the desired block size of 512 Kbytes, 40H is written into bits 14-8 of the MPCS register.

The base address for the mid-range memory is also programmable. This requires the base address to be loaded into bits 15-9 of the MMCS register. This register is located in the Control Block at offset A6H. These bits correspond to A19-A13 of the 20 bit memory address. The absolute address of the beginning of mid-range memory for this design is 40000H. In binary this number is 01000000000000000000B. Therefore, the number 010000B must be written into the MMCS register bits 15-9. After all programming is complete, the MCS lines will be active for a block of memory 512 Kbytes in size. Table 3.5 indicates which lines are active for each range of addresses.

TABLE 3.5 MID-RANGE MEMORY CHIP SELECT LINES TRUTH TABLE

ABSOLUTE ADDRESS IN HEX	**MCS0** (active low)	**MCS1** (active low)	**MCS2** (active low)	**MCS3** (active low)
40000 - 5FFFE	0	1	1	1
60000-7FFFE	1	0	1	1
80000-9FFFE	1	1	0	1
A0000-BFFFE	1	1	1	0

The select lines pass through the logic shown in Figure 14. The output from this logic enables 128K words of RAM. The complete Mid-Range Ram Schematic is shown in Appendix A.

5. Memory Power Consumption Calculations

Power consumption is not expected to be a problem. ROM is only accessed during initialization of the microprocessor. RAM is accessed significantly more, but typically only two chips are selected at any given moment. For this reason it is safe to assume that the remaining RAM devices will be in a low power state. The MSM8128S/J Monolithic CMOS SRAM and the WS27010L ROM have the following operational characteristics:

V_{CC}= +4.5 to +5.5 volts for both chips

Chip Type	Operating	Standby
RAM	I_{CC}= 45 mA typical	I_{CC}= 1.0 mA typical
ROM	I_{CC}= 60 mA typical	I_{CC}= 1.0 mA typical

Power Requirement per active chip = (5.5V)(45mA)=0.25 watts

Power Requirement per inactive chip = (5.5V)(1mA)=0.01 watts

To approximate the power requirement for the memory section, the following assumptions were made:

1. Only two RAM chips are active at any given time.
2. ROM is active an insignificant portion of the time.
3. RAM chips are active 10% of the time and inactive 90% of the time.
4. Address selection circuitry power requirements are insignificant.

These assumptions lead to the following memory section power consumption power calculations.

Total Power=(Pwr Active RAM Chips)+(Pwr inactive RAM chips)+(Pwr inactive ROM chips)

Total Power=2(.25w)(0.1)+10(.01w)+2(.01)(.9)+4(.01w)

Total Power=0.21 watts

IV. TELEMETRY SECTION

A. GENERAL

The Telemetry Section of the Digital Control System provides an interface between the microprocessor and the real world. The system collects physical data and converts it to digital code in a timely fashion for further transmission to the Master Control Station. This data is then used by the operators determine the health and welfare of various subsystems within the spacecraft.

The physical quantities which must be collected are listed in Table 4.1. Also included in the table is the type of signal to be measured and the location of the sample point.

The actual collection and conversion of the telemetry is time consuming. The quantity of data to be collected is significant. To ensure the microprocessor has time to carry out real time commands, an interrupt driven data collection system was designed.

B. DESIGN REQUIREMENTS

1. Temperature Collection Requirements

Temperature Detecting Diodes (TDD) are used as transducers to convert the temperature of various components into a usable signal. This signal is a differential voltage across the diode. To acquire accurate voltages, the TDD must be driven by a steady current. This current must be provided for a minimum of twenty milliseconds to

ensure the diode is warmed up and operating in the linear range. It must be noted here, due to the power restrictions, it is impossible to allow each diode to have it's own current source. An analog multiplexer provides a solution to this problem. By using the MUX the current source is aligned to the TDD only during the warm up period and subsequent sampling time.

TABLE 4.1 SAMPLING REQUIREMENTS

Physical Quantity	Signal Type	Sample Point
Array Voltages	Volts	Solar Arrays
Battery Volts	Volts	Battery Terminals
Panel Temperature	Dif. Volts	Solar Panels
Solar Panel I-V Performance	Dif. Volts	Solar Panel Circuitry
Watts	Dif. Volts	Control Board Power Bus
Watts	Dif. Volts	Transmitter Power Bus
Watts	Dif. Volts	Receiver Power Bus
Degrees C	Dif. Volts	Battery Casing
Degrees C	Dif. Volts	Center of Control Board
Watts	Dif. Volts	Transmitter Power Bus Output
Watts	Dif. Volts	Received Signal Power Detection Circuit
Degrees C	Dif. Voltage	Transmitter (internal)
Degrees C	Dif. Voltage	Receiver (internal)

Power restrictions minimize the number of discreet devices which can be placed on the circuit board. With a second series of analog multiplexers, the various signals are routed to a single Analog to Digital (A/D) Converter. The microprocessor must orchestrate the operation of the A/D Converter and the various multiplexers to ensure usable data is collected. To provide the microprocessor enough control lines to operate so many peripheral devices, a PPI is required.

2. Non-Temperature Telemetry Signal Sampling

All other physical signals and analog data must be converted to a differential voltage signal. This signal is then multiplexed into the A/D converter and saved in a binary format. The various voltage measurements do not present a problem. Their magnitude is stepped down to allow for more uniform signals to the A/D converter. The various power signals are converted to a differential voltage which is proportional to the actual power. This again allows uniformity in sampling.

With all of the signals provided to the A/D Converter as differential voltages, then the telemetry section needs only one Conversion device. The range for the differential voltage signal is +5 volts to 0 volts.

C. OPERATIONAL DESCRIPTION OF SAMPLING SEQUENCE

1. Sampling Initialization (TDD Warm Up)

Telemetry sampling begins when the microprocessor (μP) writes a command word to the PPI. This command word aligns the PPI allowing the next command word from the μP to align the current source multiplexers as well as the signal to the A/D

converter multiplexers. The μP then writes a word to "Timer 2" (an internal timer on the M80C186) which generates an interrupt in about twenty five milliseconds. [Ref. 1:p. 24-86] The M80C186 then returns to other operations or handles higher priority interrupts.

2. Timer Interrupt

The Timer 2 interrupt vectors the μP to a subroutine which again writes a command word to the PPI enabling the ICL7115 via port C. The μP pulses the 'Write' line, initiating the conversion process. This completes the Timer 2 interrupt routine and the M80C186 returns to other jobs.

3. Conversion Cycle

When the conversion process is completed, the A/D Converter generates an End of Conversion (EOC) signal. This signal generates an "Interrupt 3" signal. [Ref. 1:p.24-88] If the μP is not handling a higher level interrupt, it is vectored to a collection subroutine. This subroutine reads the converted data into a memory location. The routine then aligns the next sample point to the current source (if a temperature is measured) and initializes Timer 2. Upon completion of the collection/realignment the μP returns to normal operations.

D. IMPLEMENTATION

1. General

The design of the telemetry section was parsed down into several subsections. the current source alignment circuitry, the analog signal alignment circuitry, the analog to digital converter circuitry and the telemetry control circuitry. These circuits are illustrated in Drawing Eleven, Appendix A.

2. Current Source Alignment Circuitry

The current source alignment circuitry is required to align a steady state current to the TDD's. There are several of these located throughout PANSAT. They are:

1. Battery temperature-2 signals
2. Transmitter temperature-1 signal
3. Receiver temperature-1 signal
4. Control board temperature-2 signals
5. Solar Panel Temperatures-17 signals

There are 23 sample points which require the current source to be aligned. The devices used for this operation are the Analog Multiplexer AD7507 coupled with the 82C55 PPI (See descriptions of devices listed in 3.a and 3.b).

3. Signal Alignment Circuitry

The Signal Alignment Circuitry is required to align all the telemetry points to the Analog to Digital Converter. The following signals are aligned to the ICL 7115 14-bit, High Speed, A/D Converter :

1. Battery Temperature-2 signals
2. Transmitter Temperature-1 signal
3. Receiver Temperature-1 signal
4. Control Board Temperature-2 signals
5. Solar Panel Temperatures-17 signals
6. Solar Cell I-V Curves-1 signal
7. Solar Cell Array Voltages-17 signals
8. Transmitter Signal Power Out-1 signal
9. Received Signal Power-1 signal
10. Control Board Power Use-2 signals
11. Transmitter Power Use-1 signal
12. Receiver Power Use-1 signal
13. Battery Voltage (Bus)-1 signal

There are 48 signals which must be aligned to the ICL 7115. This requires the use of six multiplexers. The telemetry section requires 11 AD7507 CMOS Multiplexers. Addressing of the various signal points is accomplished through Port A of

the PPI described below. The Truth Tables 4.2A-4.2C list the control signals required to align the signals described. TS1-TS7 are written to via LA1-LA7 (latched addresses), while TS0, written via LA0, toggles the high and low converted data.

TABLE 4.2A
TELEMETRY TRUTH TABLE
TS:= Telemetry Select (Lines from Port A of PPI)

TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0	SIGNAL DESCRIPTION
0	0	0	0	0	0	0	0/1	Battery Temp A
0	0	0	0	0	0	1	0/1	Battery Temp B
0	0	0	0	0	1	0	0/1	Transmitter Temp
0	0	0	0	0	1	1	0/1	Receiver Temp
0	0	0	0	1	0	0	0/1	Control Board A
0	0	0	0	1	0	1	0/1	Control Board B
0	0	0	0	1	1	0	0/1	Solar Panel 1 Temp
0	0	0	0	1	1	1	0/1	Solar Panel 2 Temp
0	0	0	1	0	0	0	0/1	Solar Panel 3 Temp
0	0	0	1	0	0	1	0/1	Solar Panel 4 Temp
0	0	0	1	0	1	0	0/1	Solar Panel 5 Temp
0	0	0	1	0	1	1	0/1	Solar Panel 6 Temp
0	0	0	1	1	0	0	0/1	Solar Panel 7 Temp
0	0	0	1	1	0	1	0/1	Solar Panel 8 Temp

TABLE 4.2B

TSS7	TSS6	TSS5	TSS4	TSS3	TSS2	TSS1	TSS0	SIGNAL DESCRIPTION
0	0	0	1	1	1	0	0/1	Solar Panel 9 Temp
0	0	0	1	1	1	1	0/1	Solar Panel 10 Temp
0	0	1	0	0	0	0	0/1	Solar Panel 11 Temp
0	0	1	0	0	0	1	0/1	Solar Panel 12 Temp
0	0	1	0	0	1	0	0/1	Solar Panel 13 Temp
0	0	1	0	0	1	1	0/1	Solar Panel 13 Temp
0	0	1	0	1	0	0	0/1	Solar Panel 15 Temp
0	0	1	0	1	0	1	0/1	Solar Panel 16 Temp
0	0	1	0	1	1	0	0/1	Solar Panel 17 Temp
0	0	1	0	1	1	1	0/1	Battery Volts (Bus)
0	0	1	1	0	0	0	0/1	Solar Panel I-V
0	0	1	1	0	0	1	0/1	Solar Panel 1 Volts
0	0	1	1	0	1	0	0/1	Solar Panel 2 Volts
0	0	1	1	0	1	1	0/1	Solar Panel 3 Volts
0	0	1	1	1	0	0	0/1	Solar Panel 4 Volts
0	0	1	1	1	0	1	0/1	Solar Panel 5 Volts
0	0	1	1	1	1	0	0/1	Solar Panel 6 Volts

TABLE 4.2C

TSS7	TSS6	TSS5	TSS4	TSS3	TSS2	TSS1	TSS0	SIGNAL DESCRIPTION
0	0	1	1	1	1	1	0/1	Solar Panel 7 Volts
0	1	0	0	0	0	0	0/1	Solar Panel 8 Volts
0	1	0	0	0	0	1	0/1	Solar Panel 9 Volts
0	1	0	0	0	1	0	0/1	Solar Panel 10 Volts
0	1	0	0	0	1	1	0/1	Solar Panel 1[illegible] Volts
0	1	0	0	1	0	0	0/1	Solar Panel 12 Volts
0	1	0	0	1	0	1	0/1	Solar Panel 13 Volts
0	1	0	0	1	1	0	0/1	Solar Panel 17 Volts
0	1	0	0	1	1	1	0/1	Solar Panel 15 Volts
0	1	0	1	0	0	0	0/1	Solar Panel 16 Volts
0	1	0	1	0	0	1	0/1	Solar Panel 17 Volts
0	1	0	1	0	1	0	0/1	Trans Sig Pwr Out
0	1	0	1	0	1	1	0/1	Received Signal Power
0	1	0	1	1	0	0	0/1	Control Brd A Power
0	1	0	1	1	0	1	0/1	Control Brd B Power
0	1	0	1	1	1	0	0/1	Transmitter Power Use
0	1	0	1	1	1	1	0/1	Receiver Power Use
0	1	1	0	0	0	1	0/1	Spare

CMOS devices were selected for use throughout the spacecraft because of their low power requirements and robustness. In all cases, Mil Standard devices are available for each of the devices.

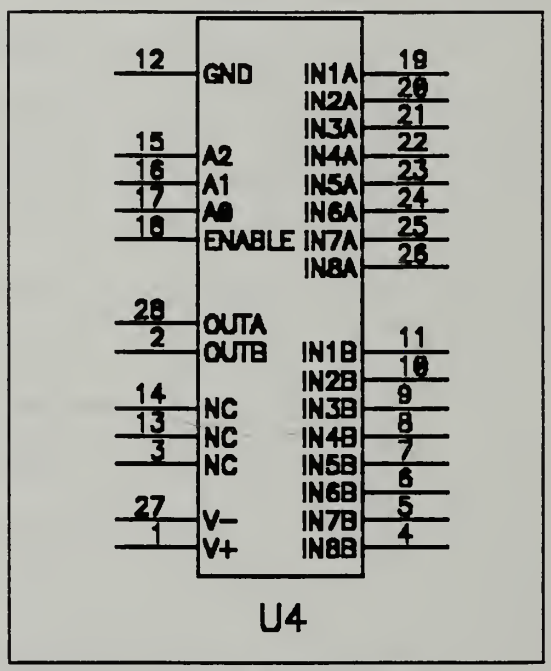


Figure 17 Analog Multiplexer

a. AD7507 Dual 8-Channel Analog Multiplexer

The Multiplexer selected for the Telemetry Section is the AD7507, shown in Figure 17. The basic characteristics of the device are listed below. The Analog Devices chip AD7507 has the following features which make it suitable for telemetry sampling in PANSAT: [Ref. 7:p.5-13]

1. V_{DD} = +15V
2. V_{SS} = -15V

3. High Temperature Range Device available

4. Low Power (10 mW typical)

The telemetry section requires a minimum of eleven multiplexers. This leads to a worst case power consumption, due to multiplexers, of 110 mW.

b. 82C55 Programmable Peripheral Interface, Telemetry Operations

The Programmable Peripheral Interface, the M82C55, developed by Intel was used to allow the 80C186 to operate the multiplexers and the Serial Communications Controllers (Chapter II discusses this device in detail in Section D.4). The Serial Communications Controllers are discussed in detail in the Communications Section Chapter (Chapter V).

(1)Initializing the PPI for Telemetry Operations. Peripheral to Microprocessor handshaking is simplified dramatically with this device. The multiplexers are controlled by writing a control word to Port A of the 82C55. On initial start-up, the μP initializes the PPI by writing a command word to it's control word port. The control word port is located at absolute I/O address location 0003H (This sets the PPI in Mode 0 which allows Ports A and C to be used as output/control lines). Port A is located at absolute I/O address location 0000H. Table 2.1, Chapter II lists the various addresses associated with the PPI.

(2)PPI-M80C186 Operational Description of a Data Collection. The sequence of events for a realignment of the current multiplexers is as follows:

1. The μP writes 00H to Port A (defined as 0000H I/O space). This will align the current source multiplexer to the Temperature Detecting Diode in the battery A temperature detection loop (The address of the battery temperature detector is given in Table 4.2A).

2. The μP waits for a timer interrupt before it reads the converted data. However, the actual signal from the TDD is aligned to the ICL 7115 by the same command in step 1. The data is not read until the End of Conversion signal is produced by the A/D converter.

3. The data is read a byte at a time into Port B of the PPI. The selection of a high or low byte is accomplished with Port A, Pin 0 (PA0), of the PPI producing the TS0 signal. When TS0 is low, the ICL7115 places the low byte of the converted signal on it's output. This low byte is read into the PPI at Port B. When the μP reads the low byte, it adds one to the value in Port A, thus aligning the high byte to Port B.

The actual conversion of data is accomplished with the Intercil A/D7115 14 bit, High Speed CMOS Analog to Digital Converter. The 7115 provides a highly accurate conversion when driven with a differential input. Each conversion requires 20 microseconds for a full 14-bit transformation.

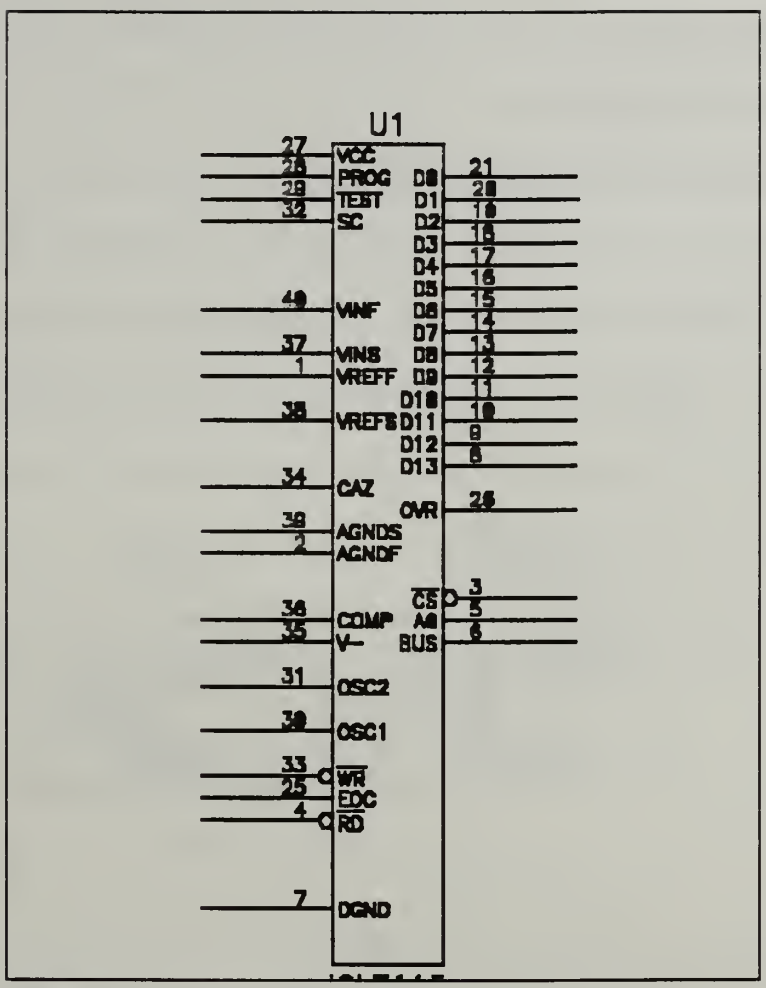


Figure 18 A/D Converter

c. ICL7115 14-bit High Speed CMOS, µP-Compatible A/D Converter

The Intercil ICL7115, shown in Figure 18, has the following characteristics which make it suitable for use with PANSAT: [Ref.8:p.6-66]

1. 14-Bit Resolution
2. $V_{cc} = \pm 5$ V

3. Byte-Organized
4. Buffered Outputs
5. Fast Conversion (40 μs)
6. Low Power Consumption (60 mW)

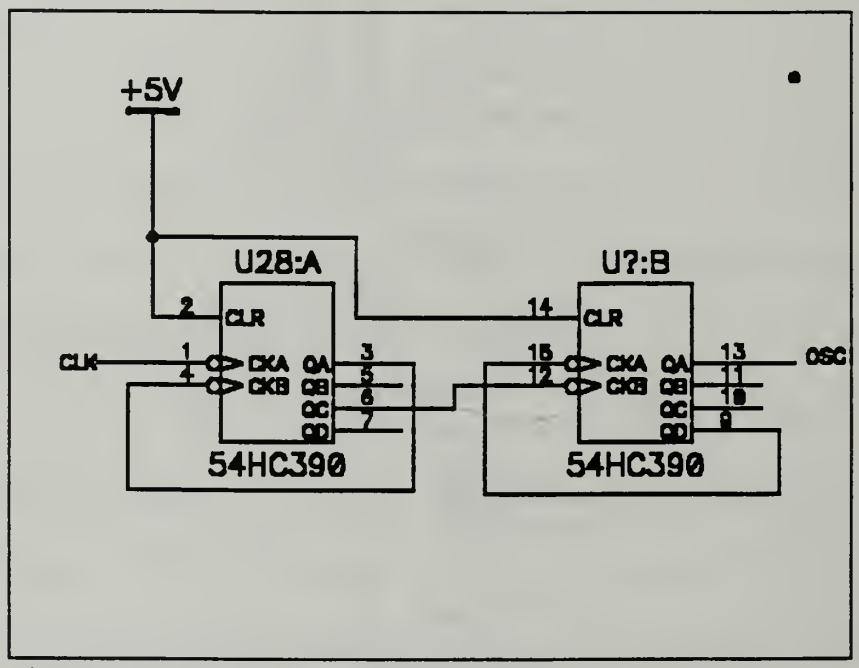


Figure 19 500 KHz Clock for ICL7115

The ICL7115 requires a clock speed of 500 KHz or less. To achieve this requirement the M80C186 clock out (CLKOUT) signal was divided by 20. This provides a clock frequency slightly less than 500 KHz and a signal conversion time of slightly greater than 20 μsec. The clock circuit in Figure 19 was selected to provide the required signal. [Ref. 2: p. 3-291]

Converted data is placed on D0-D7 with the BUS pin tied low. This allows the A0 line to toggle the high and low bytes out. The actual data is present on lines D0-

D13. However, port B of the PPI is connected with lines D0-D7 attached to pins PB0-PB7 and lines D8-D13 attached to pins PB0-PB5 respectively. PB6 is also tied to the OV (overflow) line. This allows the μP to check the overflow condition.

The actual conversion sequence is initiated by a "Write" pulse on the Write line. After the μP has aligned the current source and/or the signal to the ICL7115 and timed out, if necessary, it pulses this line and returns to other operations. The End of Conversion pin (EOC) on the ICL7115 is tied directly to the M80C186 via the "INT3" pin. This generates an interrupt with priority level three when the data conversion is complete. A delay of twenty microseconds is expected, based on a 500 KHz clock connected to the "OSC2" pin. The μP is then vectored to a telemetry collection subroutine located in memory.

4. Telemetry Sampling Time Calculation

At 500 KHz, the AD7115 requires approximately 20 μsec to complete a conversion cycle. This delay alone would normally be insignificant. However, the 23 TDD's require current to be provided for at least 20 milli-seconds. The calculations below take this into consideration in the determination of the total time required to sample all points. The switching times of the multiplexers are insignificant and therefore are neglected. Elapsed time for a complete telemetry cycle can be calculated as follows:

CWD = Current Warm-up Delay

ADCD= Analog to Digital Conversion Delay

TCT= Total Conversion Time

$$
\begin{aligned}
TCT &= 23 \times (CWD) + 48 \times (ADCD) \\
&= 23 \times (25 msec) + 48 \times (20 \mu sec) \\
&= 575.9 msec
\end{aligned}
$$

This is approximately one half of a second to perform a complete telemetry cycle. Although this is a large time allotment, this does not limit the design from operating in real time. Those signals which require constant monitoring, signals such as array voltage can be sampled at anytime. The sample rates for voltage monitoring is very flexible and had not been completely defined at the time of design completion.

5. Circuit Power Considerations

Telemetry must be collected and forwarded to the Master Ground Station. This section of the Control Board is large. However, it's power requirements are small. The use of CMOS devices coupled with minimizing the number of devices flown limits the total power consumption to a reasonable level. The calculations below do not account for the current source and the differential voltage circuitry. These are expected to be insignificant.

Power Requirement for Multiplexers = 110 mW [Ref.7: p.5-13]

Power Requirement for A/D Converter = 60 mW [Ref. 8: p. 6-66]

Total Power Requirement = 170 mW (typical)

These calculations are based on the worst case assumption that all the devices are active.

V. COMMUNICATIONS SECTION

A. GENERAL

The primary function of the satellite is to communicate with stations around the world. The digital control system must collect and store incoming traffic. If the final address for that traffic is the spacecraft, the microprocessor must interpret it. Any commands from the ground station must be translated to usable operational code and carried out. Any message not addressed specifically to the satellite must be stored until a ground station request it's traffic. In this case the microprocessor must interpret it's destination address and be ready to relay the message on to that station when it poles.

This design treats the modems as black boxes. The following general assumptions were made:

1. The microprocessor will become aware of incoming traffic when the first bit arrives at it's Serial Communications Controller (SCC).

2. The microprocessor will receive a bit stream in AX.25 protocol.

3. Transmission of data will be accomplished automatically when the microprocessor sends data to it's SCC for either one of the modems.

4. The modems will require no control lines from the microprocessor for the purpose of communications control (This design allows control line implementation with very little change).

5. The modem will require a clock from the microprocessor. This clock must be 152.4 KHz (This provides the modem with the necessary clock frequency to produce a signal at 1200 baud).

6. Transmitter power will be monitored and controlled via the power section of the control board.

7. Only one control board will control both modems at any given time. (Reset Circuitry discussion deals with modem control switching).

B. COMMUNICATIONS RESET CIRCUITRY

1. Design Requirements

a. General

The communications control section of PANSAT consists not only of the equipment necessary to communicate with ground stations, but also with the secondary microprocessor and it's board. The Secondary Control Board (SCB) must maintain some form of surveillance on the Primary Control Board (PCB) if it is going to effectively provide backup support in a timely fashion.

b. Secondary Control Board

The SCB monitors the power system whether it is in control of the spacecraft or not. It will not control the power system until it assumes control of the spacecraft. This is to ensure that one microprocessor does not try to drive the voltage up while the other attempts to take it low. Contention must be avoided.

If a problem occurs, the SCB must assume control of the spacecraft. It should take complete control quickly without threat of contention. This can be done through high speed switches on all critical control lines and with RS422 chip enable lines. The communications control section incorporates both into it's design.

A simple reset condition occurring on the PCB should not require the SCB to assume control. As discussed in Chapter III, the PCB will switch both system RAM and system ROM whenever it resets. This should correct the problem and allow the PCB to continue normal operations. If it does not, the SCB will assume control after a yet to be determined time delay. Initial discussions among the spacecraft design team include time delays as short as one minute to as long as five minutes.

c. Operational Status Register (OSR)

Inter-Control Board communications is accomplished via an octal latch register. This register is called the Operational Status Register (OSR). The PCB will, within a specified period of time, write to the OSR. The SCB monitors this register constantly. Whenever an update occurs, the spare re-initializes it's timing circuit and begins to wait again. If the specified time elapses without an update to this register, the SCB will assume complete control and notify the ground station at the earliest opportunity. The PCB will be unable to assume control again unless the ground station tells the spare board to transfer control back to the primary board.

C. IMPLEMENTATION

1. General

Throughout the design of the Digital Control System, the PCB and SCB were developed to be as similar as possible. In all previous sections of the control board design, the units were identical. However, in the Communications Section the two

boards differ slightly. The variations in the boards are illustrated in drawings thirteen and fourteen of Appendix A.

The OSR, shown in Figure 20, is implemented with the 82C55 Programmable Peripheral Interface controlling an MM54HC573 TRI-STATE Octal D-Type Latch. It is physically located on the SCB.

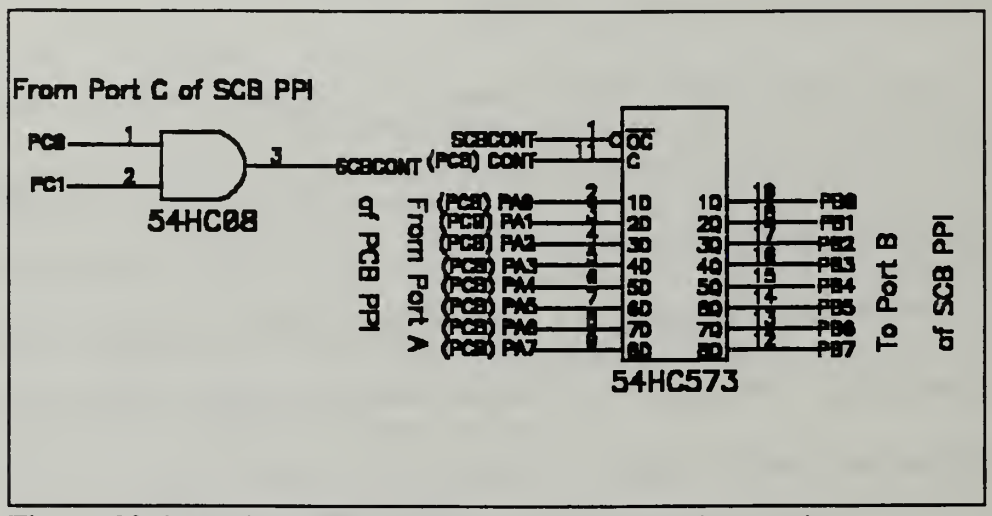


Figure 20 Operational Status Register with Supporting Logic

2. Operational Status Register Control Circuitry

a. MM54HC573 Tri-State Octal D-Type Latch (See Ch. 1.D.2)

The device is controlled by both microprocessors however, it is located exclusively on the SCB. The PCB controls the latch enable line and the SCB controls the output enable line. The truth table, Table 5.1 indicates the chip behavior for various combinations of signals. The SCB isolates itself from the PCB by taking the Output Control line high. This would only be necessary if the SCB assumes control of the

spacecraft. The output of the OSR is read via the SCB's Programmable Peripheral Interface Port B. The Primary Control Board drives the Latch Enable line via Port C of it's PPI and the combinational logic of lines PC0 and PC1, shown in Figure 20.

TABLE 5.1 TRUTH TABLE FOR OCTAL D-TYPE LATCH [Ref. 3: p. 3-320]

Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

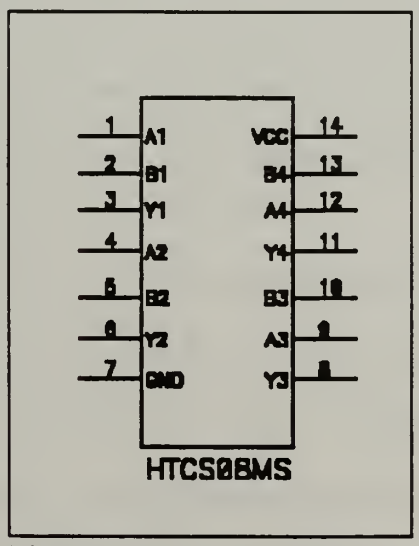


Figure 21 High Reliability AND Gate

b. HCTS08MS Quad 2-Input AND Gate [Ref. 4: p.12-16]

The Quad 2-Input AND Gate, radiation hardened device illustrated in Figure 21, was selected to implement this portion of the design. A highly reliable part will ensure that this critical section of the PCB does not fail. This chip is located on the SCB. It has the following characteristics which make it suitable for this task:

1. Propagation delay: 12 ns
2. V_{CC}= 4.5 - 5.5 Volts
3. Cosmic Ray upset immunity $2x10^{-9}$ errors/bit-day
4. Wide operating temperature: -55°C - +125°C

c. 82C55 Programmable Port Interface (See Ch. 1.D.4)

Port C of the PCB PPI is used for many peripherals. In order for the microprocessor to update the OSR, it has to write 03H into port C. The AND combination of PC0 and PC1 then enables the latch on the HC573 and the circuit will then latch and hold whatever is written to it.. The truth table for this combination is given in Table 5.2.

TABLE 5.2 OPERATIONAL STATUS REGISTER "AND" TRUTH TABLE

PC0	PC1	LATCH ENABLE
0	0	0
0	1	0
1	0	0
1	1	1

With the latch enabled, the PCB's microprocessor then writes a FFH followed by 00H into the register. The OSR is wired into Port A of the PCB and Port B of the SCB. The SCB then detects the writes and resets it's timers.

3. Transfer Control Circuitry

a. General

The Secondary Control Board assumes control whenever it times out. The command from the Master Ground Station to switch control from the PCB to SCB operates in the same manner. If the Ground Station desires the Secondary Control Board to assume control, it commands the PCB to stop writing to the OSR. This allows a simple, dependable design for the reset circuitry.

A clean transfer of spacecraft control from the Primary Control Board to the Secondary Control Board is a necessity. Clean is used here to mean quickly, without interruption of normal power system operations. The design of the communications control section of both the PCB and SCB ensures that when the SCB must assume control it is accomplished efficiently and cleanly.

b. Switching Control Lines

Control of the spacecraft is accomplished with a small number of control lines. The following lines have only one controlling source at any given time, but are switchable when necessary:

1. Pulse width modulated (PWM) signal to the voltage regulating circuit.
2. Clock input to the modems.
3. Communications lines from the modems.
4. Any control lines to experiments or to the modems if the need arises.

The design of the SCB section allows it to switch the lines to it's control. The PCB is designed to allow that to occur.

(1) Pulse Width Modulated Signal for Power System Control. Both the PCB and SCB monitor array and battery voltages at all times and both microprocessors generate a pulse width modulated signal to provide voltage regulation. However, the PCB is the normal source of this signal while the SCB simply writes it's signal to a high impedance. If the command to transfer control occurs, or the SCB must assume control because of a time out condition, then the SCB pulse width modulated signal will be multiplexed into the voltage control circuitry. Drawing 13 in Appendix A contains the details of the design.

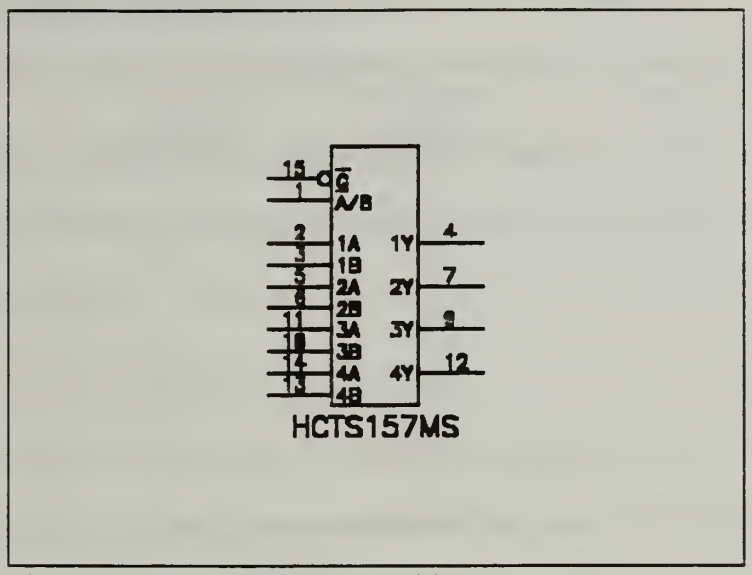


Figure 22 High Reliability Multiplexer

(2) HCTS157MS High-Reliability, Radiation Hardened, High-Speed, CMOS/SOS Quad 2-Input Multiplexer [Ref. 4: p. 12-81]. The HCTS157MS illustrated in Figure 22, was selected to provide the switching circuit for the PWM signal. The critical nature of this section of the circuit required a high reliability chip. This device was chosen for the following characteristics:

1. Propagation delay: 20 ns
2. V_{CC}= 4.5 - 5.5 Volts
3. Cosmic Ray upset immunity $2x10^{-9}$ errors/bit-day
4. Wide operating temperature: -55°C - +125°C

TABLE 5.3 TRUTH TABLE FOR HCTS157MS [Ref. 4: p. 12-81]

ENABLE	SELECT INPUT	DATA INPUTS	DATA INPUTS	OUT
E	S	I_0	I_1	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H=High voltage
L=Low voltage
X=Immaterial

The output enable line (E), which is connected to pin 15 in Figure 22, is tied low to ensure that this chip is always on line. The select input line (S), which is connected to pin one in Figure 22, is driven by the SCB. I_0 is the input from the SCB and the select lines are pulled up by resistors connected to a power source. Although pull up resistors waste power, they are necessary for a dependable system. This ensures that the only way the SCB can assume control of voltage regulation is by driving the select line low. In the normal operating mode, the I_1 line from the PCB is active.

Experiments which require control lines from the microprocessor will pass through an HCTS157MS. The multiplexer is configured identically to the one illustrated in Figure 22 and the select line is pulled up. The SCB is required to actively drive this line low to assume control of the experiment. The high reliability of this

device was one of the primary selection criteria because of the strong desire to prevent accidental control transfer or prevention of transfer.

c. External Communications Control Implemented with RS422

All lines associated with the external communications pass through the RS422 transmitters and receivers. The selection of which device is on line is carried out by the SCB. In the normal configuration, the PCB will be receiving and transmitting traffic. If a board transfer occurs, the SCB will disable the PCB transmitters and receivers and enable it's own. Figure 23 shows the circuit diagram for this section of the PCB. The transmitters and receivers for the PCB are located on the PCB and their control lines are driven by the SCB via it's Programmable Peripheral Port.

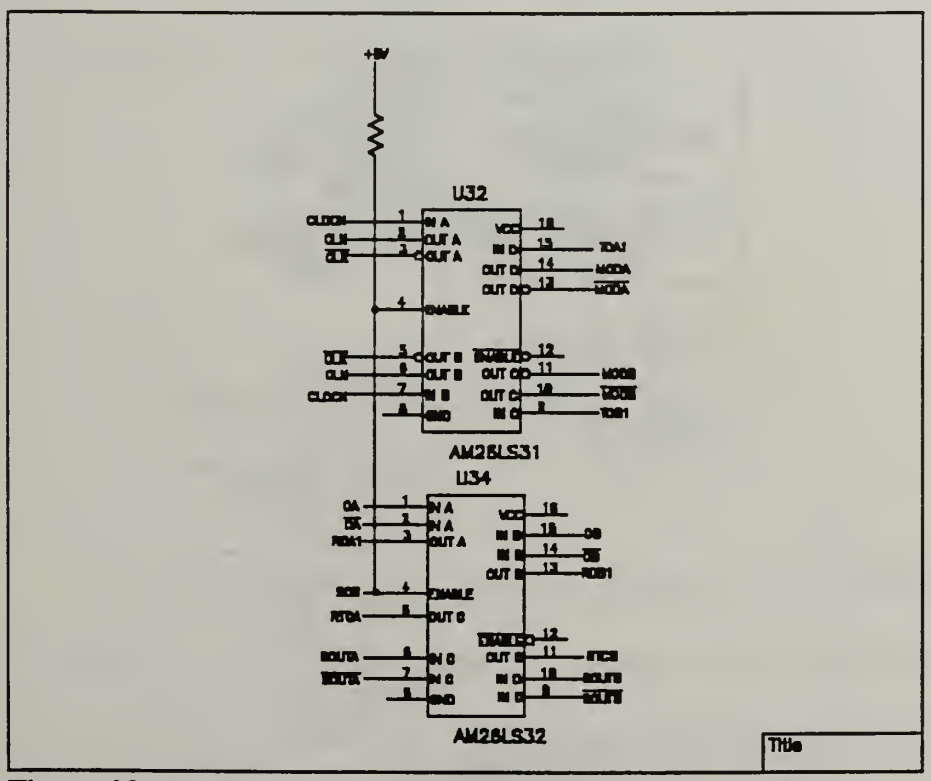


Figure 23 Communications. Control for PCB

A modem control board (MCB) had to be designed. This board is shown in Figure 24 and is also located in Appendix A. The MCB is controlled by the SCB via RS422 protocol. The SCB control signals are sent via line drivers and receivers. This section of the system aligns the data path to the SCB or PCB. By design, the normal data path will be via the PCB.

The lines which are implemented in this manner are the data lines and the clock signal line. The clock signal is used by the modem to control synchronization with signals from the earth. The data is transmitted using AX.25 protocol while it is passed to the control board via devices using RS422 protocol.

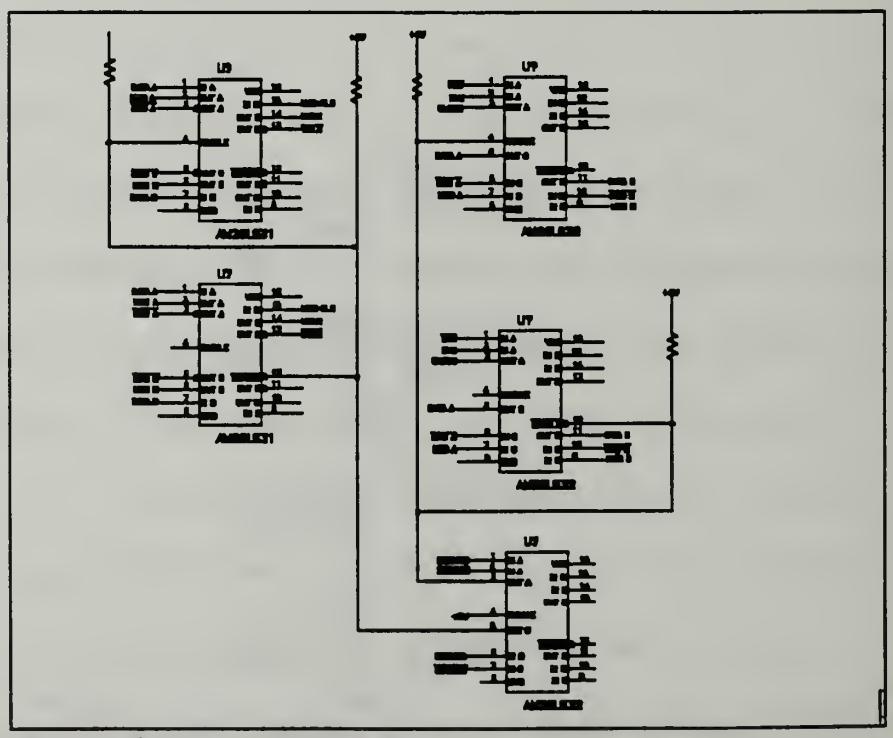


Figure 24 Modem Control Board

RS422 was selected because it has an excellent immunity to noise. Noise is high in the satellite environment due to the proximity of the control board to the transmitter. This protocol uses a twisted pair differential connection. This type of connection has excellent common mode rejection characteristics. The Am26LS31 Line Drivers and Am26LS32 Receivers are used for the RS-422 protocol generation.

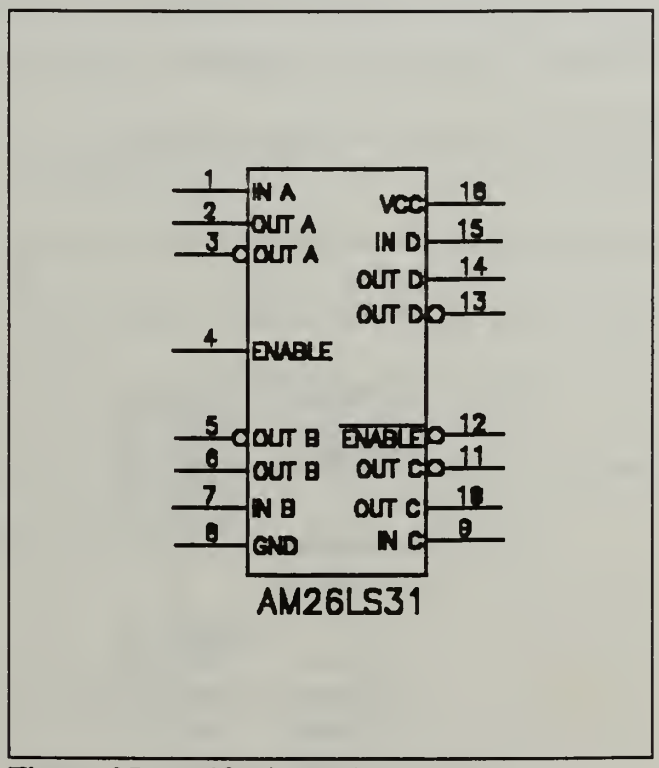


Figure 25 RS422 Line Driver

(1) AM26LS31 Quad High-Speed Differential Line Driver. The Am26LS31, [Ref. 9: p. 4-28] shown in Figure 25, possesses the capabilities necessary to operate in the PANSAT environment. This device was selected for the following reasons:

1. Output skew 2.0 ns typical
2. Input to output delay - 12 ns
3. Operation from a single +5V supply
4. Four line drivers in one package for maximum package density
5. Common enable disable line

This Advanced Micro Device Chip is available in military specifications. For initial implementation of the design, the commercial version is used.

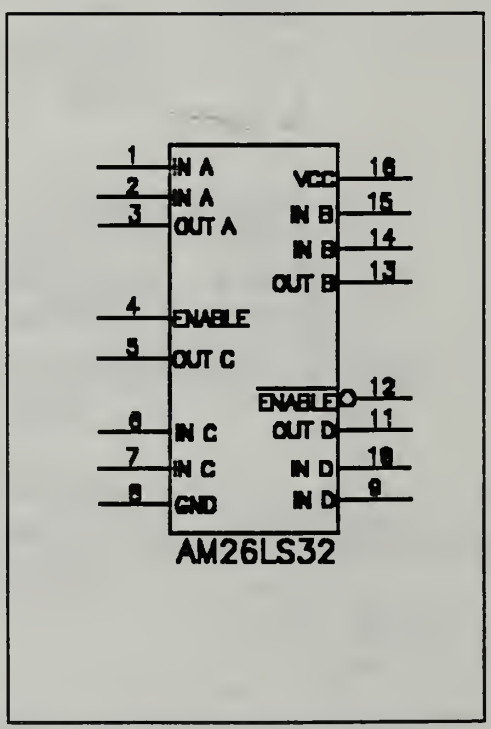


Figure 26 RS422 Line Receiver

(2) AM26LS32 Quad Differential Line Receiver. The Am26LS32 is a Quad Differential Line Receiver and is shown in Figure 26 [Ref. 9: p. 4-39]. It was selected because it is compatible with the Am26LS31 and has excellent sensitivity.

Assumption of control by the SCB will be implemented as discussed above. All transfer control is accomplished by the SCB, but only after it detects no activity in the OSR for a specified period of time. This delay will either be generated by command from the master ground station to the PCB or by the PCB's failure to update the OSR.

D. AM85C30 SERIAL COMMUNICATIONS CONTROLLER (SCC)

1. General

The communications subsection uses an SCC to maintain contact with Modems A and B. The Am85C30 is a sophisticated communications device capable of being programmed to use various code protocols and transmission techniques. The technical manual for this device alone is several chapters in length. A general presentation of the more critical points concerning PANSAT is given below. [Ref. 10: p. (ALL)] This SCC was selected for the following reasons:

1. Compatible with M80C186 microprocessor.
2. Low power requirements (uses CMOS technology)
3. Has two independent full duplex channels
4. Supports synchronous or asynchronous data transfers
5. Can be used with DMA
6. Internal Synchronization
7. Has facilities for modem control in both channels (not required for present design, but can be implemented easily in later upgrades)

8. Available in Military Specifications (not used in initial implementation)

The Am85C30 logical design is compatible with the requirements of PANSAT in that it provides a flexible interface between the M80C186 and the Modem. It's functional layout is shown in Figure 27. The implementation of the device in the communications subsection of the PCB is shown in the schematic in drawing 12, Appendix A. The SCC is programmed to receive AX.25 protocol and will use Cyclic Redundancy Coding (CRC) for error detection and correction.

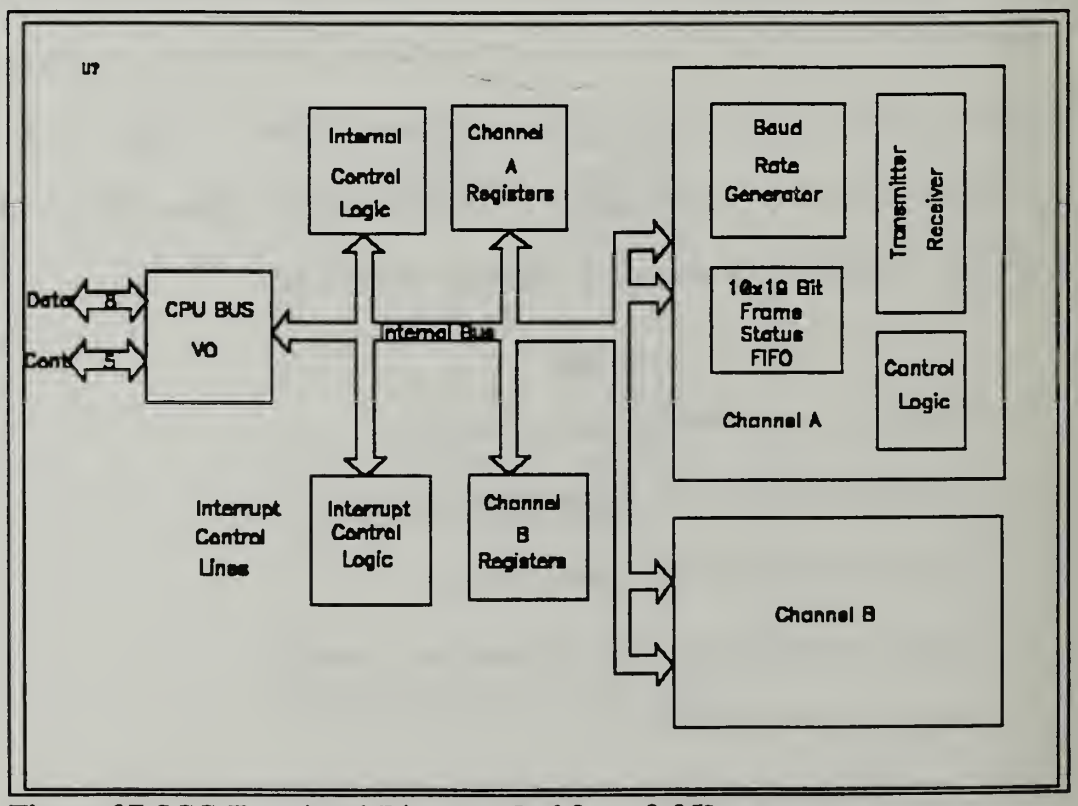


Figure 27 SCC Functional Diagram [Ref.8: p. 2-35]

2. Programming the Am85C30 SCC

Programming of the Am85C30 is performed during the initialization of the control board. When the M80C186 resets, it programs the SCC. Read only memory (ROM) contains the required programming data for the 80C186 to correctly setup the device. The SCC can operate in one of three modes. Each of these modes can be programmed at any time during operations. This allows some flexibility if coding should change after design completion.

The SCC must be enabled before the actual programming can begin. To enable the SCC, the M80C186 writes to Port C of the PPI. The control word for the SCC activation is listed in Table 2.2 of Chapter II. Once 80H is written into Port C, the 85C30 is ready to be programmed.

All programming of the SCC is accomplished via a two step process of writing to Write Register 0 (WR0) of the 85C30. WR0 is shared by both communications channels of the SCC. To access a particular register, the pointer bits of WR0 are set. To address WR0, the microprocessor must address the SCC. The SCC addresses are located in I/O Space at the locations listed in Table 5.4.

The sequence of steps required to write to an SCC register follows:

1. Write control word to Port C of the PPI (80H selects the SCC)
2. Write the address of the function desired (This address is latched, the latched values will drive pins A/~B, D/~C)
3. Write pointers into WR0 (see Table 5.4)
4. Write command or data

TABLE 5.4 SCC FUNCTIONAL ADDRESSES

A8	A7	A6	A5	A4	A3	A2	A1	Register Addressed
0	0	0	0	0	0	0	0	Ch B Command Trans
0	0	0	0	0	0	0	1	Ch B Data Trans
0	0	0	0	0	0	1	0	Ch A Command Trans
0	0	0	0	0	0	1	1	Ch A Data Trans

After the pointer bits are set, the next read or write will be to the desired register. Table 5.5A and 5.5B lists and describes each register of the SCC. Table 5.6A and Table 5.6 B indicate the address for the various registers.

TABLE 5.5A REGISTER SET [Ref. 10: p.2-4]

	Read Register Functions
RR0	Transmit/Receive buffer status, and External status
RR1	Special Receive Condition Status, residue codes, error conditions
RR2	Modified (Channel B only) interrupt vector and Unmodified interrupt vector (Channel A only)
RR3	Interrupt Pending bits (Channel A only)
*RR6	14-bit frame byte count (LSB)
*RR7	14-bit frame byte count (MSB), frame status
RR8	Receive buffer
RR10	Miscellaneous XMTR, RCVR status parameters
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR15	External/Status interrupt control information

TABLE 5.5B REGISTER SET [Ref. 10: p.2-4]

	Write Register Functions
WR0	Command Register (Register Pointers), CRC initialization, resets for various modes
WR1	Interrupt conditions. Wait/DMA request control
WR2	Interrupt vector (access through either channel)
WR3	Receive/Control parameters, number of bits per character, Rx CRC enable
WR4	Transmit/Receive miscellaneous parameters and codes, clock rate, number of sync character, stop bits, parity
WR5	Transmit parameters and control, number of Tx bits per character, Tx CRC enable
WR6	SYNC character (1st byte) of SDLC address
WR7	SYNC character (2nd byte) or SDLC flag
WR8	Transmit Buffer
WR9	Master interrupt control and reset (accessed through either channel), reset bits, control interrupt daisy chain
WR10	Miscellaneous transmitter/receiver control bits, NRZI, NRZ, FM encoding , CRC reset
WR11	Clock mode control, source of Rx and Tx clocks
WR12	Lower byte of baud rate generator time constant
WR13	Upper byte of baud rate generator time constant
WR14	Miscellaneous control bits: baud rate generator, Phase-Locked Loop control, auto echo, local loopback
WR15	External/Status interrupt control information-control external conditions causing interrupts

TABLE 5.6A SCC REGISTER MAP [Ref. 10: p.2-8]

A/B	PNT_2	PNT_1	PNT_0	WRITE	READ
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	(RR0B)
0	1	0	1	WR5B	(RR1B)
0	1	1	0	WR6B	(RR2B)
0	1	1	1	WR7B	(RR3B)
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2A	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR3A	(RR0A)
1	1	0	1	WR5A	(RR1A)
1	1	1	0	WR6A	(RR2A)
1	1	1	1	WR7A	(RR3A)

Note: The remaining Register Map is with the Point High Command active [D5-3 (WR0) = 001]

TABLE 5.6B SCC REGISTER MAP [Ref. 10: p. 2-8]

A/B	PNT_2	PNT_1	PNT_0	WRITE	READ
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	(RR13B)
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	(RR15B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	(RR10B)
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	(RR13A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	(RR15A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	(RR10A)
1	1	1	1	WR15A	RR15A

3. Operating Modes of the Am85C30

The Am85C30 SCC operates in one of three modes, polling, interrupt or block transfer. The microprocessor can program the SCC at any time to operate in one of these modes. When the SCC is in the polling mode, the microprocessor can determine if data has been written to or from the device by checking the status of various registers. The interrupt mode allows the SCC to request service from the M80C186

when data is present. The M80C186 executes an interrupt handling subroutine that stores the incoming data into a specified memory location. Actual data transfer is accomplished using Direct Memory Access (DMA). The SCC is provided with up to three sources of interrupt per channel with each type of interrupt generating a unique vector address in Read Register 2 (RR2).

a. Receive Interrupt Mode [Ref. 10: p.3-10]

The Receive Interrupt mode is used in the design of the PANSAT control boards. The SCC has four sub-modes under the Receive Interrupt mode. These modes are:

1. Receive Interrupts Disabled
2. Interrupt on First Character or Special Condition
3. Interrupt on All Received Characters or Special Condition
4. Receive interrupt on Special Condition Only

This design implements "Interrupt on First Character or Special Condition," which allows the microprocessor to start the reception of a message and then continue with other operations. The microprocessor passes control for message reception and storage to it's DMA Controller (DMAC). Since the transfer of data from earth stations is at 1200 baud, the microprocessor would be very inefficiently used if it were required to wait for the complete transmission of a packet.

b. Programming for Receive Interrupt Mode Operations

To program the SCC to operate in this mode the 80C186 must write to various internal control registers. This is accomplished in the following sequence:

1. Master Interrupt Enable (MIE) bit set. This is accomplished by writing '1' to D3 of WR9. [Ref. 10: p. 3-3] WR9 is accessed by first writing 0010001B to WR0, this will issue the point high command and set the pointers to WR9. [Ref. 10: p.6-7]

2. Interrupt Enable Bits (IE) are written by the processor. The serial communications controller IE bits are located in WR1 which is illustrated in Figure 28. [Ref. 10: p. 6-8] WR1 is accessed by first writing to the pointers in WR0. In this case, writing to WR1A would require 1001B be entered into the D0-D3 of WR0.

D7	D6	D5	D4	D3	D2	D1	D0
W/DMA REQ Enable	W/DMA REQ Funct.	W/DMA REQ on Rx/Tx			Parity INT Enable	Tx INT Enable	Ext/Sta INT Enable

0	0	-Rx INT Disable on 1st
0	1	-Rx INT on 1st Char or Special Condition
1	0	-INT on All Rx Char. or Special Condition
1	1	-Rx INT on Special Only

Figure 28 WR1-- Interrupt Source IE [Ref 10: p. 3-5]

After processing an interrupt, the microprocessor issues a RESET HIGHEST Interrupt Under Service (IUS) command. It does this via WR0 to re-enable lower

priority interrupts. IUS bits are set whenever an interrupt is received. These bits are not readable by the microprocessor.

c. Operational Description of Receive Interrupt Mode

Interrupt vectors are placed into RR2. D1 of WR9 determines whether a vector will be placed into RR2. When this bit is 0, the vector is placed in the register. In this design, WR9 will have D1 set to 0. When an SCC interrupt occurs, it will drive INT1 of the M80C186 low. This will cause the microprocessor to jump to an SCC interrupt handling routine. The interrupt handling routine will read the vector located in RR2A or RR2B. RR2B will contain the status of interrupts. This vector is accessed via WR0. The vectors generated by the various interrupts are listed in Table 5.8.

TABLE 5.8 INTERRUPT VECTORS WITH MODIFICATION [Ref. 10: p. 6-19]

V3	V2	V1	Status High/Status Low=0
V4	V5	V6	Status High/Status Low=1
0	0	0	Ch B Transmit Buffer Empty
0	0	1	Ch B External/Status Change
0	1	0	Ch B Receive Character Available
0	1	1	Ch B Special Receive Condition
1	0	0	Ch A Transmit Buffer Empty
1	0	1	Ch A External/Status Change
1	1	0	Ch A Receive Character Available
1	1	1	Ch A Special Receive Condition

The PANSAT SCC will then set D0 of WR9 to zero. This causes the interrupt vector to include the status bits. The status bits indicate the highest interrupt being processed [Ref 8: p.6-19] (WR2, the interrupt vector register will be initialized to zero). This allows the microprocessor to determine exactly which interrupt occurred in-spite of only one interrupt line from the SCC. The vector is placed into bits D1-D3 of WR9 while the Status High bit, bit 4 of WR9, is set low. WR9 is critical to interrupt operations and is shown in Figure 29.

D7	D6	D5	D4	D3	D2	D1	D0
		Inter. Mask without INTACK	Stat High/ Status Low	Master Inter. Enable	DLC	No Vector	Vector Include Status

0	0	No Reset
0	1	Channel Reset B
1	0	Channel Reset A
1	1	Force Hardware Reset

Figure 29 Write Register 9 [Ref.10: p.6-18]

WR9 will typically be loaded with 00100X01B. This allows interrupts to occur and it allows masking of lower priority interrupts. The status of the interrupt is placed in the least significant bits of the data register (RR2).

d. Direct Memory Access for Communications Use

Transmission of signals will be accomplished by using DMA. This allows the microprocessor to begin the transmission of a message and return to housekeeping operations. In this mode, there is no requirement for a transmission interrupt. When the ground station requests a message, the microprocessor will initialize the DMAC to transfer the data to the SCC for transmission. Polling is used to determine when the message transmission is completed.

VI. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

The Petite Amateur Navy Satellite's success depends on many things, not the least of which is the Digital Control System. This system is designed to provide dependable communications service for the life of the satellite. At present, the lifetime of the spacecraft is estimated to be approximately two years after it's launch date. Two years in the harsh environment of space will have a negative effect on any electronic equipment carried aboard PANSAT.

Concern for providing a design capable of absorbing some equipment failure without loss of capability lead to a major change in design philosophy in October of 1992. The new philosophy was to provide an increase in redundancy, while maintaining a reasonably low budget. A preliminary design for the digital control system had been completed prior to this decision, but it was developed without concern for single point failures. Single point failures and single event upsets were of foremost concern as this design developed. Redundancy was designed into the system, but budget constraints and development time limited the level which could be incorporated. The use of a Primary Control Board constantly monitored by a Secondary Control Board seemed to be a workable compromise between a fully protected, redundant system and the initial design of the Digital Control System.

The M80C186 is an excellent control device. It's high tolerance of ionizing radiation should ensure it's lifetime will be greater than other critical sections of the spacecraft. Several versions operating at various clock frequencies are available in the marketplace. This will provide some flexibility for future revisions to the design. Although the M80C186 is not the best or fastest microprocessor available today, it is an excellent choice for PANSAT. The PANSAT design team already possesses the development tools for this device and several of the team members have experience implementing it in spacecraft control systems.

Critical sections, such as the reset circuitry and the Operational Status Register are implemented with CMOS silicon on sapphire (SOS) devices. These devices are far less susceptible to single event upsets or the permanent damage associated with ionizing radiation.

CMOS technology was used throughout the design because of it's tolerance for radiation and it's low power requirements. PANSAT has a very small power budget, one which is further restricted by the need to have a relatively powerful transmitter in the spacecraft. CMOS devices minimize the power requirements of the digital control system freeing up more power for the communications section of the vehicle. Power consumption of the Memory Section and the Telemetry Section were computed. These sections are expected to have the highest energy requirements. Together their total power consumption is expected to be approximately 380 milliwatts. If we assume the rest of the digital control system will use as much power, a very conservative estimate, the PCB and the SCB combined require less than two watts of power (the Secondary

Control Board is expected to consume the same quantity of energy as the Primary Control Board).

B. RECOMMENDATIONS

PANSAT is a light, relatively inexpensive satellite. If it proves to be a viable system, demand can be expected to go up for more satellites. It is conceivable, that a constellation of these satellites will exist one day. With this in mind, the design team needs to consider other possible uses for PANSAT now. From a Digital Control Systems perspective, this means a more capable system should be designed. A system which incorporates more redundancy and a faster microprocessor must be considered for the next generation of PANSAT.

The M80C186 is a capable computing engine, however there are several options available today which should be considered for later PANSAT designs. A Reduced Instruction Set Computer (RISC) should be considered for any follow on PANSAT projects. With a RISC device, more tasking can be loaded onto the system, while still maintaining real time control of the power and communications systems.

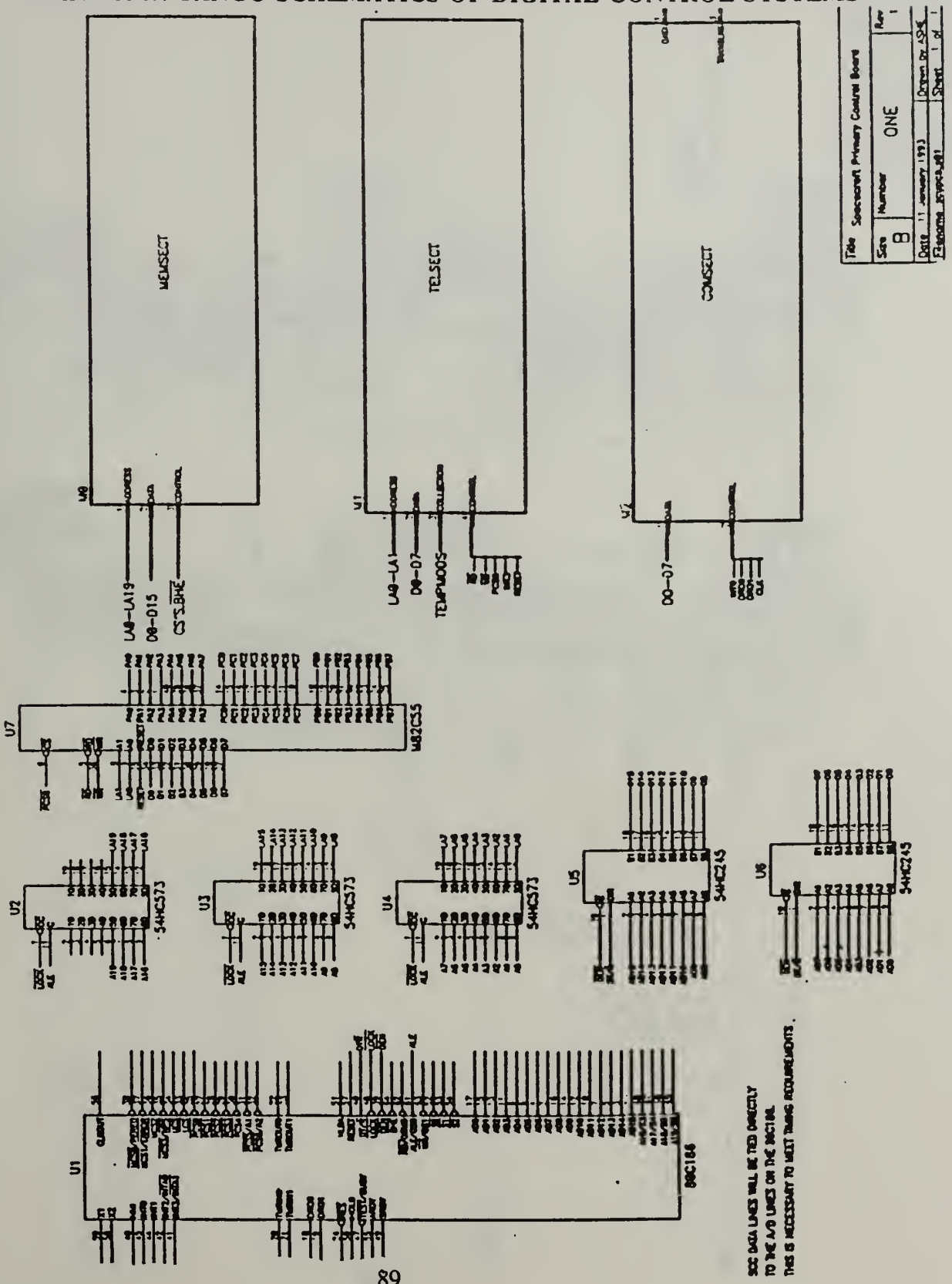
Naval Postgraduate students interested in VLSI design and implementation should be challenged with developing specialized chips. Chips which will decrease the overall size of a control board and lower the net power requirements of the Digital Control System. This will free up space and provide an increased margin in the power budget.

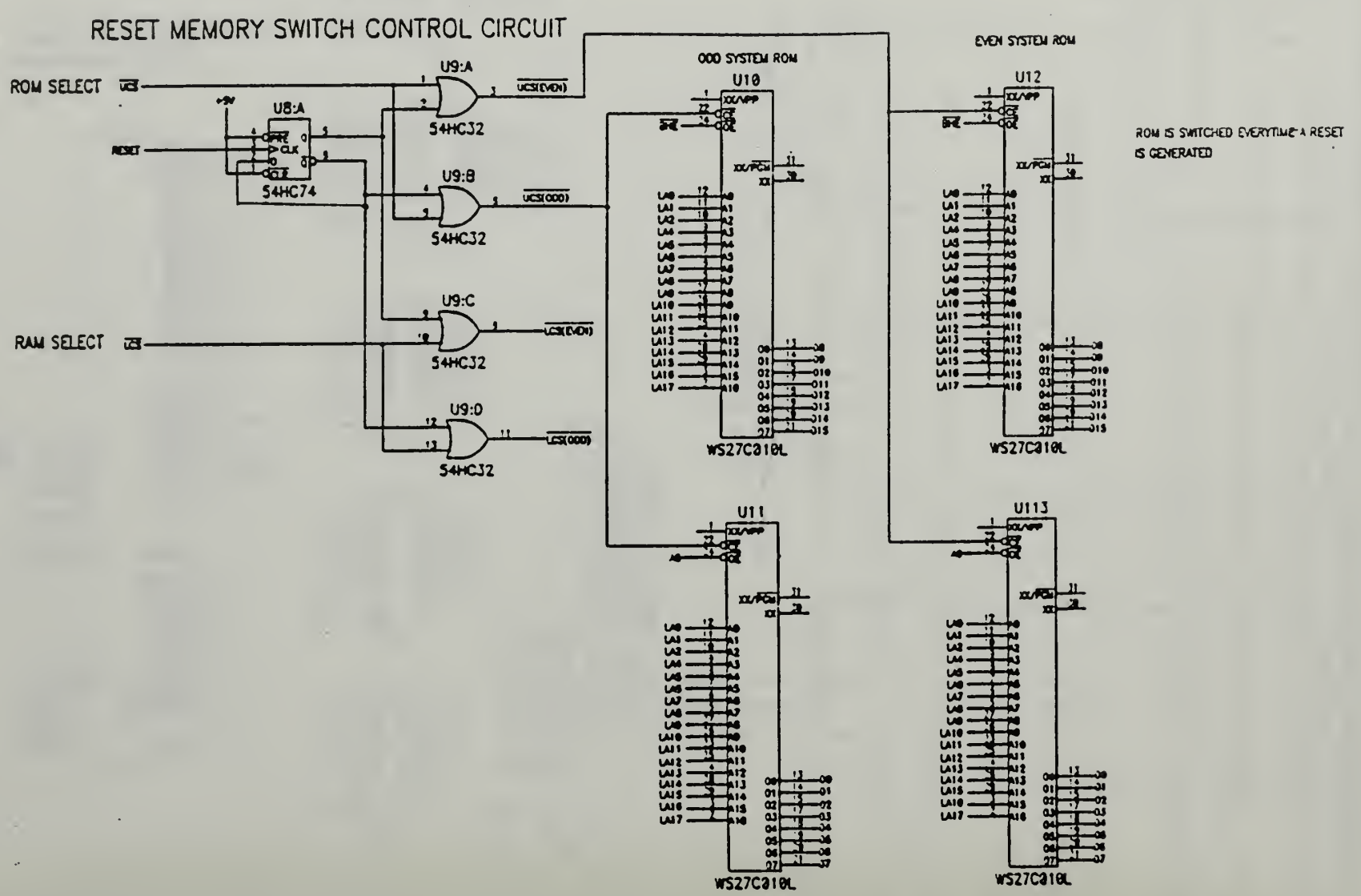
A commercially available operating system (OS) should be used for the Digital Control System. One which has been proven in other spacecraft. There are several

operating systems available, however, the design team should only get one which has source code documentation. This will allow NPS personnel to customize or modify the code. The selected OS should also provide an AX.25 protocol interpreter. This will allow the design team to concentrate their efforts on those mission requirements which are unique to PANSAT.

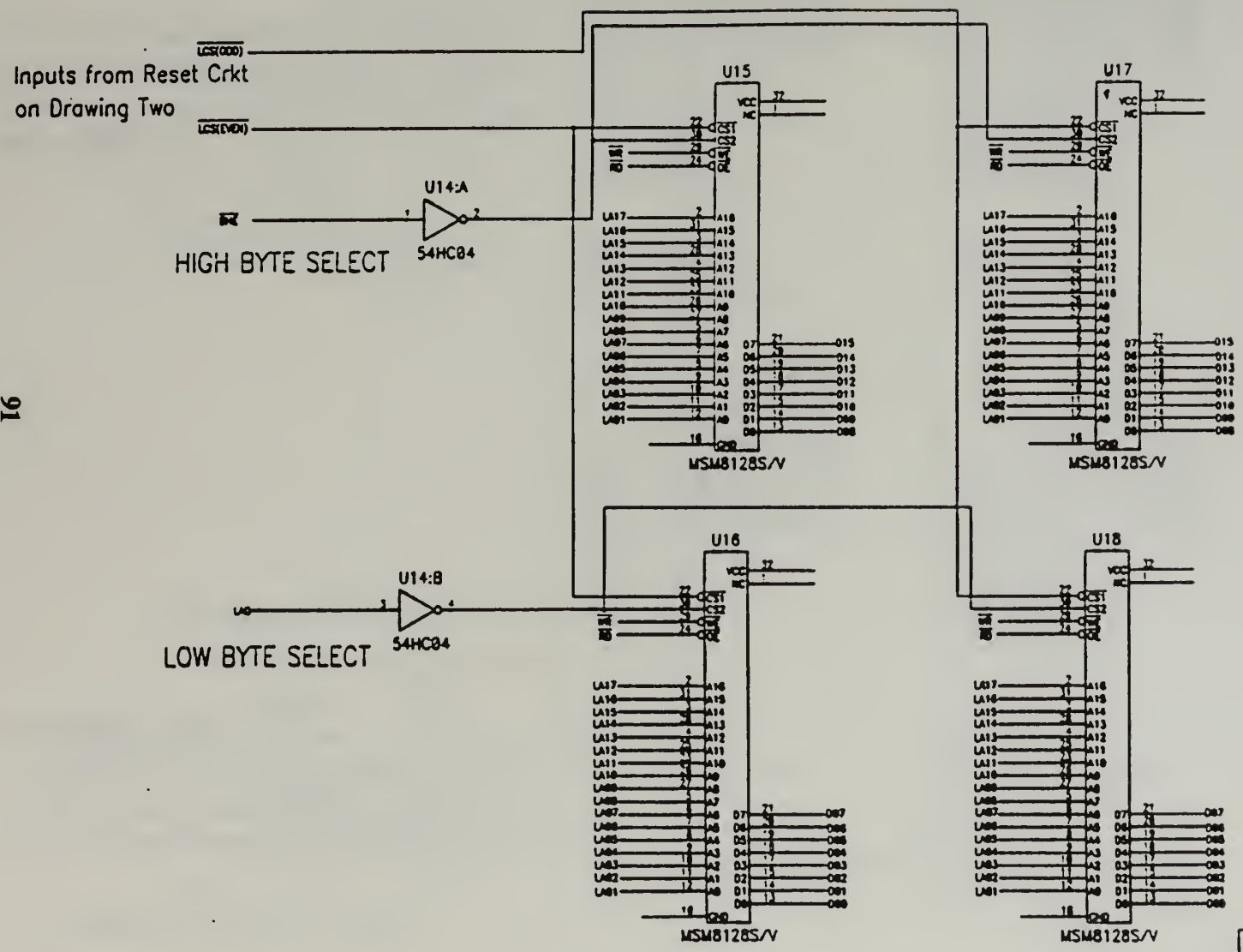
Data transmission rates are a concern. Access time to the satellite will be limited to less than 10 minutes per session. It is strongly recommended that the group responsible for actual communications between the spacecraft and the ground stations use the highest transmission rate possible for the given bandwidth. Faster baud rates will allow more complex software modifications to be uploaded after the launch, thus allowing greater freedom to experiment with the OS.

APPENDIX A: TANGO SCHEMATICS OF DIGITAL CONTROL SYSTEMS



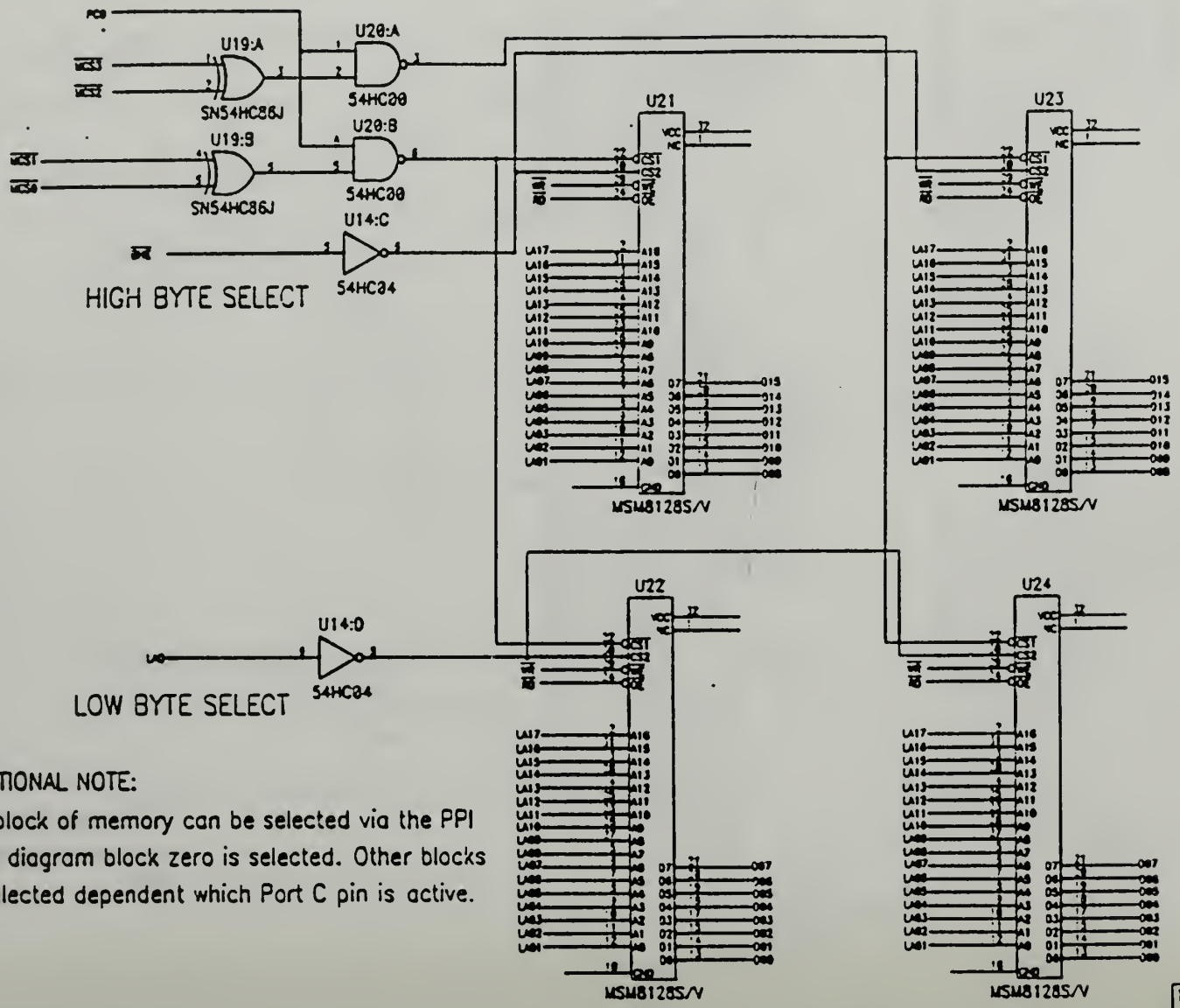


Title	SYSTEM ROM WITH RESET CRKT	
Size D	Number TWO	Rev 2



Title: System RAM		
Size: B	Number: THREE	Rev: 2
Date: 11 January 1993	Drawn by: ASHE	
Filename: mrsms.sch1	Sheet 1 of 1	

MEMORY BLOCK SELECT CRKT

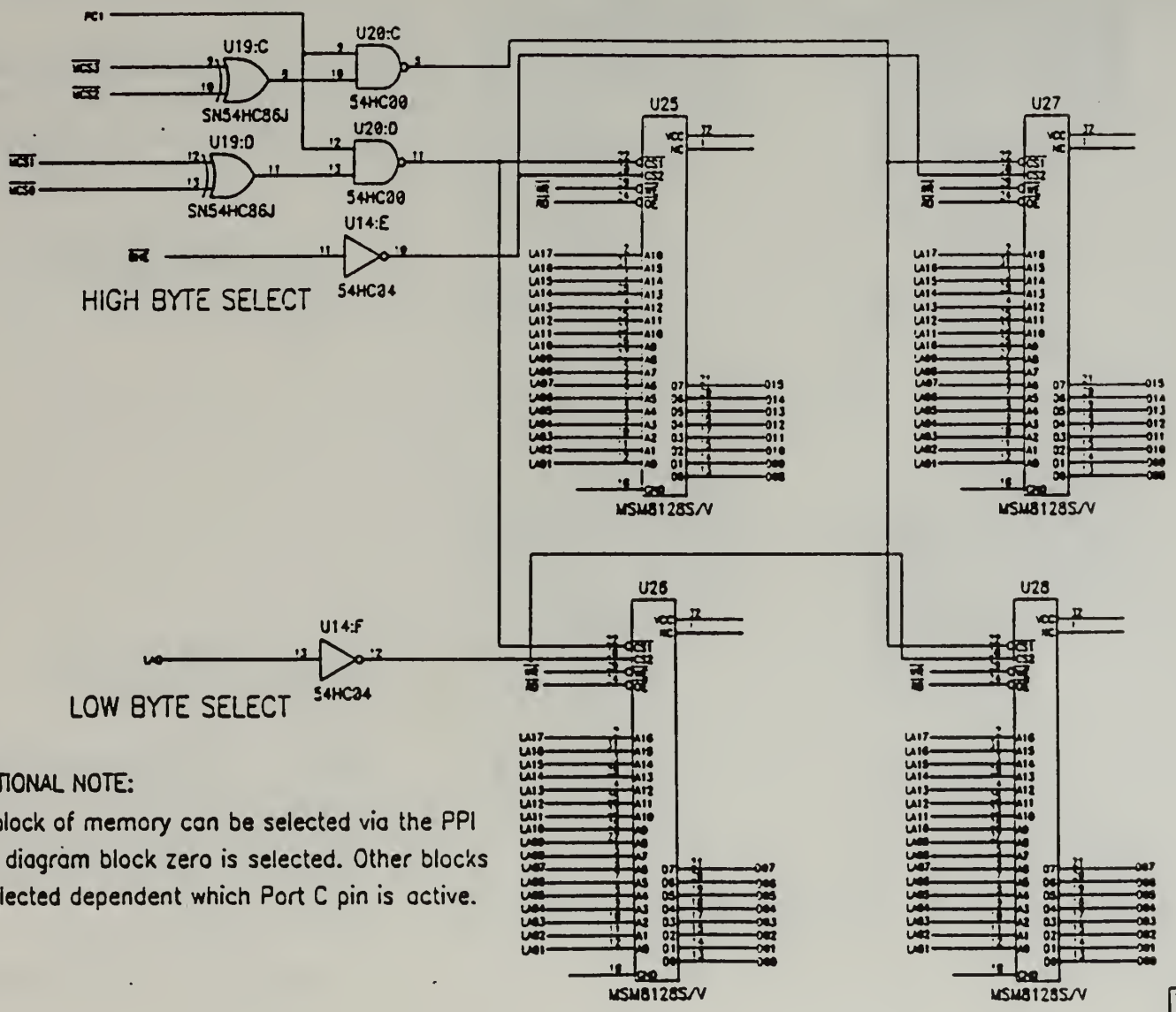


OPERATIONAL NOTE:

Each block of memory can be selected via the PPI In this diagram block zero is selected. Other blocks are selected dependent which Port C pin is active.

Title	MIDDLE RAM BLOCK 0	
Size: B	Number: FOUR	Rev: 0
Date: 24 November 1992	Drawn by: ASK	
Filename: MDRAM0.SCH	Sheet 1 of 1	

MEMORY BLOCK SELECT CRKT

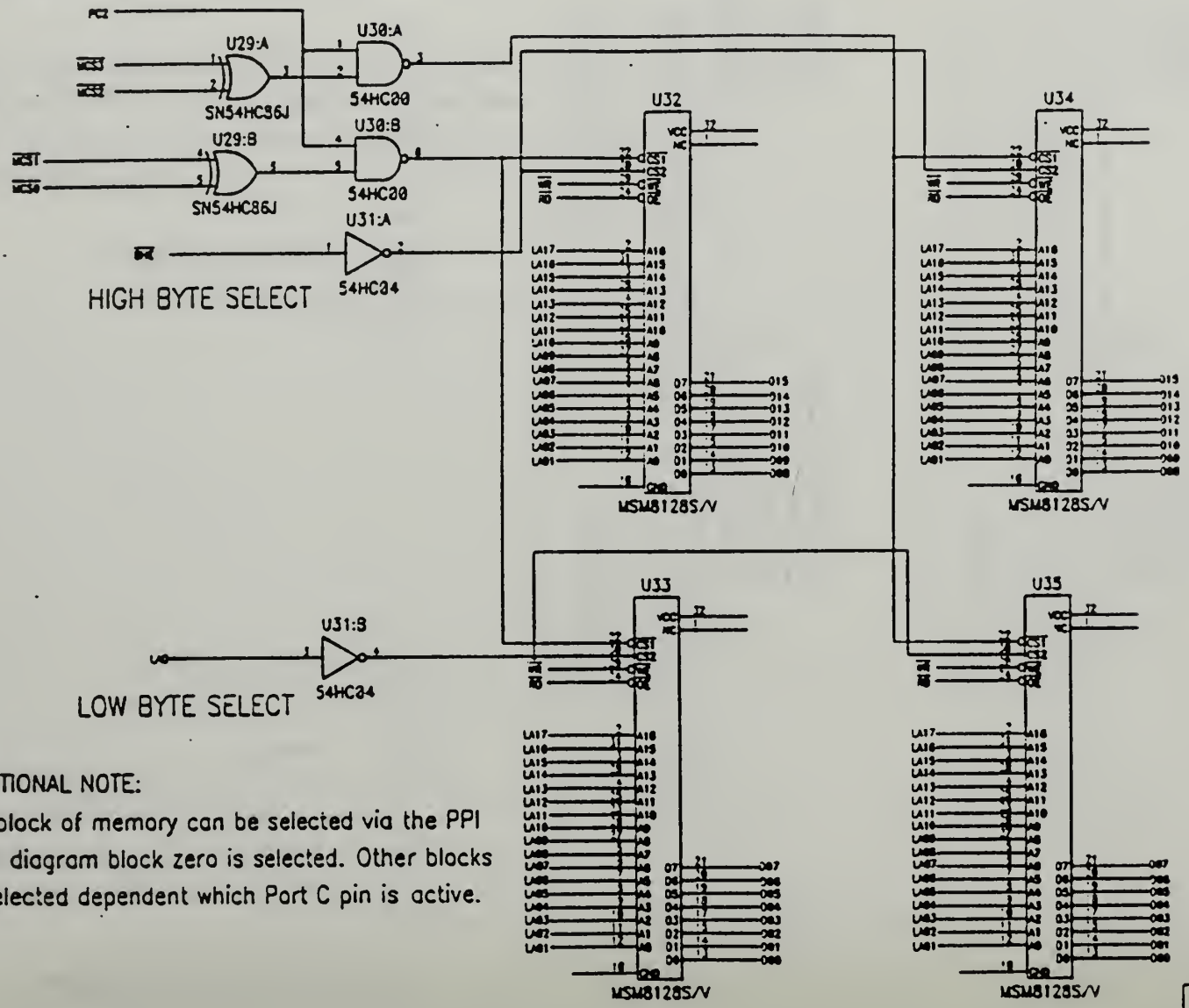


OPERATIONAL NOTE:

Each block of memory can be selected via the PPI In this diagram block zero is selected. Other blocks are selected dependent which Port C pin is active.

Title: MIDDLE RAM BLOCK 1		
Size: B	Number: FIVE	Rev: 0
Date: 11 January 1993	Drawn by:	
Filename: MDRAM1.SCH	Sheet 1 of 1	

MEMORY BLOCK SELECT CRKT

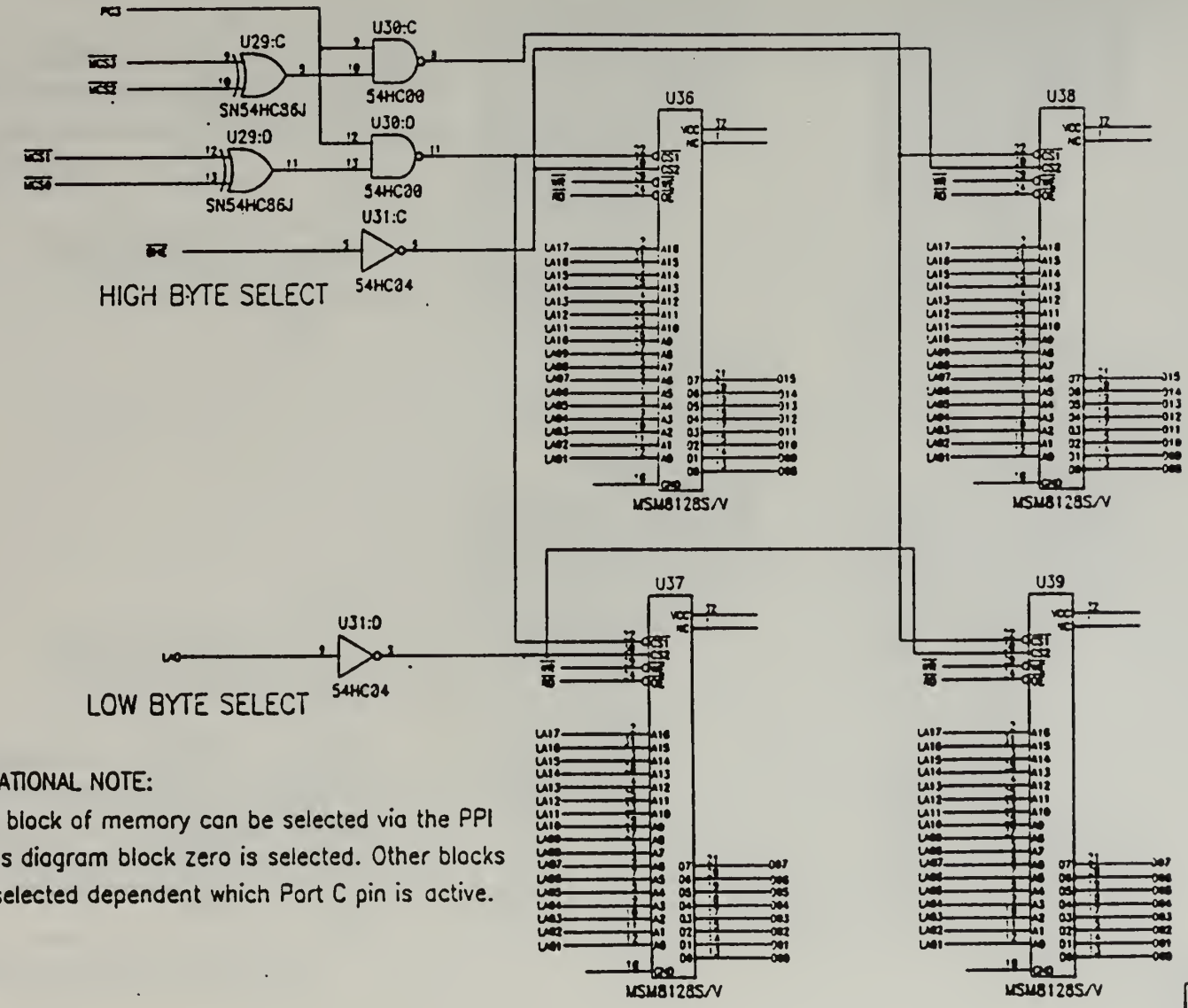


OPERATIONAL NOTE:

Each block of memory can be selected via the PPI In this diagram block zero is selected. Other blocks are selected dependent which Port C pin is active.

Title	MIDDLE RAM BLOCK 2	
Size B	Number SIX	Rev 0
Date 11 January 1993	Drawn by ASHE	
Filename MDRAM2.SCH	Sheet 1 of 1	

MEMORY BLOCK SELECT CRKT

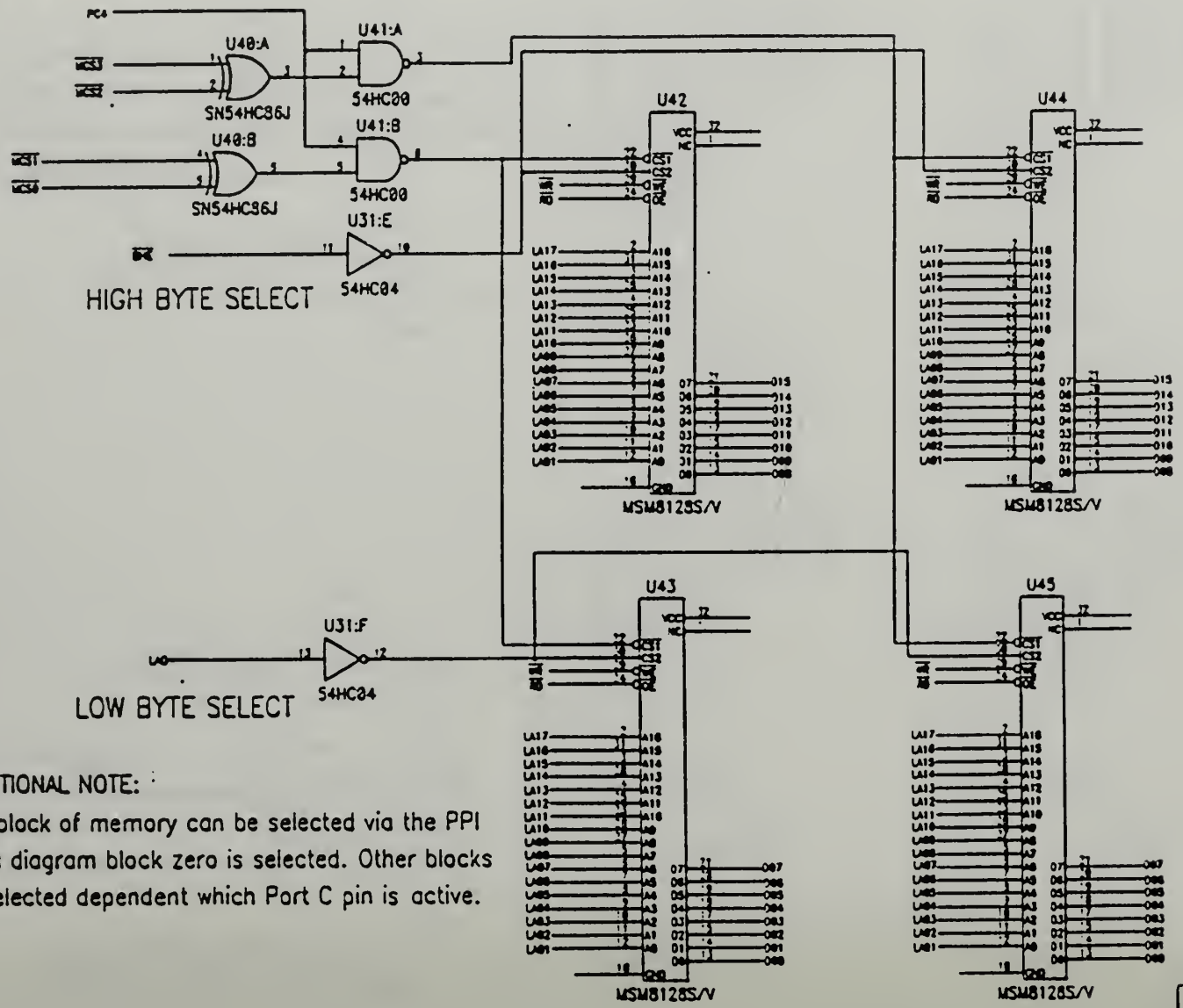


OPERATIONAL NOTE:

Each block of memory can be selected via the PPI In this diagram block zero is selected. Other blocks are selected dependent which Port C pin is active.

Title: MIDDLE RAM BLOCK 3		
Size: B	Number: SEVEN	Rev: 0
Date: 11 January 1993		Drawn by: [illegible]
Filename: MDRAM3.SCH		Sheet 1 of 1

MEMORY BLOCK SELECT CRKT

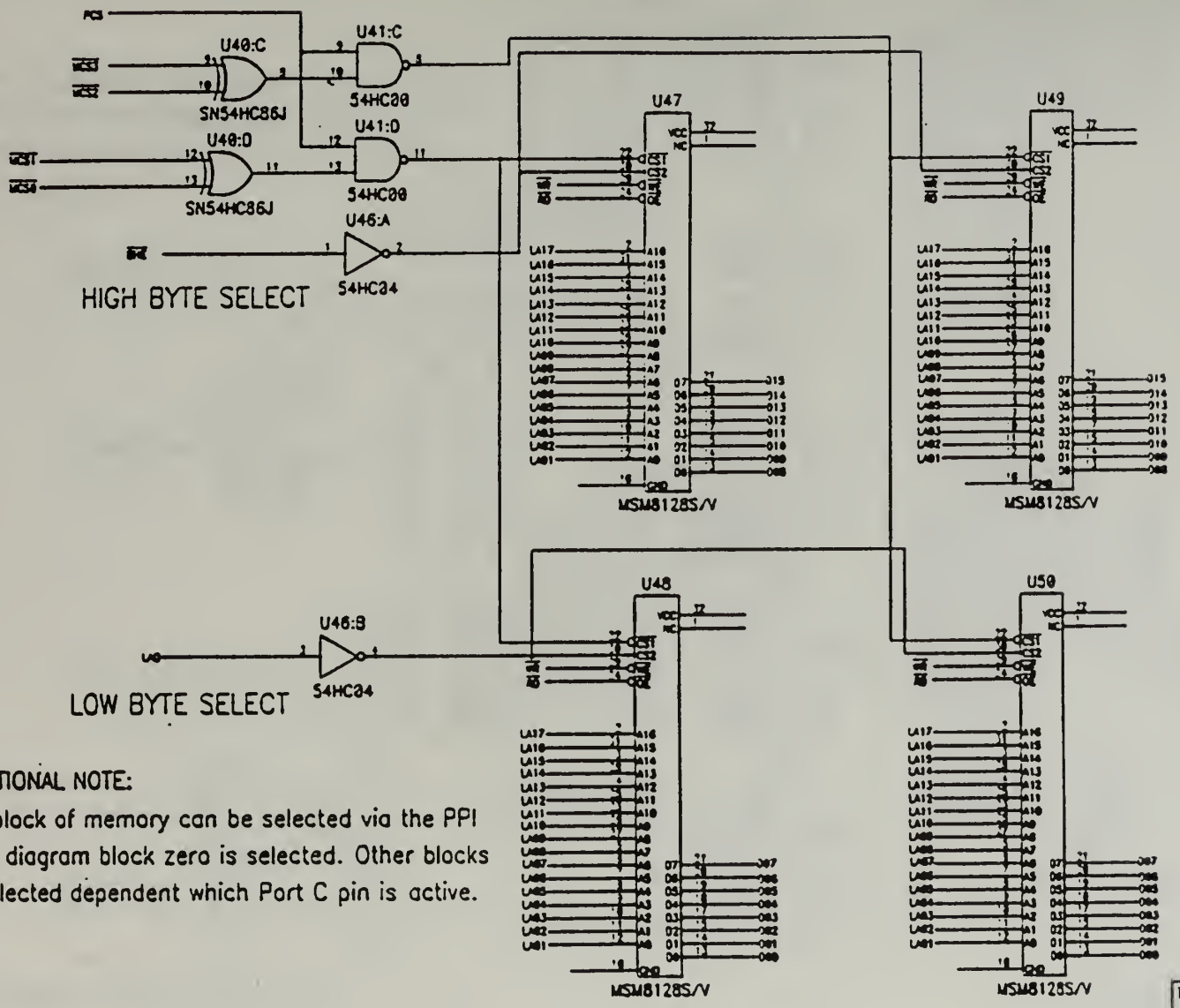


OPERATIONAL NOTE:

Each block of memory can be selected via the PPI In this diagram block zero is selected. Other blocks are selected dependent which Port C pin is active.

Title	MIDDLE RAM BLOCK 4	
Size B	Number EIGHT	Rev 0
Date 11 January 1993	Drawn by	
Filename VDRAM4.SCH	Sheet 1 of 1	

MEMORY BLOCK SELECT CRKT

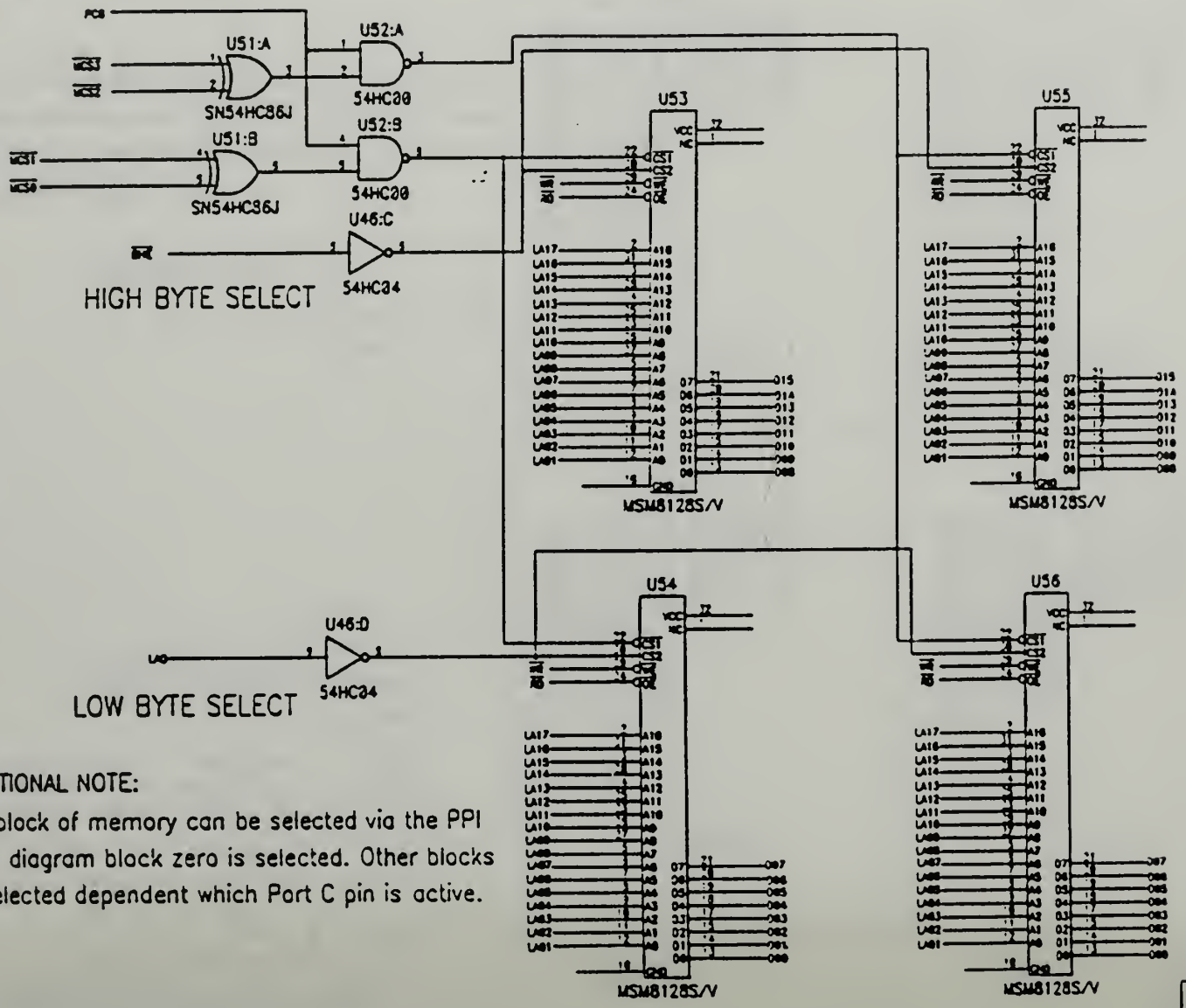


OPERATIONAL NOTE:

Each block of memory can be selected via the PPI In this diagram block zero is selected. Other blocks are selected dependent which Port C pin is active.

Title: MIDDLE RAM BLOCK 5		
Size: B	Number: NINE	Rev: 0
Date: 11 January 1993		Drawn by: ASME
Filename: MDRAM5.SCH		Sheet 1 of 1

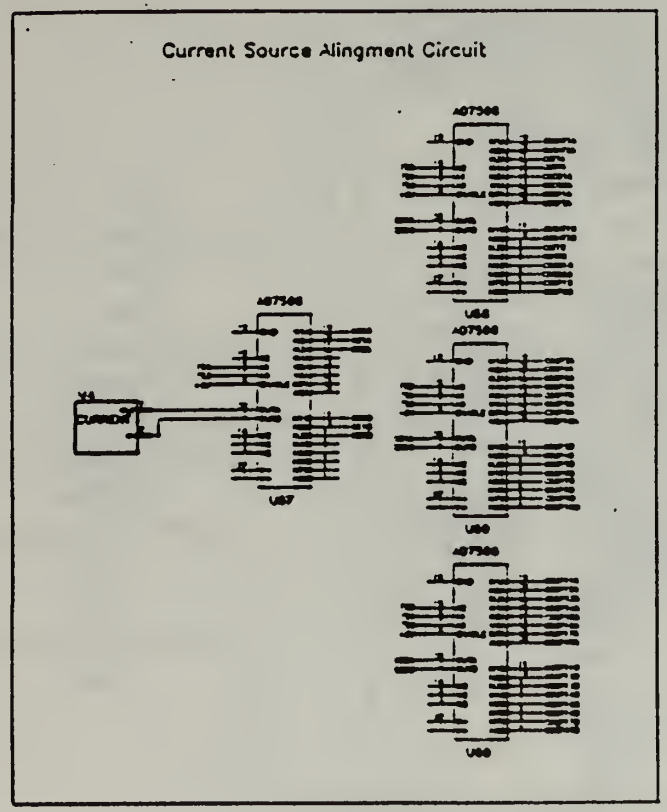
MEMORY BLOCK SELECT CRKT

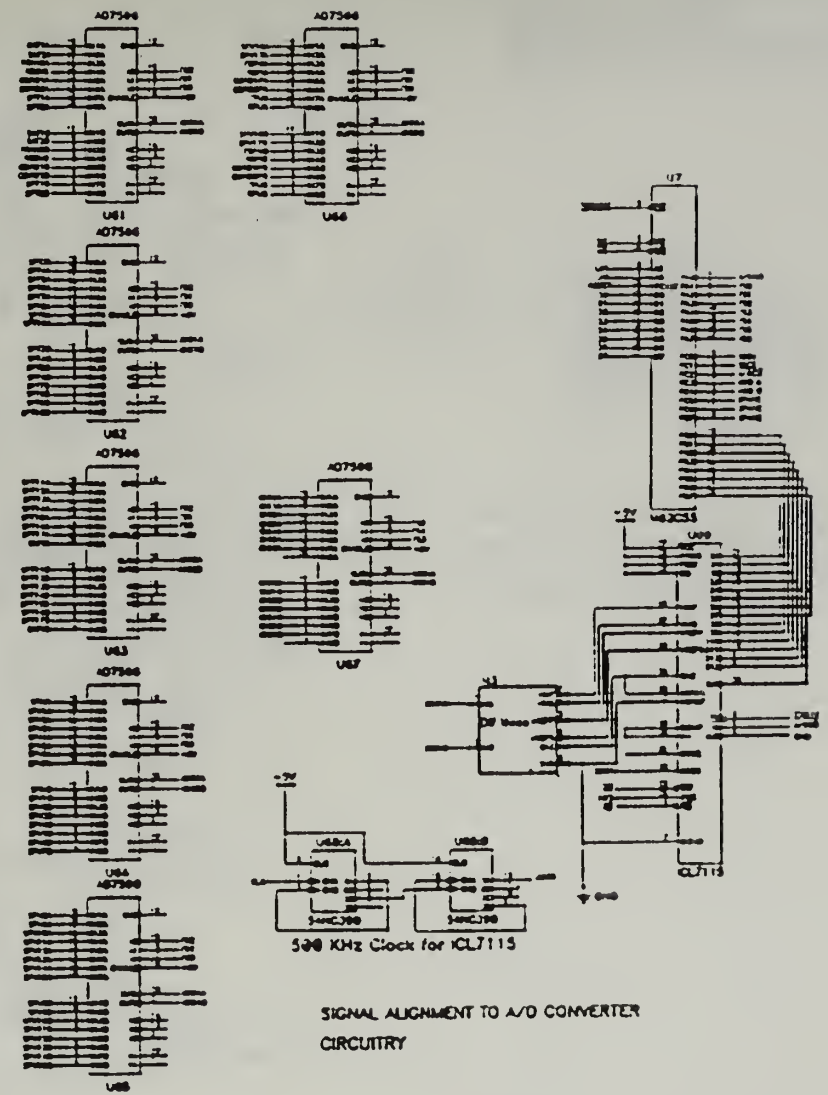


OPERATIONAL NOTE:

Each block of memory can be selected via the PPI In this diagram block zero is selected. Other blocks are selected dependent which Port C pin is active.

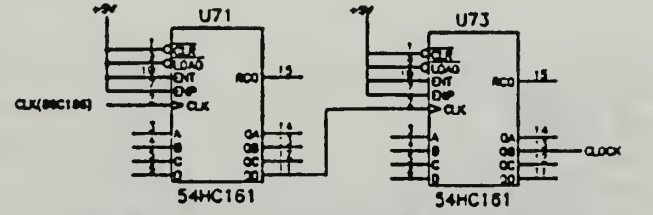
Title	MIDDLE RAM BLOCK 6	
Size 8	Number TEN	Rev 0
Date 11 January 1993	Drawn by ASHE	
Sheet 1 of 1		



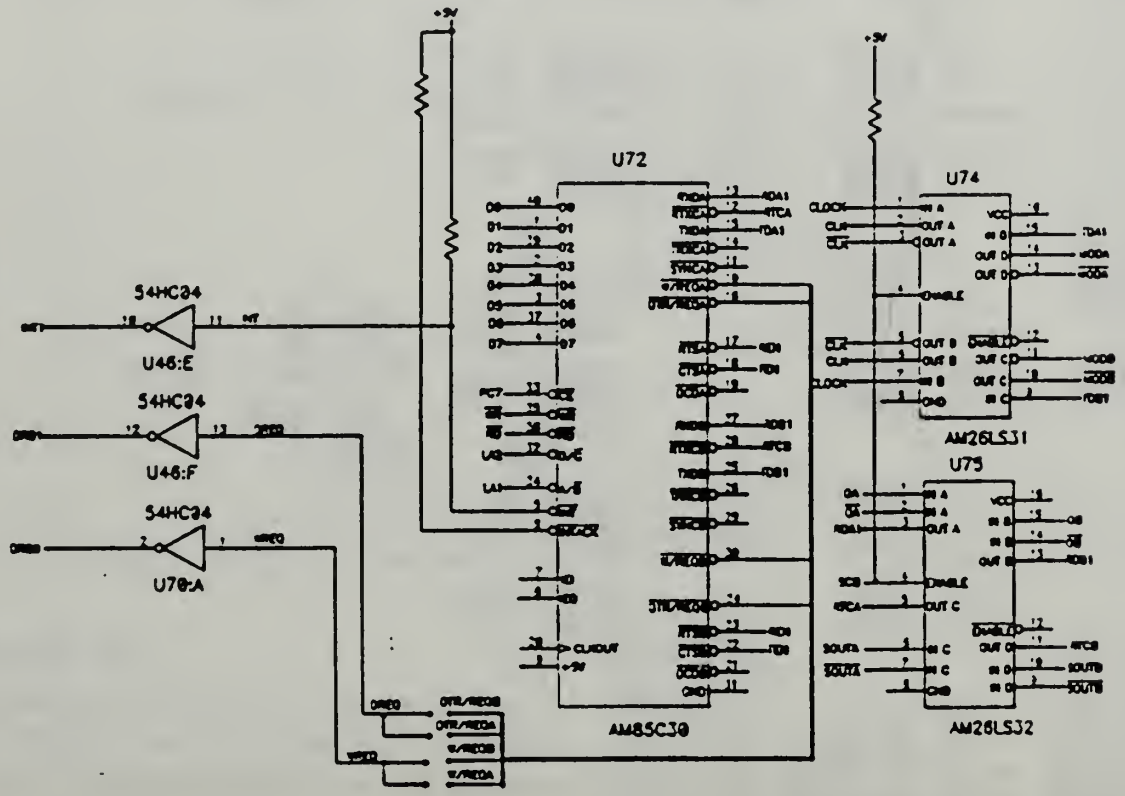


SIGNAL ALIGNMENT TO A/D CONVERTER CIRCUITRY

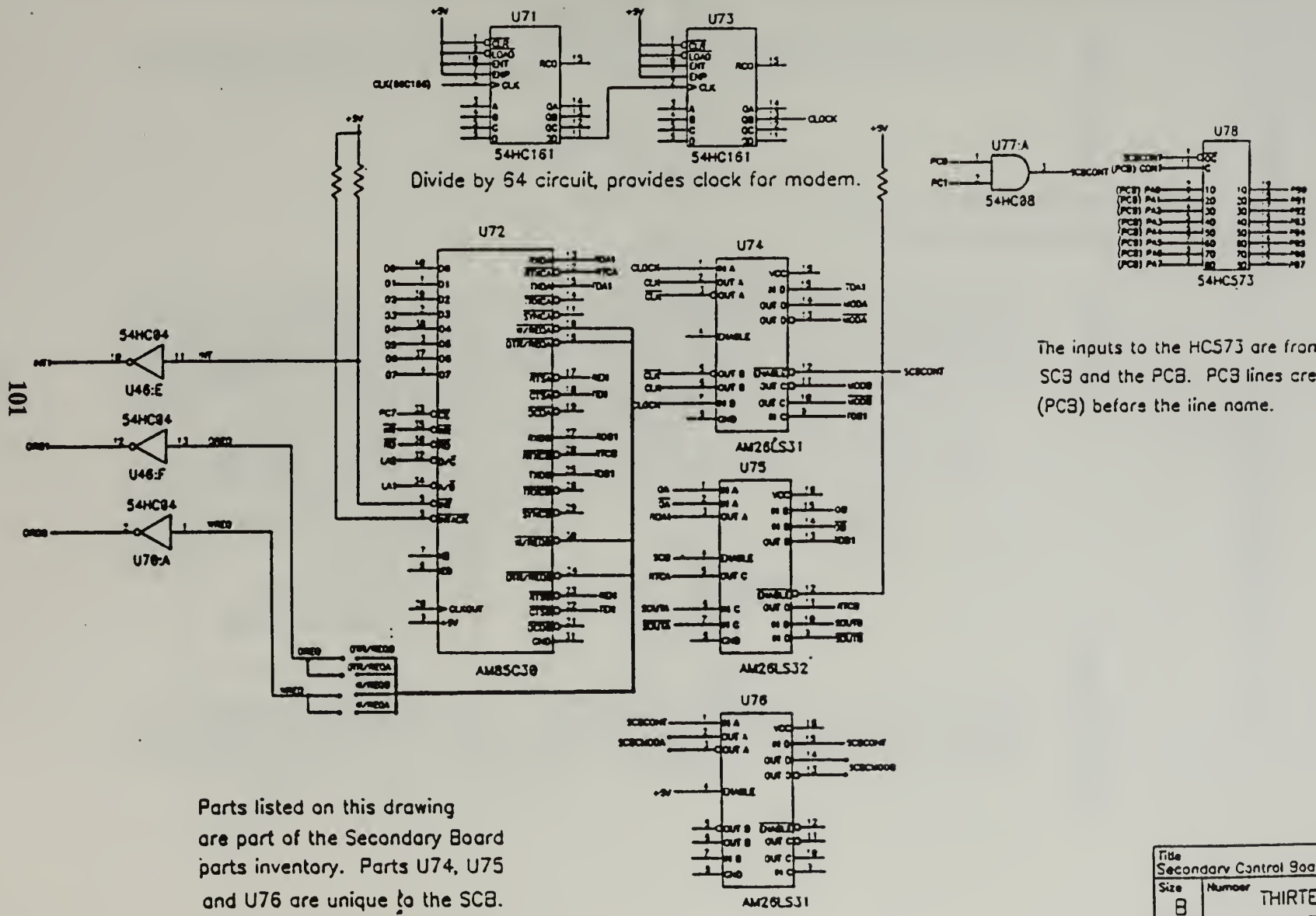
Title	PCB Telemetry Alignment Circuit	
Size C	Number ELEVEN	Rev 0
Date 13 January 1993	Drawn by ASME	
Filename TELMOD.301	Sheet 1 of 1	

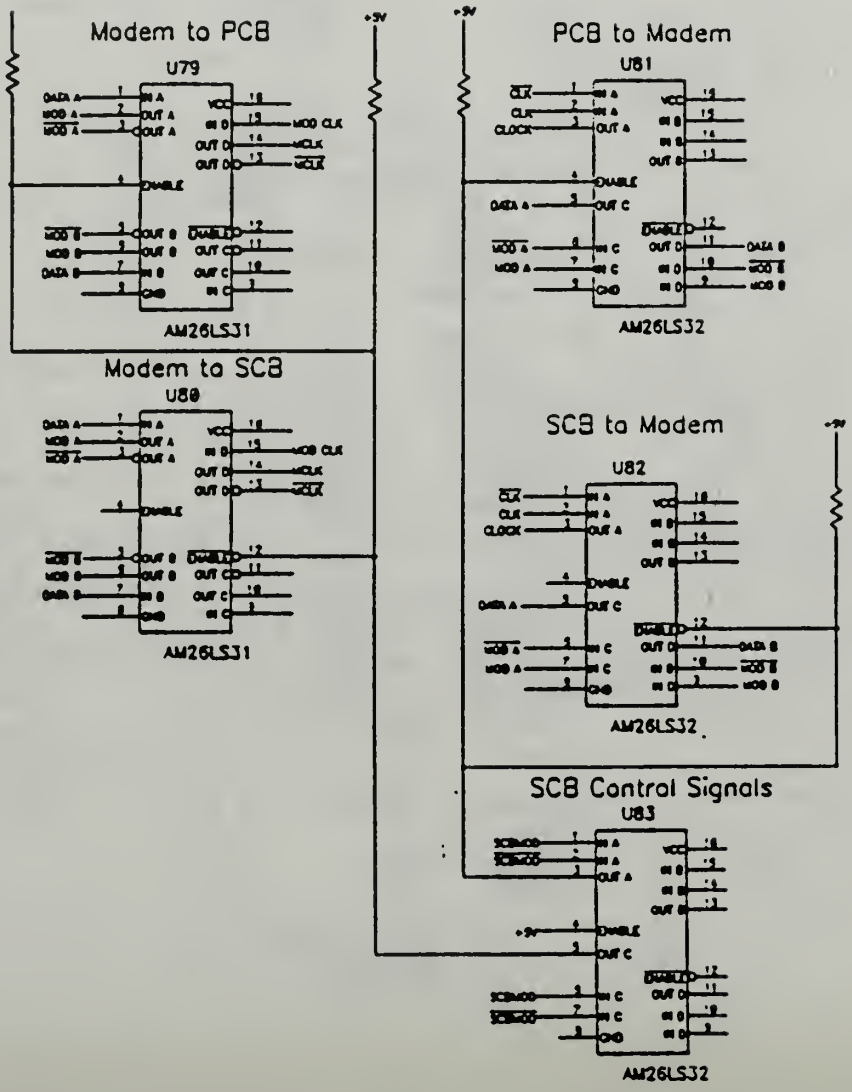


Divide by 64 circuit, provides clock for modem.



Title		
Primary Control Board Comm Section		
Size: B	Number: TWELVE	Rev: 0
Dated: December 1992	Drawn by: Jane	
Filename: pcbcom.sch	Sheet 1 of 1	


U71
54HC161
U73
54HC161
CLOCK
Divide by 64 circuit, provides clock for modem.
U77:A
54HC08
U78
54HC573
The inputs to the HC573 are from both the SCB and the PCB. PCB lines are denoted with (PCB) before the line name.
U72
AM85C30
U74
AM26LS31
U75
AM26LS32
U76
AM26LS31
54HC04
U46:E
54HC04
U46:F
54HC04
U76:A
101
Parts listed on this drawing are part of the Secondary Board parts inventory. Parts U74, U75 and U76 are unique to the SCB.
Title
Secondary Control Board Comm Section
Size
B
Number
THIRTEEN
Rev
0
Dated December 1992
Drawn by ASNS
Filename SCBCOM.SC
Sheet
of



Parts listed on this drawing are accounted for on the Secondary Control Board Inventory.

Title: Modem/Con Brd Interface		
Size: 9	Number: FOURTEEN	Rev: 0
Date: December 1992	Drawn by: ASOE	
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APPENDIX B DIGITAL CONTROL SYSTEM PARTS LIST

	Part Number	Description	Drawing Number
1.	U1	M80C186	ONE
2	U2	54HC573 LATCH	ONE
3.	U3	54HC573 LATCH	ONE
4.	U4	54HC573 LATCH	ONE
5.	U5	54HC245 TRANSCEIVER	ONE
6.	U6	54HC245 TRANSCEIVER	ONE
7.	U7	82C55 PPI	ONE
8.	U8A	54HC74 FLIP-FLOP	TWO
9.	U9A	54HC32 OR GATE	TWO
10.	U9B	54HC32 OR GATE	TWO
11.	U9C	54HC32 OR GATE	TWO
12.	U9D	54HC32 OR GATE	TWO
13.	U10	WS27010L EPROM	TWO
14.	U11	WS27010L EPROM	TWO
15.	U12	WS27010L EPROM	TWO
16.	U13	WS27010L EPROM	TWO
17.	U14A	54HC04 INVERTER	THREE
18.	U14B	54HC04 INVERTER	THREE
19.	U15	MSM8128S/V 128X8 RAM	THREE
20.	U16	MSM8128S/V 128X8 RAM	THREE
21.	U17	MSM8128S/V 128X8 RAM	THREE
22.	U18	MSM8128S/V 128X8 RAM	THREE
23.	U14C	54HC04 INVERTER	FOUR
24.	U14D	54HC04 INVERTER	FOUR
25.	U19A	54HC86J XOR GATE	FOUR
26.	U19B	54HC86J XOR GATE	FOUR
27.	U20A	54HC00 NAND GATE	FOUR
28.	U20B	54HC00 NAND GATE	FOUR
29.	U21	MSM8128S/V 128X8 RAM	FOUR
30.	U22	MSM8128S/V 128X8 RAM	FOUR
31.	U23	MSM8128S/V 128X8 RAM	FOUR

	Part Number	Description	Drawing Number
32.	U24	MSM8128S/V 128X8 RAM	FOUR
33.	U14E	54HC04 INVERTER	FIVE
34.	U14F	54HC04 INVERTER	FIVE
35.	U19C	54HC86J XOR GATE	FIVE
36.	U19D	54HC86J XOR GATE	FIVE
37.	U20C	54HC00 NAND GATE	FIVE
38.	U20D	54HC00 NAND GATE	FIVE
39.	U25	MSM8128S/V 128X8 RAM	FIVE
40.	U26	MSM8128S/V 128X8 RAM	FIVE
41.	U27	MSM8128S/V 128X8 RAM	FIVE
42.	U28	MSM8128S/V 128X8 RAM	FIVE
43.	U29A	54HC86J XOR GATE	SIX
44.	U29B	54HC86J XOR GATE	SIX
45.	U30A	54HC00 NAND GATE	SIX
46.	U30B	54HC00 NAND GATE	SIX
47.	U31A	54HC04 INVERTER	SIX
48.	U31B	54HC04 INVERTER	SIX
49.	U32	MSM8128S/V 128X8 RAM	SIX
50.	U33	MSM8128S/V 128X8 RAM	SIX
51.	U34	MSM8128S/V 128X8 RAM	SIX
52.	U35	MSM8128S/V 128X8 RAM	SIX
53.	U29C	54HC86J XOR GATE	SEVEN
54.	U29D	54HC86J XOR GATE	SEVEN
55.	U30C	54HC00 NAND GATE	SEVEN
56.	U30D	54HC00 NAND GATE	SEVEN
57.	U31C	54HC04 INVERTER	SEVEN
58.	U31D	54HC04 INVERTER	SEVEN
59.	U36	MSM8128S/V 128X8 RAM	SEVEN
60.	U37	MSM8128S/V 128X8 RAM	SEVEN
61.	U38	MSM8128S/V 128X8 RAM	SEVEN
62.	U39	MSM8128S/V 128X8 RAM	SEVEN
63.	U40A	54HC86J XOR GATE	EIGHT
64.	U40B	54HC86J XOR GATE	EIGHT
65.	U41A	54HC00 NAND GATE	EIGHT
66.	U41B	54HC00 NAND GATE	EIGHT
67.	U31E	54HC04 INVERTER	EIGHT
68.	U31F	54HC04 INVERTER	EIGHT
69.	U42	MSM8128S/V 128X8 RAM	EIGHT

	Part Number	Description	Drawing Number
70.	U43	MSM8128S/V 128X8 RAM	EIGHT
71.	U44	MSM8128S/V 128X8 RAM	EIGHT
72.	U45	MSM8128S/V 128X8 RAM	EIGHT
73.	U40C	54HC86J XOR GATE	NINE
74.	U40D	54HC86J XOR GATE	NINE
75.	U41C	54HC00 NAND GATE	NINE
76.	U41D	54HC00 NAND GATE	NINE
77.	U46A	54HC04 INVERTER	NINE
78.	U46B	54HC04 INVERTER	NINE
79.	U47	MSM8128S/V 128X8 RAM	NINE
80.	U48	MSM8128S/V 128X8 RAM	NINE
81.	U49	MSM8128S/V 128X8 RAM	NINE
82.	U50	MSM8128S/V 128X8 RAM	NINE
83.	U51A	54HC86J XOR GATE	TEN
84.	U51B	54HC86J XOR GATE	TEN
85.	U52A	54HC00 NAND GATE	TEN
86.	U52B	54HC00 NAND GATE	TEN
87.	U46C	54HC04 INVERTER	TEN
88.	U46D	54HC04 INVERTER	TEN
89.	U53	MSM8128S/V 128X8 RAM	TEN
90.	U54	MSM8128S/V 128X8 RAM	TEN
91.	U55	MSM8128S/V 128X8 RAM	TEN
92.	U56	MSM8128S/V 128X8 RAM	TEN
93.	U57	AD7506 MUX	ELEVEN
94.	U58	AD7506 MUX	ELEVEN
95.	U59	AD7506 MUX	ELEVEN
96.	U60	AD7506 MUX	ELEVEN
97.	U61	AD7506 MUX	ELEVEN
98.	U62	AD7506 MUX	ELEVEN
99.	U63	AD7506 MUX	ELEVEN
100.	U64	AD7506 MUX	ELEVEN
101.	U65	AD7506 MUX	ELEVEN
102.	U66	AD7506 MUX	ELEVEN
103.	U67	AD7506 MUX	ELEVEN
104.	U68A	54HC390 COUNTER	ELEVEN
105.	U69	ICL7115 A/D CONVERTER	ELEVEN
106.	U46E	54HC04 INVERTER	TWELVE

	Part Number	Description	Drawing Number
107.	U46F	54HC04 INVERTER	TWELVE
108.	U70A	54HC04 INVERTER	TWELVE
109.	U71	54HC161 COUNTER	TWELVE
110.	U72	AM85C30 SCC	TWELVE
111.	U73	54HC161 COUNTER	TWELVE
112.	U74	AM26LS31 LINE DRIVER	TWELVE
113.	U75	AM26LS32 RECEIVER	TWELVE
114.	U46E(SCB)	54HC04 INVERTER	THIRTEEN
115.	U46F(SCB)	54HC04 INVERTER	THIRTEEN
116.	U70A(SCB)	54HC04 INVERTER	THIRTEEN
117.	U71(SCB)	54HC161 COUNTER	THIRTEEN
118.	U72(SCB)	AM85C30 SCC	THIRTEEN
119.	U73(SCB)	54HC161 COUNTER	THIRTEEN
120.	U74(SCB)	AM26LS31 LINE DRIVER	THIRTEEN
121.	U75(SCB)	AM26LS32 RECEIVER	THIRTEEN
122	U76(SCB)	AM26LS31 LINE DRIVER	THIRTEEN
123.	U77(SCB)	54HC573 LATCH	THIRTEEN
124.	U78A(SCB)	54HC08 AND GATE	THIRTEEN
125.	U79(MCB)	AM26LS31 LINE DRIVER	FOURTEEN
126.	U80(MCB)	AM26LS31 LINE DRIVER	FOURTEEN
127.	U81(MCB)	AM26LS32 RECEIVER	FOURTEEN
128.	U82(MCB)	AM26LS32 RECEIVER	FOURTEEN
129.	U83(MCB)	AM26LS32 RECEIVER	FOURTEEN

SCB := SECONDARY CONTROL BOARD
MCB:= MODEM CONTROL BOARD

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