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Configurable Fault-Tolerant Processor (CFTP) for Space Based Applications

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Abstract

The harsh radiation environment of space, the propensity for SEUs to perturb the operations of silicon based electronics, the rapid development of microprocessor capabilities and hence software applications, and the high cost (dollars and time) to develop and prove a system, require flexible, reliable, low cost, rapidly developed system solutions. Consequently, a reconfigurable Triple Modular Redundant (TMR) System-on-a-Chip (SOC) utilizing Field Programmable Gate Arrays (FPGAs) provides a viable solution for space based systems. The Configurable Fault Tolerant Processor (CFTP) is such a system, designed specifically for the purpose of testing and evaluating, on orbit, the reliability of instantiated TMR soft-core microprocessors, as well as the ability to reconfigure the system to support any onboard processor function.

The CFTP maximizes the use of Commercial Off-The-Shelf (COTS) technology to investigate a low-cost, flexible alternative to processor hardware architecture, with a Total Ionizing Dose (TID) tolerant FPGA as the basis for a SOC. The flexibility of a configurable processor, based on FPGA technology, will enable on-orbit upgrades, reconfigurations, and modifications to the architecture in order to support dynamic mission requirements.

The CFTP payload consists of a Printed Circuit Board (PCB) of 5.3 inches x 7.3 inches utilizing a slightly modified PC/104 bus interface. The initial FPGA configuration will be an instantiation of a TMR processor, with included Error Detection and Correction (EDAC) and memory controller circuitry. The PCB is designed with requisite supporting circuitry including a configuration controller FPGA, SDRAM, and Flash memory in order to allow the greatest variety of possible configurations.

The CFTP is currently manifested as a Space Test Program (STP) experimental payload on the Naval Postgraduate School's NPSAT1 and the United States Naval Academy's MidSTAR-1 satellites.

Introduction

The space environment exacerbates common electrical circuit error occurrences seen on earth, as well as introduces a new set of problems. Close to earth's surface, within the atmosphere, circuits are shielded from many of the effects of space, most notably radiation. Leaving the earth's atmosphere, a semiconductor device is exposed to an environment heavily populated by high-energy ions. These ions can introduce a variety of errors into logic circuits.

Complementary Metal Oxide Semiconductor (CMOS) devices have a well-documented history of susceptibility to the effects of ionized particles. This radiation induces two principal types of failures; total-dose effects and Single-Event Effects (SEEs), which include Single-Event Upsets (SEUs) and Single-Event Latchups (SELs). Total Ionizing Dose (TID) effects contribute to the deterioration of a device over time, and SEEs are those radiation effects that occur unpredictably with a wide range of consequences.

Many methods exist to mitigate the effects of SEE generated errors in circuits, both on earth and on orbit. Manufacturing and fabrication techniques can be used to reduce the circuit susceptibility to TID effects. While some of these techniques will decrease the circuit susceptibility to SEEs, mitigation schemes based on architectural modifications are also often necessary. One such mitigation scheme is Triple Modular Redundancy (TMR), which is a hardware implementation that includes replicated circuits and voting logic to detect and correct a faulty value. This replication and voting may occur at the individual gate level or at the block or subsystem level, but it requires special and unique chips

and architectures. This uniqueness means that it is extremely difficult (in practice impossible) to use state-of-the-art Commercial-Off-The-Shelf (COTS) devices in most space environments.

Since the market introduction of Field Programmable Gate Arrays (FPGA) in the late 1990's, FPGA technology has matched, if not exceeded, Moore's Law [1]. Available devices now support more than 8 Million logic gate (equivalents) on a single chip, and run at speeds of up to 420 MHz. At these performance levels and gate counts, these chips are now robust enough to support an entire TMR processor system on a single chip. In addition, since FPGAs are in-circuit re-configurable, it is possible to completely change the architecture at any time, even months after launch..

These advantages come with significant risks and concerns The Configurable Fault-Tolerant Processor (CFTP) is designed specifically for the purpose of testing and evaluating, on orbit, the reliability of FPGA instantiated TMR soft-core microprocessors, and the ability to reconfigure the system to completely different processor architectures or dedicated application-specific circuits.

Field Programmable Gate Arrays

FPGAs are user-programmable devices that perform the functions of Large Scale Integration (LSI) circuitry. They are comprised of thousands to millions of programmable logic elements, each capable of performing any logic function, in a sea of interconnects [2]. The basic architecture of an FPGA is an array of uncommitted circuit elements, called *logic blocks*, and interconnect resources [3]. FPGA configuration is performed through programming by the end user. Because FPGAs support very high logic density, this technology has been responsible for a major shift in the way few-of-a-kind or prototype digital circuits are designed [3].

FPGAs are available as both Radiation Hardened (RADHARD) and COTS devices. Combining the TID tolerance of the RADHARD FPGAs with various mitigation schemes, FPGAs have the potential to perform well in space applications. Since an FPGA can be configured to perform the functions of COTS processors, it now becomes possible to provide COTS functionality in a RADHARD device.

Applying the re-configurability of RADHARD FPGAs to the space industry provides a tool for engineers to overcome some of the constraints that are imposed on systems designers. First, systems can now be designed using FPGAs with the most current configuration of a processor. As processor architectures change and advance, the FPGA's configuration can be changed to match, not only during develoment but conceivably throughout the on-orbit life of the system.

Soft-cores

A soft-core is a software expression in Hardware Description Language (HDL) of a processor design. As such, it typically lags its hardwired version in performance, but it can be changed or upgraded by simply re-coding. FGPAs can be configured with soft-cores to perform any conceivable function that could be performed by an ASIC, from rudimentary state-machines to complex microprocessors. Combining the most sophisticated HDL expressions for microprocessors with state-of-the-art FPGAs, provides the capability to implement reconfigurable processing into an environment where reconfiguring hardwired systems is impossible.

Configurable Fault-Tolerant Processor (CFTP)

The primary objectives of the CFTP flight experiment are two-fold. First, the CFTP will evaluate, in various orbital regimes, a TMR, fault-tolerant, reconfigurable SOC design in order to mitigate bit errors in computation by detecting and correcting errors using voting logic. Second, the CFTP will demonstrate the use of reprogrammable FPGA technology in spacecraft architecture as a viable means of decreasing development time, decreasing costs, and increasing reliability as well as flexibility in hardware development and implementation [4].

Concept

The CFTP design is centered on the investigation of a low-cost, flexible alternative to processor-hardware architectures, using FPGAs as a basis for a SOC. The increased flexibility of the FPGA implementation will serve as a means of decreasing development time while allowing software development and component integration to commence at the earliest stages of the process. The expectation is that the processor can be re-configured to alleviate the design constraints that arise out of the process. Our version of TMR provides an essential aspect of the reliability of the CFTP by detecting and correcting single event transients without requiring a system reset and the commensurate loss of data normally associated with a return to a trusted state. Finally, the flexibility of a configurable processor, based on COTS FPGA technology, will enable on-orbit upgrades, reconfigurations, and modifications to the onboard architecture in order to support dynamic mission requirements.

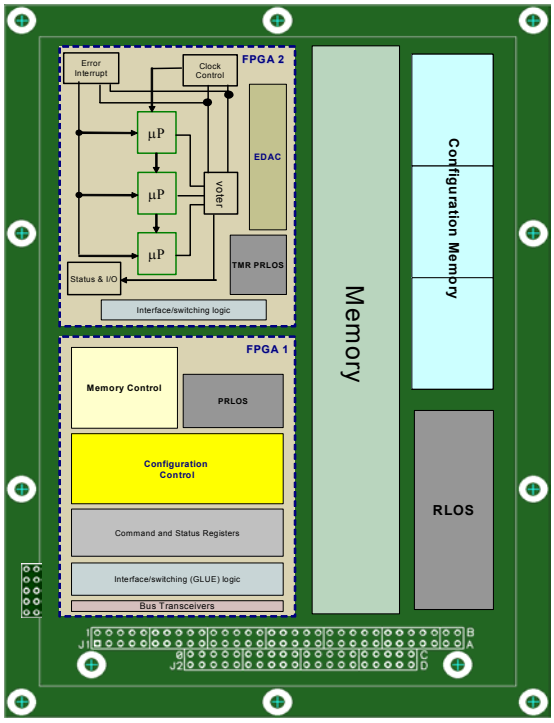

Figure 1. CFTP Conceptual Illustration.

Components

The basic structure of the CFTP is depicted in Figure 1, and while it is not a true System on a single chip, it is close. As listed in Table 1, the total chip count is 13, consisting of two FPGAs, 8 memory chips, two power converters and an oscillator. The TMR Configurable Processor FPGA is the large block in the top left and the Configuration Controller FPGA is in the lower left with its associated functions. On the right side of the image are the system memory, configuration memory, and left-over discrete components. The CFTP utilizes Xilinx RADHARD Static Random-Access-Memory (SRAM) FPGAs, (part number XQVR600 in CB228 packages.) These devices have 661,111 gates and were selected for both the Configurable Processor and the Configuration Controller FPGAs due to TID tolerance and the Quad Flat-pack packaging. Supporting the FPGAs are Hitachi (now Elpida) Synchronous Dynamic Random-Access Memory (SDRAM), Xilinx In-System Programmable (ISP) and One-Time Programmable (OTP) Programmable Read Only Memory (PROM), and Intel Electrically Erasable PROM (EEPROM), as well as discrete devices including resistors, capacitors and voltage regulators, and an oscillator. The SDRAM provides system memory for the normal functioning of the system as a processor. The EEPROM and PROM provide configuration storage for the two FPGAs. Using an elaborate interconnection architecture between the CFTP's devices provides maximum flexibility in both how the devices are configured and how the devices communicate between each other. Because the FPGAs can be configured for almost an infinite number of functions, providing a robust interconnection architecture allows the greatest flexibility for future configurations. .

Table 1. CFTP Parts List.

Device	Primary Function	Alternate/Secondary Functions	Potential Future Uses
Xilinx XQVR600 FPGA	Configurable Processor	TMR Microprocessors	Image Compression Network/Communications Routing Satellite On-Board Systems redundancy/Back-up DSP Most functions listed for Configuration Controller Future Functions TBD
Xilinx XQVR600 FPGA	Configuration Controller	SDRAM Configuration Controller EDAC Controller JTAG Controller Readback, Partial reconfiguration, and background CFTP Interrupt Handling/Control Command and Status registers Bus Address Decoding PC/104 Bus interface	Bus Master Functions Communications Control Future Functions TBD
Xilinx XC18V04 ILP PROM	Developmental Configuration Storage for Configuration Controller	Will be replaced by XQR17V16 for flight	
Xilinx XQR17V16	Flight Configuration Storage for Configuration Controller	Up to 8 additional configurations including BIST and Status Reporting	Future Configurations TBD
Intel 28F320C3 Flash	Configuration Storage for Configurable Processor	Storage for Operating System/Codes Extra application space for microprocessor	
Hitachi SDRAM	System Memory	User defined storage	
3.3V Regulator	5V to 3.3V Conversion		
2.5V Regulator	3.3V to 2.5V Conversion		
Oscillator Socket	Clock Signal Development	Optimized Flight Board Oscillator (TBD)	

Architecture

The CFTP architecture was designed with maximum flexibility to support future, yet to be determined, soft-cores. This required logic paths to be created between the CFTP's components as well as between the CFTP and the system host for multiple functions, many without specific definition.

The CFTP primary design architecture supports a rudimentary 16-bit TMR microprocessor developed in References [5] and [6], running in the Configurable Processor FPGA with the SDRAM controller and EDAC controller cores also instantiated in that FPGA. The Configuration Controller FPGA would then be responsible for controlling the background partial reconfiguration of the Processor FPGA, providing PC/104 Bus Interface services, providing a Command and Status register, satellite C&DH interrupt handling functions and bus address decoding, as well as providing its own background SEU-mitigating scrub routine control.

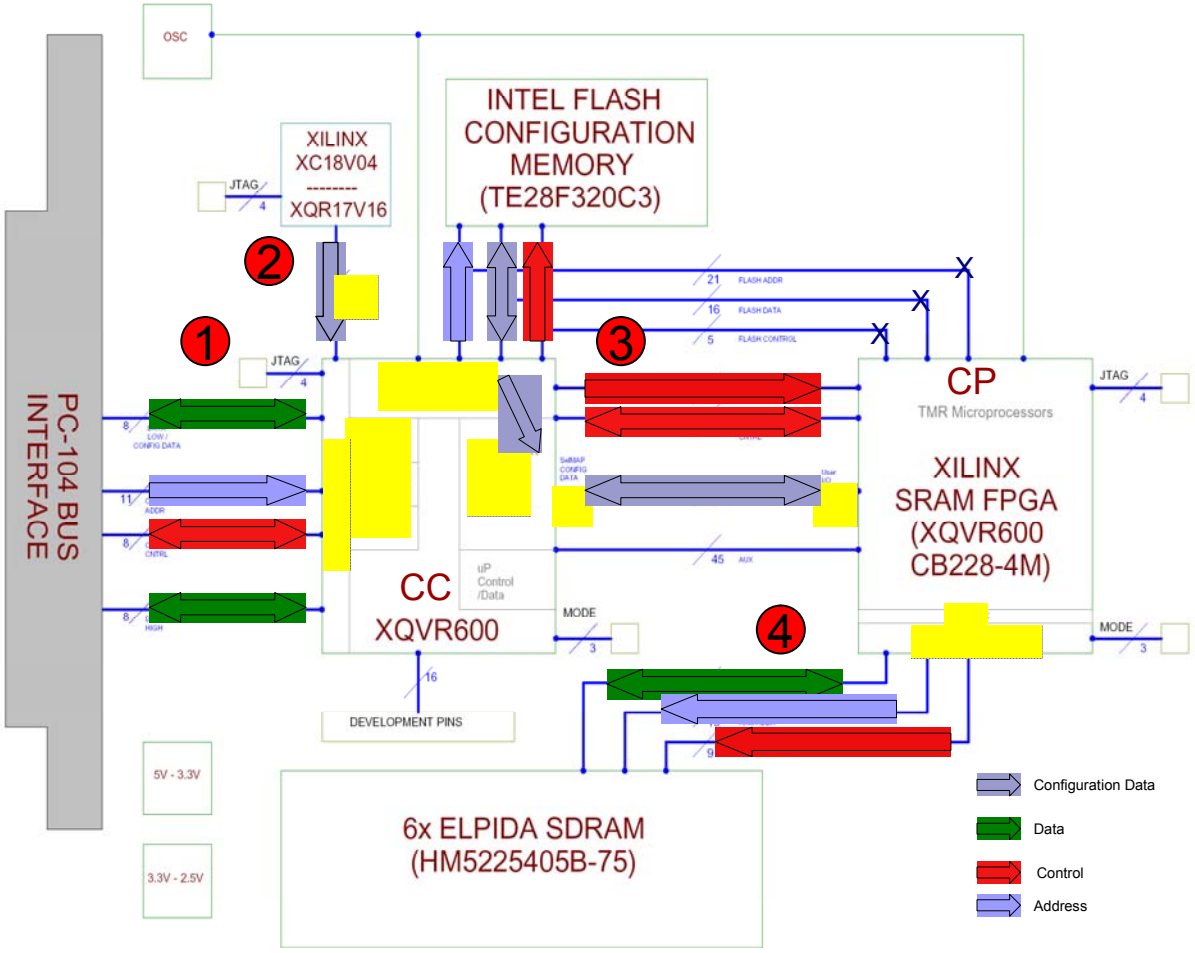

Figure 2. CFTP Block Diagram

This concept is graphically depicted in figure 2. Control, data and address signals across the PC/104 bus (1) trigger the Configuration Controller (CC) to configure in its initial state from the PROM (2), which in turn commands and controls the initial configuration of the Configurable Processor (CP) from the flash memory (3). During normal operations, the CP will utilize the SDRAM for its processor memory (4) while the CC controls background configuration scrubbing of the CP using the flash memory (3). Also, the CC will control its own background scrubbing (self-scrubbing mode) using the configuration stored in the PROM (2). If either the CP or the CC require bus attention, then it is the CC's responsibility to negotiate the interrupt service and handling routines with the host system (1).

Because the single XQVR600 may be too small to contain TMR microprocessor cores and the additional controllers mentioned above, multiple direct traces connect the user configurable I/O pins of the two FPGAs. This allows for moving various "components" of the architecture to one or the other FPGA, depending on the designer's constraints. For example, one of the three microprocessors that make up the TMR architecture could be moved from the Configurable Processor to the Configuration Controller, allowing for larger microprocessor soft-cores to be used. Anticipating "unknown-unknowns," additional paths have been designed into the CFTP. A 45-bit-wide dedicated path exists between the two FPGAs, conceptually for the PC/104 to exchange data directly with the Configurable Processor, via the bus transceiver logic instantiated in the Configuration Controller FPGA. The 42-bit-wide Flash memory data/address/ control busses are paralleled between the FPGAs, providing an additional FPGA to FPGA path. It is worth mentioning that the user I/O FPGA pins (all of which these are) can be internally configured for a number of input and output functions, including pull-up, pull-down, and high impedance conditions. Thus, depending on the operating configurations of the two FPGAs, these paths can be used between the FPGAs and or between each of them

and the Flash. Additionally, the pins that are dual use for configuring the devices and as user IO are, for the most part, connected in parallel between the devices providing further on-board flexibility.

Configuring the FPGAs

In order to satisfy future configuration requirements and to achieve requisite SEE tolerance, suitable configuration/reconfiguration capabilities were designed into the CFTP architecture. Consideration was given to the number of available pins on the CB228 packages; the decision to use, and how best to employ, partial reconfiguration and scrubbing as error mitigation techniques; and the need to ensure the Configuration Controller FPGA is as RADHARD as possible. The CFTP design includes a wide variety of choices for the programmer. Configuration options maximize flexibility of the FPGAs by including JTAG readback and reconfiguration controller, SelectMAP reconfiguration controller, Master-Slave Serial load, and self-scrubbing functions. Table 2 summarizes the methods available for the CFTP's FPGAs to be configured.

Joint Test Action Group (JTAG) / Boundary Scan

Boundary Scan provides a very useful developmental method of loading, reading back and testing configurations, as well as providing a method for background configuration scrubbing without interrupting surface processing. The JTAG functionality in the CFTP is provided for two principal reasons. First, it is easy to use and it conveniently interfaces with desktop Personal Computers (PCs) supported by useful development software. Second, the protocol supports robust test functions so this will be the preferred method of loading the configurable devices on the board during development. Third, it will be via the JTAG port that the Configuration Controller FPGA performs its SEU mitigation background scrubbing while on-orbit, a capability also provided for in the Configurable Processor.

Configured Device	source of Config.	Control	Method (Mode)	Mode pins set by:	Clock from	Initialize	Reconfigure	Scrubbing	Comments
CP	Flash	CC	SelMAP	Default	Osc.	X	X	X	CP Default configuration mode
CP	Flash	CC	Sl. Serial	CC	CC		X		
CP	Flash	CP	JTAG	CC	CC			X	Self-scrub, CP must Serialize data
CP	PROM	CC	Sl. Serial	CC	CC		X		
CP	PC/104	CC	SelMAP	CC	Osc.	X	X		CC serves PC/104 data like Flash
CP	PC/104	CC	Sl. Serial	CC	CC		X		
CP	Flash	CC	Mas. Ser.	CC	CP		X		CC must appear as a PROM to CP
CP	PROM	CC	Mas. Ser	CC	CP		X		CC must appear as a PROM to CP
CC	PROM	CC	Mas. Ser	Default	CC	X	X		CC Default configuration mode
CC	Flash	CP	SelMAP	CP	Osc.		X	X	
CC	PROM	CC	JTAG	CC	CC		X	X	Self-scrub
CC	PC/104	CC	JTAG	CC	CC			X	Self-scrub
CC	Flash	CP	Mas. Ser	CP	CP		X		CP must appear as PROM to CC

CC: Configuration Controller
CP: Configurable Processor
Osc: Oscillator
Sl Serial: Slave Serial mode
Mas. Ser: Master Serial mode
Initialize refers to power-off/hard reset
Reconfigure refers to power-on/soft reset
Scrubbing refers to any reconfiguration occurring in the background of normal operations

Table 2 Configuration methods for CP and CC FPGAs

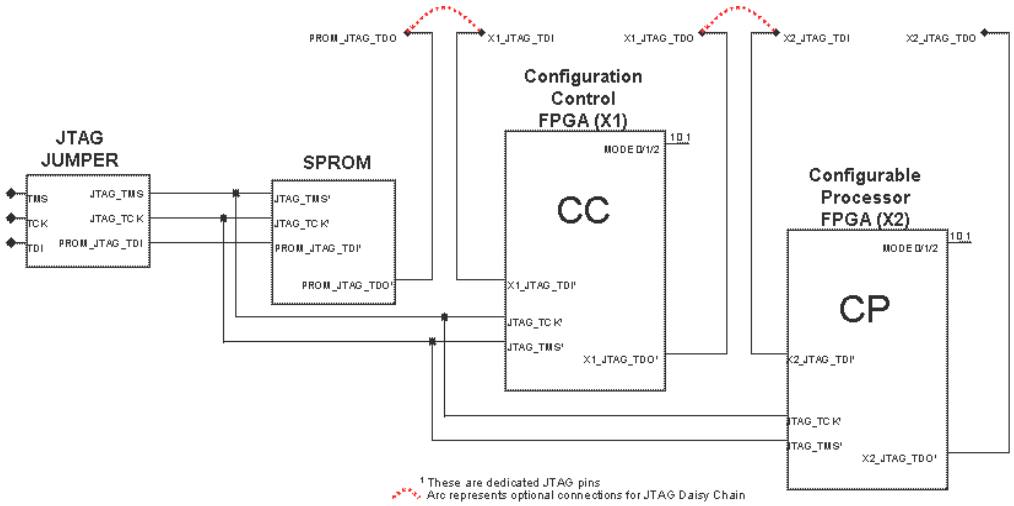

Figure 3 JTAG Daisy Chain

The JTAG daisy chain is shown in Figure3, and the self-scrubbing JTAG path is shown for the Configuration Controller in Figure 4.

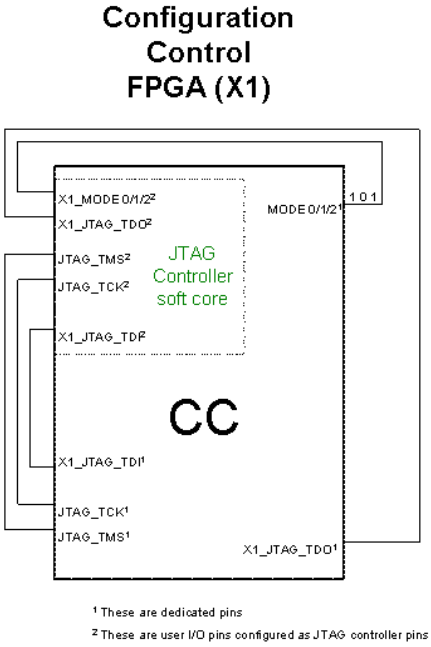

Figure 4. JTAG Self-Scrubbing Configuration.

SelectMAP

The primary method of loading the Configurable Processor will be using SelectMAP. This method provides for 8-bit-wide parallel loading of the device and is the preferred method for performing background configuration readback and partial reconfiguration. There are two principal drawbacks when using the mode. First, although the SelectMAP pins are dual-use, they must be dedicated to configuration loading when the readback/reconfiguration scheme is utilized. Secondly, this method requires an external controller. Therefore, the CFTP design allows either FPGA to act as the SelectMAP controller for the other device. The block diagram with the Configurable Processor in SelectMAP is shown in Figure 5.

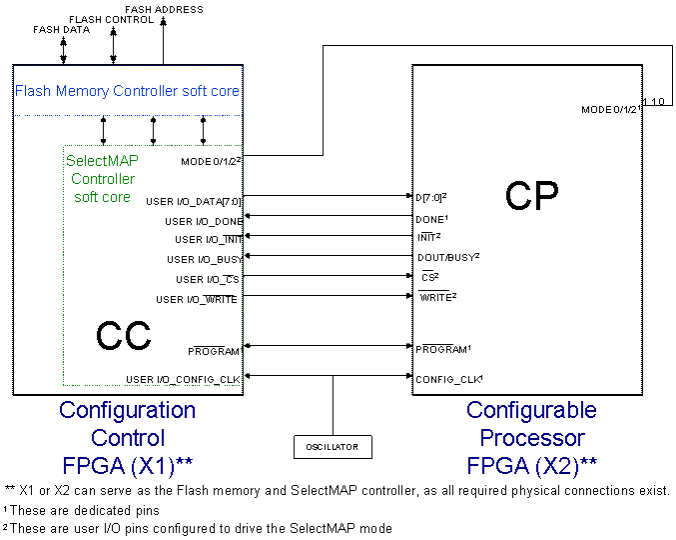

Figure 5. SelectMAP Mode.

Master-Slave Serial Mode

The Master Serial mode is the default method of loading a configuration into a Xilinx Virtex FPGA. This method was selected to be the fail safe mode to load the Configuration Controller FPGA with its initial configuration, as it is extremely simple and requires no external clocking. When the power-on/reset command is given to the CFTP, the Configuration Controller will be loaded from the RADHARD SPROM via the Master Serial Mode, with no controller required. As an additional option, the Processor FPGA can be daisy chained in Slave Serial Mode and loaded from the same SPROM. Figure 6 depicts the Master-Slave Serial Mode as used in the CFTP.

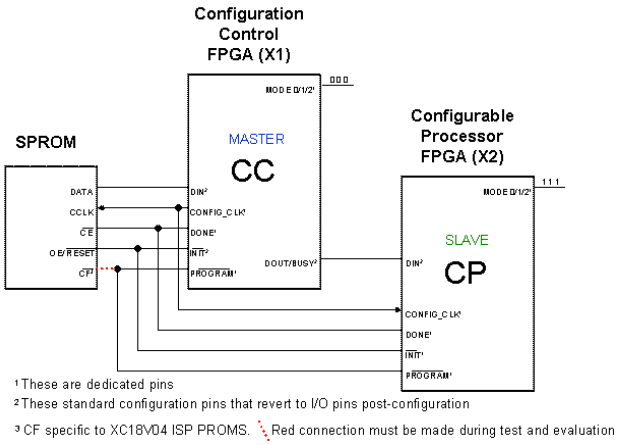

Figure 6. Master Slave Serial Mode.

Project Status

The Configurable Fault Tolerant Processor (CFTP) project has led to the design of two different Prototypes, one for each manifested spacecraft. For the Naval Postgraduate School's NPSat1, the CFTP Printed Circuit Board (PCB) is housed within the spacecraft's Command and Data Handler (C&DH). For the U.S. Naval Academy's MidSTAR-1, the CFTP PCB is augmented with a Power Supply Board and a Communications Interface Board. The CFTP PCB which is the core of each experiment has been designed and is currently in fabrication. The flexibility of a design where all of the functionality is implemented as softcores in FPGAs has serious implications on the test process.

The test process must include developmental tests of the hardware, and environmental tests of the entire experiment.

Development Tests

Development Tests are intended to verify the physical and electrical performance of the CFTP components. These tests will be performed at ambient temperature and pressure conditions. This will provide a baseline prior to subjecting CFTP to the required environments. Additional Development Tests will be conducted and compared to the baseline results during and after Environmental Testing to determine the impact of the environments on CFTP.

In developing a System-On-a-Chip (SOC) that would maximize support for dynamic mission requirements and maintain reliability while on-orbit, CFTP has been designed with a wide variety of data paths between components and made to support an array of configurations. This extreme flexibility presents some challenges in designing Development Tests. Every data path and the functionality of each possible configuration must be exercised. Each component possesses specific tasks it must be able to accomplish. At a minimum, the physical connections between components must be correct in order for these tasks to be possible and functional tests must be designed to examine these physical connections. These portions of the Development Tests will confirm the correct implementation of the CFTP design. Additionally, the interconnect between components must be such that they can perform their intended tasks correctly. While they may be physically wired according to the design, whether the design allows the intended operations must be confirmed. This portion of the Development Tests will confirm the CFTP design itself. This building block approach will validate the Prototype design and reduce the risk involved in committing designs to fabrication of Flight models.

The other major component of functional testing are the memory tests, which will verify the correct operation of the RAM, ROM, and EPROM on the board. These tests will include both destructive (to the contents) and non-destructive tests to verify memory connection and proper operation.

Each of these tests can be conducted via a self-test routine that can be stored locally on the PCB or uploaded via the PC104 Bus. The CFTP configuration can be such that the self-test routine runs automatically upon power-on/reset or when commanded. In order to test the PC104 Bus interface, identical RAM and ROM tests can be run again this time passing command and status via the PC104 Bus. Any failures identified now and not previously, can be attributed to the PC104 Bus connections.

Hardware functionality.

To complete the Development Tests, the functionality of the components must be proven as follows:

Confirm ROM correctly stores and passes the configuration for the configuration controller FPGA.

Confirm RAM correctly stores and passes data to and from the configurable processor.

Confirm EEPROM correctly stores and passes configuration(s) to and from the configurable processor.

Confirm PC104 Bus correctly passes data to and from the CFTP PCB.

Operational Tests

Once the Development Tests result in each component being correctly connected and functioning properly, Operational Tests can be conducted. These tests will mimic the specific missions defined to meet the CFTP program objectives. In order to evaluate the TMR softcore design to mitigate bit errors in computations (both detection and correction), inject errors within the Configurable Processor and confirm the detection and correction of the error. And in order to demonstrate CFTP's reconfigurability, reconfigure the configurable processor via EEPROM and PC104 Bus.

Environmental Tests

The objective of Environmental Testing is not necessarily to duplicate the space environment, but to approach it sufficiently so that any unit that passes the tests will operate successfully in its designed space environment. The major features of the space environment that need to be simulated are high vacuum, solar radiation, particle radiation, and extreme temperatures. Each of these features is incorporated into a specific environmental test. Successful completion of these tests verifies that the unit will survive the launch and it will operate properly in space.

Subjecting the CFTP PCB to the Environmental Tests will evaluate the suitability of its design in numerous space environments. The Thermal Vacuum Test will evaluate CFTP's ability to function in a given range of temperatures while under a space vacuum. The Random Vibrations Test will evaluate CFTP's ability to function after being subjected to given levels of random vibrations. The Shock Test will evaluate CFTP's ability to function after being subjected to given shock loads. The Electromagnetic Interference Test will evaluate CFTP's susceptibility to and emission of electromagnetic interference. The parameters for these various Environmental Tests are based on levels from the Launch Vehicle, a Delta IV rocket, and propagated to CFTP through the respective spacecrafts.

Additionally, Radiation Tests will evaluate the suitability of CFTP's design in numerous radiation environments in order to test its susceptibility to SEUs and Total Dose Tolerance through radiation exposure.

Conclusions

The design of a complex system, without knowing what functions it will perform in the future, and therefore not truly knowing what the necessary architecture should be designed to, is a challenging problem. By simply maximizing system flexibility by including reconfigurability options, as well as selecting the most advanced and reliable parts available, this system offers the necessary architecture to demonstrate fault tolerance and reconfigurability in the space environment.

The on-orbit reconfiguration concept stands to provide the space industry, and particularly the military, the advantage of ensuring that electronic equipment on-orbit utilizes the most current algorithms and processors. Continued CFTP research will help contribute to improvements in space based computing systems, offering system designers reliable flexibility unavailable in the past.

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