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GALLIUM ARSENIDE DRAM MEMORY CELL DESIGN AND EVALUATION OF TEST METHODS

by

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GALLIUM ARSENIDE DRAM MEMORY CELL DESIGN AND EVALUATION OF TEST METHODS

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF ABBREVIATIONS

BFL	Buffered FET Logic
BJT	Bipolar Junction Transistor
DIP	Dual In-line Position
CLOCK	Two-Phase Non-Overlapping
CMOS	Complementary Metal Oxide Semiconductor.
COUNTER	Eight Stage Counter
DAS	Data Address Strobe
DCFL	Direct-Coupled FET Logic
DECODDRVER	DECODER Driver Circuit
DECODER	One-Of -Eight Decoder
DRAM	Dynamic Random Access Memory
DRDY	Data Ready Circuit
DREFRESH	DRAM Refresh Circuit
DRVRPAD	Driver Pad Circuit
ECL	Emitter Coupled Logic
EXPD	Even Bit X Pull-Down Signal
EXPU	Even Bit X Pull-Up Signal
FET	Field Effect Transistor
fF	Femto Farad
GaAs	Gallium Arsenide
IC	Integrated Circuit
LED	Light Emitting Diode
MBSY	Memory Busy Circuit
MOS	Metal Oxide Semiconductor
μs	Microsecond
ns	Nanosecond
ps	Picosecond
NMOS	N-Type Metal Oxide Semiconductor
OUTPUT	Output Logic Circuit
OXPD	Odd Bit X Pull-Down Signal
OXPU	Odd Bit X Pull-Up Signal
PADRCVR	Pad Receiver Circuit

RAM	Random Access Memory
SBFL	Superbuffer FET Logic
SDFL	Schottky Diode FET Logic
Si	Silicon
UBFL	Unbuffered FET Logic
V_{DS}	Drain-Source Voltage Differential
V_{EE}	ECL Component Power
V_{GS}	Gate-Source Voltage Differential
V_{REFB}	Bitline Pre-charge Reference Voltage
V_{REFD}	Dummy Cell Pre-charge Reference Voltage
V_{RVREF}	Receiver Pad Reference Voltage
V_{SS}	Termination Voltage for ECL Testbench and GaAs Substrate Voltage
V_T	Threshold Voltage
WRITEP	Operation Priority Logic Circuit

I. INTRODUCTION

This thesis follows a series of four theses concerning a Gallium Arsenide (GaAs) based Dynamic Random Access Memory chip (DRAM). Christopher Vagts [Ref. 1] developed a single bit, 8 address, capacitor-based storage cell and dynamic memory architecture. Michael Morris [Ref. 2] incorporated four of the above cells for a 32 bit array and developed the support structure to enable the reading and writing of data to the memory cell. Requirements for refresh, synchronization and command conflicts were addressed as well as the requirement for the cell to interface with a silicon based test structure. The following two theses developed this test structure. Michael Butler [Ref. 3] first designed a 6-layer emitter-coupled logic (ECL) based testbench around the requirement to read and write to each of the of the 32 bits. Later, Byron Ginter [Ref. 4] continued the work of Butler by refining the design and fabricating the testbench.

An introduction to the 32 bit DRAM is presented with a summary of subsystem characteristics. Basic operation of the capacitor-based storage cell follows. The fundamental operation and characteristics of the testbench are explained as well as the methodology for system verification. Results show that although functional, the testbench fails to meet criteria for DRAM testing leaving the current DRAM chip unverified. Recommendations are given for future testbench design and fabrication. The later chapters focus on design improvements to the DRAM storage cell. Specifically, a n-type, depletion mode diode proves to be a viable storage device offering superior charge storage and maintenance characteristics when compared to similarly sized capacitors. An emphasis on modularity shows a greater level of circuit integration in the Very Large Scale Integration (VLSI) layout. Finally, recommendations are given for future integration of the diode-based storage cell.

II. GALLIUM ARSENIDE DYNAMIC RANDOM ACCESS MEMORY

A. BACKGROUND

Memory is a critical element in most computers and is becoming more and more significant as software memory requirements grow. Historically, memory has been implemented with semiconductor, magnetic and optical devices. Memory associated with semiconductor circuits is referred to as a random-access read/write memory or RAM. Data stored in RAM is not permanent; the user has the capability of changing values in the memory. RAM is also volatile. That is, if power is removed, any data in the RAM is lost. RAM comes in two basic varieties, Static RAM (SRAM) and Dynamic RAM (DRAM). Static RAM as the name suggests is memory that remains valid until the value is changed or power is removed. Dynamic RAM however, requires that the memory be periodically rewritten. The underlying reason is that the memory cell is basically a charge storage device, like a capacitor, and will slowly lose its charge. If these storage devices are not recharged, the charge will slowly drain off the device and the data will be lost. This rewriting procedure is referred to as a refresh. Most Dynamic RAMs are manufactured using Metal Oxide Semiconductor (MOS) technologies whereas Static RAMs incorporate Complementary Metal Oxide Semiconductor (CMOS). Not only are Dynamic RAMs less expensive to fabricate than Static RAMs, they offer considerable savings in the number of transistors required to build a memory element. SRAMs on average require five to six transistors to complete a memory cell where DRAMs require only one transistor and a capacitive element. The low cost and high level of integration make the DRAM the predominate memory device with today's microprocessor. Unfortunately, the speed advances in Silicon (Si) Dynamic RAMs has not been as great as Silicon SRAMs. Therein lies the motivation to find new fabrication methods and materials for Dynamic RAMs that achieve or exceed the speed characteristics found in SRAM components. The incorporation of Gallium Arsenide (GaAs) into transistor fabrication attempts to build the fast, low cost, low power DRAM circuit. [Ref. 5]

B. GALLIUM ARSENIDE TECHNOLOGY

Gallium Arsenide (GaAs) is a compound semiconductor consisting of valence 3, gallium, and valence 5, arsenic, elements. This combination of the elements yields a high electron drift mobility and improved transconductance. GaAs transistors are classified as Metal Semiconductor Field Effect Transistors (MESFET) and distinguish themselves from Si Metal Oxide Semiconductor Field Effect Transistors (MOSFET) from the construction of the transistor. In GaAs transistor fabrication, the gate metal is deposited directly on the n-channel GaAs active implant. The gate-semiconductor junction creates a Schottky-barrier diode which becomes the basis for all GaAs transistor operation. [Ref. 6]

GaAs transistors have been in use for digital integrated circuits (IC) since the 1960's. They came into fashion as an answer to applications requiring very high speed logic without the delay and power requirements of silicon CMOS or bipolar integrated circuits. Other advantages enjoyed by GaAs implementation include short gate propagation delays, a five to one advantage over Si in Power-Delay Product (power dissipated x propagation delay) and a higher resistance to radiation (lower single event upset occurrence). The main disadvantage in using GaAs transistors is the high ratio between input/output delays and logic propagation delays, which must be taken into account when designing GaAs ICs and systems. Another disadvantage to GaAs fabrication is its relatively low circuit integration. Although GaAs designs have followed MOS like circuit design topologies and silicon like process techniques, their level of integration and complexity lag behind the levels of today's silicon circuit technology. Nevertheless, GaAs circuit integration has progressed to the point where it is now becoming a viable solution to DRAM improvements. GaAs technology, like Si, has evolved from circuits using mostly n-type enhancement/depletion mode transistors to circuits using complementary transistors. When GaAs DRAM research was initiated at NPS, the use of p-type GaAs transistors was precluded because of the low mobility of holes (250 $cm^2/(V\text{-}s)$) and low barrier height (0.45 eV) of most metals on p-type GaAs. Today however, complementary GaAs fabrication has improved mobility and increased barrier heights to allow integration into some circuits. [Ref. 7]

C. GALLIUM ARSENIDE LOGIC FAMILIES

Like silicon-based circuits, GaAs circuits can be designed using enhancement mode transistors, depletion mode transistors or a mixture of the two. The main property that distinguishes the high-speed GaAs FET from NMOS and CMOS circuits is the forward-bias gate conduction resulting from the use of a Schottky barrier formed by the GaAs gate over the n-channel. The n-channel FETs also have an inherent high transconductance relative to p-channel GaAs FETs due to the higher electron mobility and electron drift velocity. Depletion mode (normally-on) GaAs FETs are characterized by having a V_T less than zero. Logic circuits using these depletion FETs exhibit characteristics of having unequal input and output voltage levels. V_{GS} must be negative to turn off the transistor, while V_{DS} must remain positive. These circuits offer characteristics of higher noise margins and higher fan-out but suffer from higher power dissipation and current levels. Circuits using Enhancement/Depletion mode GaAs FETs, on the other hand, carry smaller current levels since the enhancement FET requires only one power source. The small logic swing from 0 V to 0.7 V provides high speed when combined with high intrinsic transconductance. [Ref. 7]

The depletion mode logic families incorporated in the design include Unbuffered FET Logic (UBFL), Buffered FET Logic (BFL), and Schottky Diode FET Logic (SDFL). Enhancement mode logic families incorporated include Direct-Coupled FET Logic (DCFL) and Superbuffer FET Logic (SBFL). Choice of a particular logic family is based on the logic operation, noise margin requirement, fanout, power consumption and size. Specific detail pertaining to the logic families can be found in the work presented by Morris. [Ref. 2]

D. GALLIUM ARSENIDE ONE-TRANSISTOR RAM CELL

The basis for research on the GaAs DRAM is a one-transistor RAM cell incorporating a capacitor for maintaining charge. This particular cell was chosen as the result of the research by Christopher Vagts. [Ref. 1] This study compared various three and one cell arrangements and compared charge storage and maintenance, sensitivity, refresh, timing, simulation and layout. Charge storage and maintenance in GaAs transistor

structures are adversely affected by secondary effects of subthreshold current and substrate leakage currents. Subthreshold current is the residual leakage current that flows from source to drain when V_{GS} is biased more negatively than V_T. Substrate leakage current is leakage through the substrate which occurs due to injection of a charge from a forward biased contact. [Ref. 7] The advantages of the one-transistor cell over other designs include less power consumption due to fewer transistors, smaller second-order effects, a simpler refresh circuit and higher scale integration. A diagram of this model can be seen in Figure 2.1.

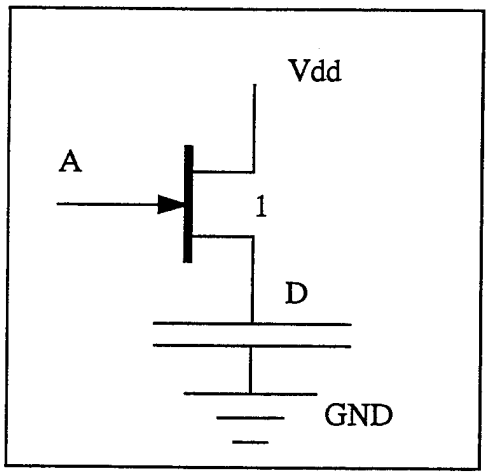


Figure 2.1. One Transistor RAM Cell with a Capacitor.

To complete the cell, pull-up and pull-down transistors are added to support the logic criteria for read and write operations. Transistor 1 and the capacitor act together as

the memory cell. Transistors 2 and 3 support logic to read or write to the cell, as seen in Figure 2.2.

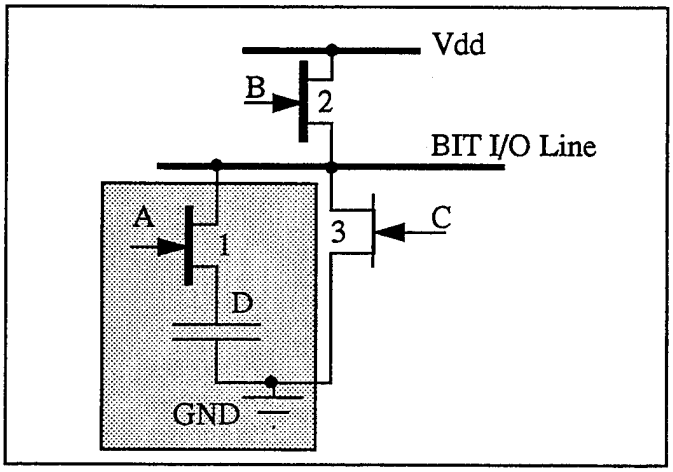


Figure 2.2. Single Cell with Read/Write Support.

To Write a ONE (high), the gates at nodes B and A are simultaneously pulsed, which turn on transistors 2 and 1. This opens a circuit from VDD through transistors 2 and 1 to charge the capacitor at node D. To Write a ZERO (low), the gates at nodes C and A are pulsed, which turn on transistors 3 and 1, creating a circuit from GND through transistors 3 and 1 to the capacitor at node D. The open path to GND discharges the capacitor.

To Read the charge at node D requires that both the pull-up transistor (transistor 2) and the pull-down transistor (transistor 3) are off. The Bit Input Output (BIO) line must also be at a low potential. Transistor 1 is then turned on by pulsing the gate at node A so that the voltage potential at D is connected to the Bit Input Output line. It is significant to note that the BIO line need not be fully discharged prior to reading. A small drop or increase in potential is sufficient to indicate a ZERO or ONE respectively.

E. SENSE AMPLIFIER

As previously mentioned, a read is accomplished by sensing the potential drop or increase on the BIO line. The sense amplifier accomplishes this task. The design incorporated in the memory follows standards from Si architecture using n-channel metal oxide semiconductor (NMOS) technology and enhancement-depletion mode transistors. Using five transistors, the sense amplifier measures changes on the BIO lines and quickly

pulls the BIO line to the respective level. The sense amplifier plays a critical role in the speed of the memory circuit. Because the transistors inside the cell are small and the capacitance of the BIO line large, pulling down the line takes a significant amount of time. The sense amplifier speeds up the read operation by amplifying the change in potential. The sense amplifier used in the DRAM is illustrated in Figure 2.3. [Ref. 2]

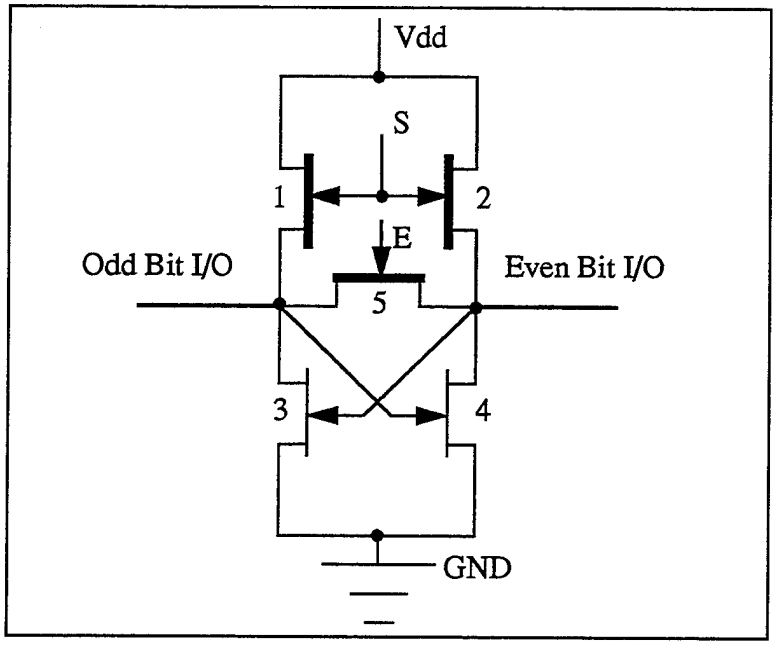


Figure 2.3. Sense Amplifier After Ref. [2].

The timing of the circuit is very important. Ideally, the sense amplifier will operate if the cell and sense transistors come on at the same time. This scheme, however, does not allow the BIO lines to be unbalanced strictly by the stored charge. The problem that results may include a fictitious read. To solve this problem, various high-level circuits to include a two-phase non-overlapping clock are required to allow for the delayed clock to the sense transistors. The drawback to the high-level support structures is a dramatic increase in power consumption. The following section outlines the high-level circuits.

F. GaAs DRAM HIGH-LEVEL CIRCUITS

The DRAM incorporates 12 high-level circuits used to facilitate read, write and refresh operations as well as to establish precedence in commands and perform the necessary conversion from ECL to GaAs logic levels. The high-level circuits include a

CLOCK, DECODER, DECODDRVR, DREFRESH, WRITEP, COUNTER, OUTPUT, WLOGIC, and pad drivers/receivers. Each high-level circuit is briefly described in this section. Block diagrams are contained in Appendix A. Complete descriptions, schematic, transient analysis, power dissipation and general comments can be found in the work by Morris. [Ref. 2]

1. Two-Phase Non-Overlapping Clock (CLOCK)

The development of the two-phase non-overlapping clock was a result of the need to equalize bit-lines and pre-charge dummy cells and bit-lines, as well as to activate sense transistors for read and write operations. The clock also required a level shifting operation due to the use of depletion mode transistors in the memory cell and other high-level circuits. The circuit accepts a single square wave input, 50% duty cycle signal of 0.06V to 0.63V. The specific outputs of the CLOCK circuit include the original signal phase one (PH1), a phase one level shifted from -1.2V to 0V (PH1L), an inverted signal phase two (PH2), a time delayed phase two (PH2D), and a time delayed and level shifted phase two signal (PH2LD). [Ref. 2]

2. One-Of-Eight Decoder (DECODER)

The one-of-eight decoder is a support circuit to decode address lines. The circuit is purely combinatorial. Inputs include the three address lines and three enable lines. Outputs include the separate control lines for each address as well as a single enable line. [Ref. 2]

3. Eight Stage Counter (COUNTER)

The counter performs the sequential selection of address lines in the refresh operation and is incorporated in another high-level circuit DREFRESH. The counter begins with logic 000 and cycles up to 111 to complete the cycle. The overall speed of the refresh cycle is in part limited by the speed of this COUNTER which is dependent on the DCFL glue logic gates used in the design. Inputs include the external clock and an enable. Outputs include counter values Q0 through Q2. [Ref. 2]

4. DRAM Refresh Circuitry (DREFRESH)

This circuit monitors the external refresh signal. The overall DRAM itself does not monitor the status of the charge in the individual memory cells, nor does it initiate a refresh cycle on its own. The circuit as previously mentioned, incorporates the COUNTER and by sequentially activating each memory address performs a successive READ operation to each bit. Each of the four bits at a particular address are refreshed simultaneously, allowing for a complete refresh to occur in as little as eight clock cycles. Inputs include phase one clock PH1, address lines (A0, A!, A2) and the external refresh signal (REFRESH). Outputs include refresh address lines (A00, A01, A02) and internal refresh signal (MREFRESH). [Ref. 2]

5. Decoder Driver Circuit (DECODDRVER)

This circuit provides synchronized signals to the memory cell to accomplish Read and Write Operations. Among the required signals control signals for Even and Odd Bit line Dummy Cells, (EDUM, EDUMD and ODUM, ODUMD) as well as the control lines to the memory cell sense transistors (DX0 to DX7) respectfully. Obviously, each bit requires its own decoder driver for a total of four in the design. Inputs include three address lines (A0,A1,A2), and internal read, write and refresh commands (MREAD, MWRITE, and MREFRESH). [Ref. 2]

6. Output Logic Circuitry (OUTPUT)

The OUTPUT circuit accomplishes the read of the appropriate bit-line in the memory cell. Inputs include an internal read command (MREAD), (EDUM and ODUM) dummy cell signals as well as odd and even bit-line control signals (ODDBIO and EVENBIO) respectfully. The output includes the data out bit-line and its complement (DOX, /DOX). [Ref. 2]

7. Operation Priority Logic Circuitry (WRITEP)

This circuit establishes command priority to the external refresh signal, REFRESH, followed by the external write signal, WRITE. The external read command, READ, has

lowest precedence. Inputs include REFRESH, WRITE and READ. Outputs include internal refresh, write and read commands (MREFRESH, MWRITE, and MREAD) respectively. [Ref. 2]

8. Memory Busy Circuitry (MBSY)

This circuit sends a MBSY signal to the output pad during any refresh, write or read operation. Inputs include MREFRESH, MWRITE and MREAD and outputs include memory busy signal (MBSY). [Ref. 2]

9. Data Ready Circuitry (DRDY)

This circuit provides a (DRDY) signal for data availability. The signal becomes de-asserted only during read operations. Inputs include even and odd dummy control signals (EDUM and ODUM) as well as an internal read command (MREAD). Output is DRDY. [Ref. 2]

10. Write Logic Circuitry (WLOGIC)

WLOGIC provides the control signals to pull-up and pull-down transistors at the appropriate address to enable the write of a one or a zero to the appropriate bit. Inputs include all Data bit lines (DX), data strobe (DAS), given address line (AX), internal write command (MWRITE) and inverted clock signal (PH2). Outputs include the appropriate bit pull-up and pull-down control signals (EXPU, EXPD, OXPU, OXPD). [Ref. 2]

11. Pad Receiver Circuit (PADRCVR)

Provided by S. Long and D. Fouts, this circuit receives an external ECL signal and converts it to DCFL logic levels for the internal circuits. [Ref. 2]

12. Driver Pad Circuit (DRVRPAD)

Complementary to the Pad Receiver, the Driver Pad accepts a DCFL logic signal and converts it to ECL logic levels. Again, this design the work of S. Long and D. Fouts. [Ref. 2]

The next chapter will discuss the test bench designed for the GaAs DRAM and address its functionality.

III. PRINTED CIRCUIT BOARD TEST BENCH

A. TEST METHODS FOR GaAs DRAM

With the development of the GaAs DRAM came the need to functionally test the memory array. The DRAM pads were designed to accept Emitter-Coupled Logic, ECL, signals. ECL is the fastest silicon-based, commercially available and economically feasible technology. Local test devices lacked the capability of generating command, data, clock and refresh ECL signals up to a required 250 MHz. To meet the requirement for functional testing, Michael Butler and Byron Ginter developed a test platform based on design attributes of the GaAs DRAM incorporating ECL components [Ref. 6]. The major guiding issues to the testbench included:

- The physical characteristics of the GaAs DRAM including: a 32-bit memory consisting of eight address locations with four bits at each address; individual input pads for Data Address Strobe, Read/Write commands, Receiver Reference Voltage (RVREF), Bitline Reference Voltage (VREFB), Dummy Cell Reference Voltage (VREFD), Substrate Reference Voltage (SUB) and Input Clock (INCLK); individual output pads for Data Ready (DRDY) and Memory Busy (MBSY) control lines as well as multiple input pads for DRAM power (-2.0V) and Ground (GND).

- All pads on the DRAM interface to external logic by means of emitter-coupled logic.

- , All lines are required to be terminated utilizing transmission line interconnect techniques due to the signal edge rates and speed. The standard used for ECL termination is 50 ohm termination to -2.0 volts

- The testbench is required to test each data bit storage cell by writing data to a given address and then reading the data bit back out of the DRAM.

- The testbench should be a printed circuit board of minimal size utilizing surface mount technology (SMT) capable of achieving signal speeds up to 250 MHz.

•To achieve the clock speed necessary to adequately test the DRAM, the fixture must contain dedicated signal planes for high speed interconnect. These impedance controlled signal planes must be bounded on the top and bottom by either power (AC ground) or ground planes to reduce crosstalk and reflections. [Ref. 4]

To better understand the testbench platform, a brief description of ECL devices is in order.

B. EMITTER-COUPLED LOGIC

Emitter-Coupled Logic (ECL) is the fastest silicon-based logic circuit family. The technology essentially incorporates a bipolar junction transistor (BJT) differential pair current switch. The switch operates in the ohmic region keeping logic swings to about 0.8 volts and reduces the time required to charge and discharge load and parasitic capacitances. A popular form of ECL circuits is produced by National Semiconductor in their F100K 300 series. The 300 series meet the performance standards set by 100 and 200 series but also reduce power dissipation up to 50%. They operate with a supply voltage of (-4.2V to -5.7V) and have electrostatic discharge protection. The F100K features gate delays that are typically 0.75 ns and dissipate only 19mW/gate. [Ref. 8] The basic configuration of the ECL switch is given in Figure 3.1.

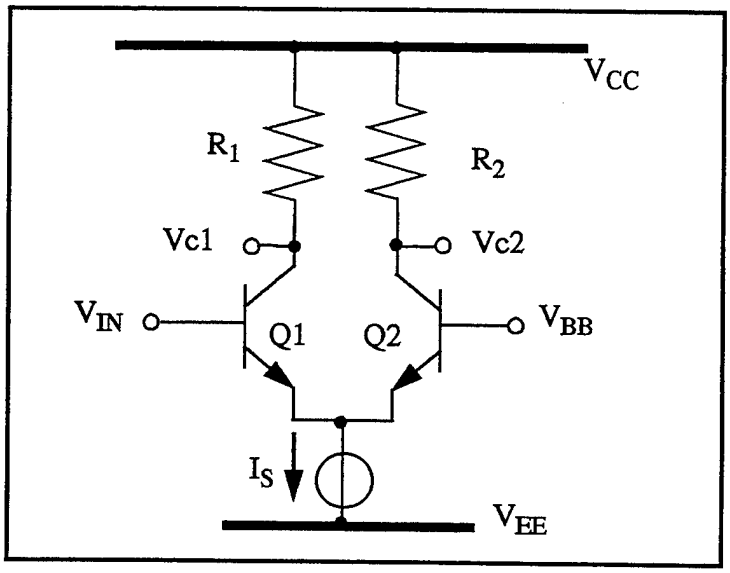


Figure 3.1. Basic ECL Switch After Ref. [8].

The switch operation begins with both base voltages V_{IN} and V_{BB} equal. In this case current flows equally between Q1 and Q2. An increase in voltage at V_{IN} by 0.125 mV causes all the current to flow through Q1. A decrease in voltage at V_{IN} causes all the current to flow through Q2. Therefore, a voltage swing of 250 mV enables the switching function. An additional voltage swing increase to 700 mV provides added noise margin. The series 300 components use negative voltages for the logic levels (-0.9 V = LOGIC '1') and (-1.6 V = LOGIC '0'). Power supplies to the components include 0V as V_{CC} and -4.5 to -5.2 V as V_{EE}. Since the switch works at speeds up to 250 MHz, secondary effects consisting of crosstalk and transmission line effects play a critical part in design. The following paragraph briefly describes the nature of the problem and solution.

C. TRANSMISSION LINE EFFECTS

The combination of short signal rise times and relatively long signal propagation times cause the phenomenon known as transmission line effects. When utilizing F100K Series 300 ECL components, signals have characteristic rise times of 0.2 ns. The signal in the printed circuit board however only travels about half the speed of light or 15 cm/ns. For this environment, problems occur because energy that reaches the end of the transmission line is not absorbed but is reflected to the transmitting end. The result is a 'ringing' or damped oscillatory signal about the final signal value. Given a 0.2ns rise time and assuming a 15 cm/ns signal propagation, a signal can travel six cm before encountering interfering oscillatory reflections. Therefore, the maximum distance between components would be 3 cm [Ref. 6]. Printed circuit board properties prohibit a 3 cm placement between all components and require that the signals be absorbed at the receiver components to prevent reflection. To achieve absorption, the transmission lines must be 'terminated' at the receiving end in a resistance equal to the line's characteristic impedance. The terminating resistor of matching impedance preserves the ratio of voltage to current and therefore retains the original signal and does not produce reflections. The following paragraph further illustrates the importance and reasons for maintaining the voltage to current ratio in the circuit.

Within the circuit board, signal lines and ground lines are used to connect various ECL components and the GaAs DRAM. The lines are basically two conductors that each have a characteristic impedance and capacitance and constitute a transmission line. The impedance is defined as the ratio of the transient signal voltage to the transient signal current and is expressed by equation (3.1).

$$\frac{V}{I} = Zo = \sqrt{\frac{Lo}{Co}} \tag{3.1}$$

L_O = inductance per unit length in Henries, C_O = capacitance per unit length in Farads, and Z_O = is impedance in Ohms. [Ref. 8] The following model helps to further illustrate the phenomenon Figure 3.2.

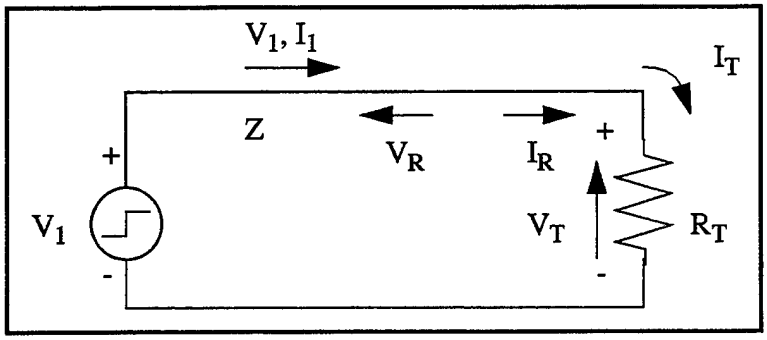


Figure 3.2. Termination and Reflection From Ref. [8].

The initial current is determined by V_1, the voltage step in the signal, and Z_O, the characteristic impedance of the transmission line, but the final steady state current is determined by V_1 and R_T, transmission line termination resistance. If the ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T, a reflected wave will be generated to satisfy Ohm's law. A nodal analysis shows only one voltage can exist. Equation (3.2) defines the voltage at the terminating resistor.

$$V_1 + V_R = V_T \tag{3.2}$$

therefore current through the terminating resistor is

$$I_T = \frac{V_T}{R_T} = \frac{V_1 + V_R}{R_T} \tag{3.3}$$

while the original and reflected currents are respectively

$$I_1 = \frac{V_1}{Z_0} \qquad I_R = -\frac{V_R}{Z_0} \tag{3.4}$$

solving for V_R, the reflected voltage signal

$$\frac{V_1}{Z_0} - \frac{V_R}{Z_0} = \frac{V_1 + V_R}{R_T} \qquad V_1 \times \left(\frac{1}{Z_0} - \frac{1}{R_T}\right) = V_R \times \left(\frac{1}{Z_0} + \frac{1}{R_T}\right) \tag{3.5}$$

$$V_R = V_1 \times \left(\frac{R_T - Z_0}{R_T + Z_0}\right) \tag{3.6}$$

Values for the terminating resistor, R_T, may range from zero (shorted line) to infinity (open line). Equation (3.6) illustrates that when R_T is equal to Z_O, the matched impedances cancel any reflecting current, I_R, since V_R goes to zero. [Ref. 8] The characteristic impedance derived by Butler [Ref. 3] was dependent on the board material, trace width and thickness, and interground plane distance and calculated out to 50 ohms. Surface mount hardware availability forced the use of type 1206, 51 ohm terminating resistors. [Ref. 4] The small difference in impedance between design criteria and actual hardware had no significant effect on operation or transmission line effects.

D. EMMISSIONS

Other major concerns with high speed signals are emission losses and signal interference. At a speed of 250 MHz the signal conductors can essentially become if emitters. The solution to emission losses and possible interference to and from external signals is to bound the signal lines by power and ground planes. This type of architecture

is known as stripling. A cross section of the test platform, six layer PCB is shown in Figure 3.3.

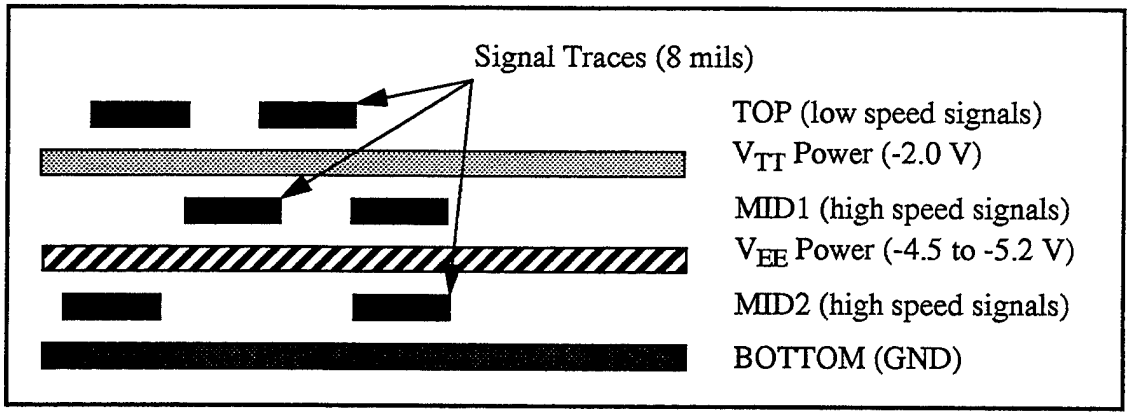


Figure 3.3. Printed Circuit Board Layer Construction After Ref. [4].

E. PRINTED CIRCUIT BOARD SYSTEMS

To achieve the test goals previously mentioned, the printed circuit board incorporated four basic systems: register, clock, control and refresh circuits. The register system was divided into three major components consisting of address registers, input data registers and output data registers. The system generated the required signals to the DRAM data and address input pads and momentarily stored a signal address data bit value. The clock system served two purposes. First, to generate clocking pulses for the synchronous operation of the ECL components. Second, to send a synchronous, 50.0% duty cycle, ECL clocking pulse to the GaAs DRAM. The clock circuit also had the capability of running without interruption in the automatic mode or could be manually switched by use of a debounced switch. The control system initiated read, write and load commands, resolved command conflicts, and ensured the memory chip was in a ready mode. The refresh system restored bit voltage levels in the individual cells on a periodic basis and could be synchronized with the clock pulse. The synchronized refresh signal was also selectable to predetermined values of refresh rate. Additionally, an external refresh port was available for an independent, unsynchronized refresh signal. All of the systems were built from six basic ECL components including a Quint 2-Input OR/NOR Gate 100302, Quint AND/ NAND Gate 100304, Low Power Quad Driver 100313, Low Power 4-Stage Counter/Shift

Register 100336 and a Low Power 8-Bit Shift Register 100341. Details of the six individual components are detailed in Appendix B. Input ports were available for a reference clock, external refresh, ground GND/VCC, power VEE, terminating voltage VTT, receiver reference voltage VRVREF, dummy cell pre-charge input VREFD, bitline pre-charge input VREFB, and negative supply for DRAM logic level shifting VSS. Figure 3.4, page 20 indicates the various system placement on the printed circuit board. A detailed schematic is also included in Appendix B.

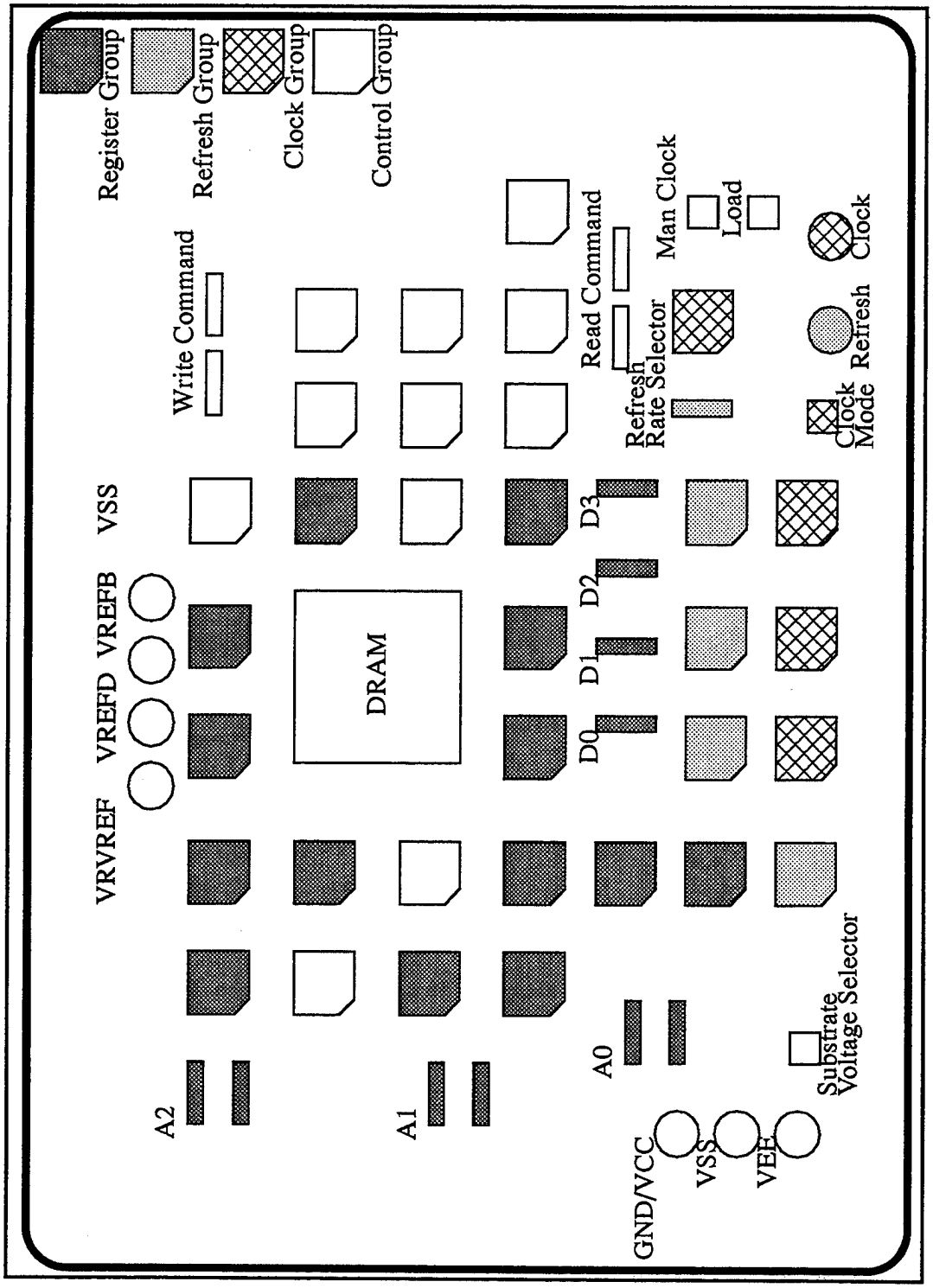


Figure 3.4. PCB System Placement.

1. Register Systems

As previously mentioned, the register system included an address group, data input group and data output group. The data input and address groups were designed in a similar fashion using two 8-Bit Shift Registers in series. Address and data bits were selectable by Dual In-Line Position, DIP, switches. By using two cascaded shift registers, all eight addresses could be selectively written to and then read from in one test sequence.

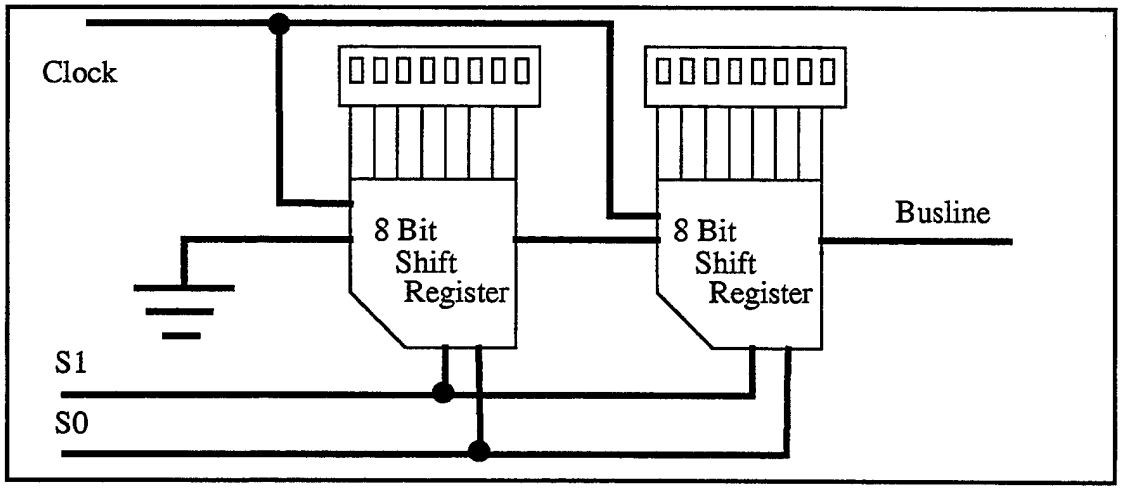


Figure 3.5. Register System.

The control of the shift registers was enabled by two signal inputs S_0 and S_1 which were generated from control system components Data Ready, DRDY, Data Address Strobe, DAS, and Read/Write commands. A partial truth table for the shift register operation is given in Table 3.1. The output registers received data inputs directly from the DRAM chip but operated on the same control inputs S1 and S0.

TABLE 3.1. Control Inputs for ECL Shift Register.

Function	S1	S0	Clock Pulse
Load	L	L	lead edge
Shift Left	L	H	lead edge
Shift Right	H	L	lead edge
Hold	H	H	X

2. Clock System

The clock system was divided into two modes, automatic and manual. The automatic mode used an external 50% duty cycle clock input at ECL logic levels (-1.6 V LOW, -0.9V HIGH). The manual mode was controlled by a synchronized, debounced clocking switch. Selection of the applicable mode was done with a similar synchronized, debounced switch. The signal was divided into four lines, one to drive the clock signal to all ECL components, a feed signal to the control group, an input to the refresh system and a clock input to the DRAM. As with the other systems, drivers were required with the clock signals since the ECL components have a fanout of 2.

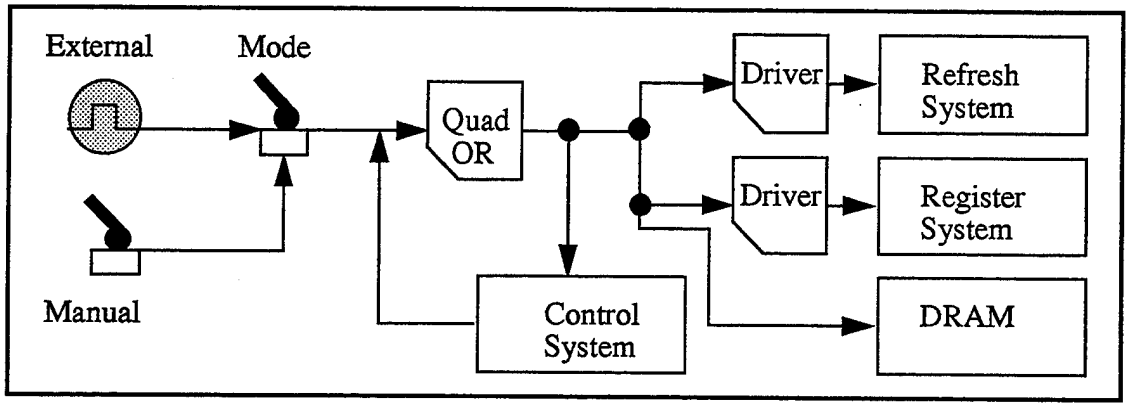


Figure 3.6. Clock System.

3. Control System

The control system provided three functions. First, it enabled READ and WRITE commands through an architecture similar to the register system. Commands were asserted HIGH and were loaded through 8 pin DIP switches to two cascaded shift registers. Second, it resolved simultaneous READ and WRITE commands and provided a Data Address Strobe DAS to the DRAM. Simultaneous commands caused register systems to revert to a hold status (S1, S0 both HIGH). Once the system entered a hold status, the only way to continue operation was to reset the entire system and reload the data. The operator had to ensure no conflicts existed between READ and WRITE commands to execute a complete cycle through all 16 command inputs. Third, the system enabled the operator to execute a load operation which initialized all registers on the circuit board. The load operation also

reset control inputs to all registers to shift right once the load function was deselected. A load operation was executed by setting the DIP switches to the desired position, selecting the load switch and then either cycling the clock mode switch to automatic or cycling the manual clock switch while in manual mode. Completion of the load function and automatic reset of control signals S1 and S0 were accomplished by deselecting the load switch. The clock mode switch had to be in the manual mode before deselecting the load switch if individual signals were to be observed. Figure 3.7 illustrates a block diagram of the control system.

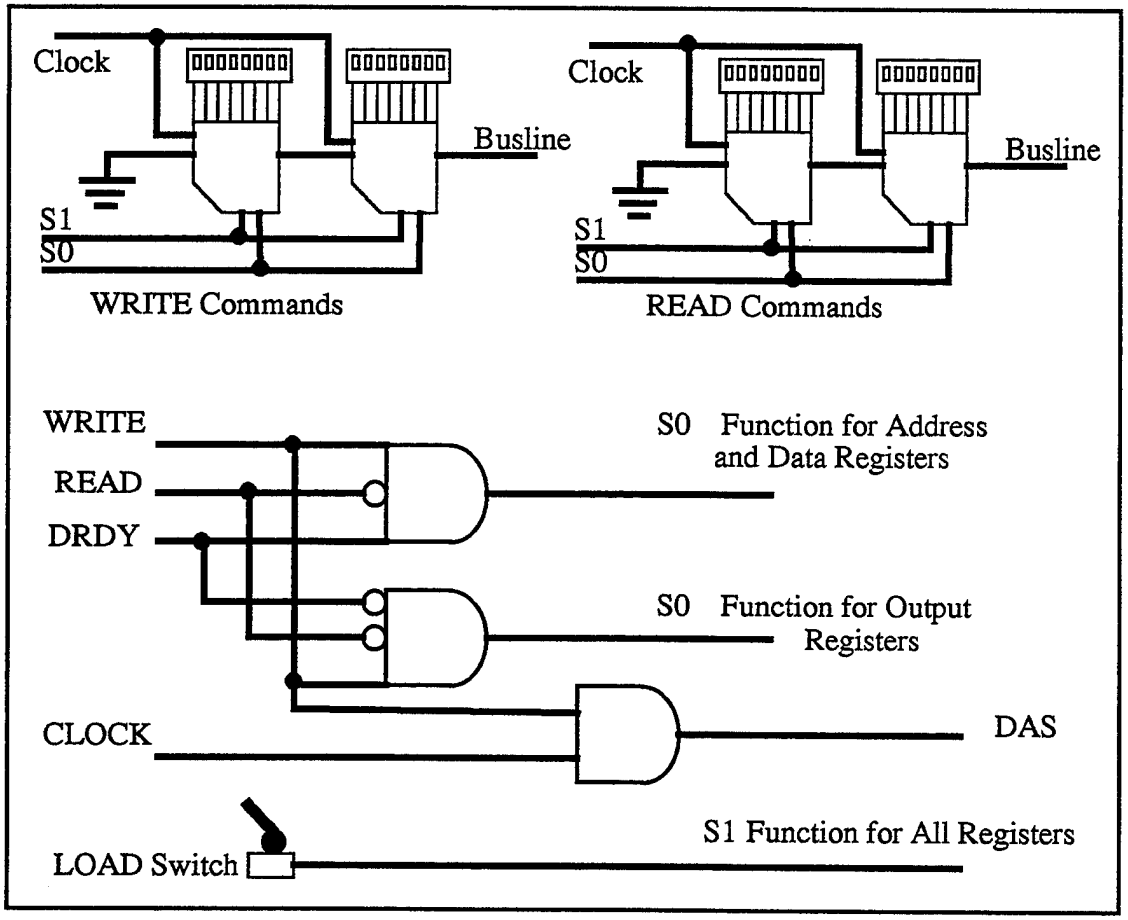


Figure 3.7. Control System.

4. Refresh System

The refresh system periodically generated REFRESH signals to the DRAM. The system had two modes, synchronous using a clock system signal and asynchronous using

an external signal. The synchronous mode generated REFRESH signals by super-scaling the clock input through the use of five cascaded 4-bit counters. The resulting 4-bit outputs were multiples of the input signal divided by 16^5. Each of the scaler outputs and the external, asynchronous REFRESH signal were routed to an 8-pin DIP switch. The outputs of the DIP were connected to a single termination resistor which allowed the selection of only one REFRESH signal at a time as shown in Figure 3.8.

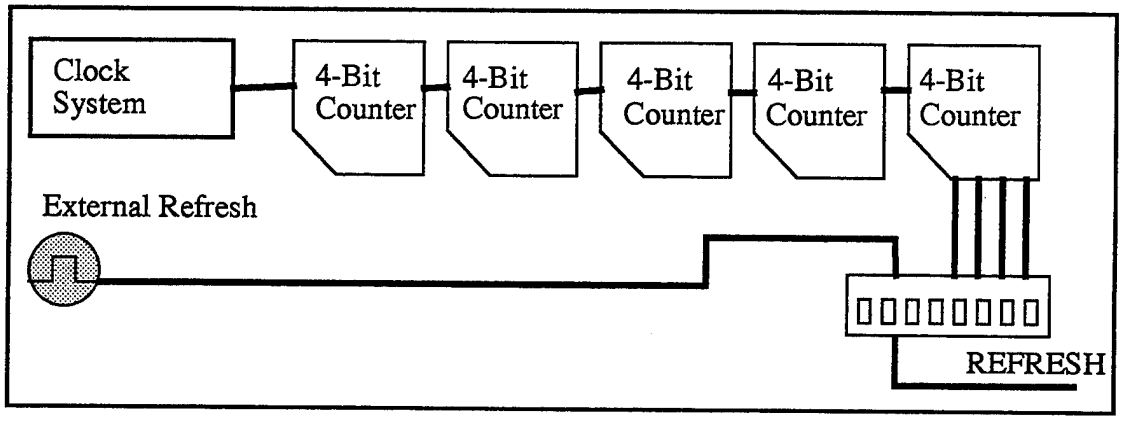


Figure 3.8. Refresh System.

F. TROUBLESHOOTING

The testing began with logic verification and basic operation of the PCB. Prior to starting two design flaws previously mentioned by Ginter [Ref. 4] were addressed. Specifically, the input pads for the system clock and external refresh signal were not equipped to handle any wire connector. Any attempt to drill holes for connectors risked the chance of damaging the connection to actual signal lines in the middle layers of the board. A coaxial wire was soldered directly to the surface of the pad and grounded to the ground plane via a jumper to the ground input pad. A SMA connector was attached to the coaxial wire and connected to a high speed signal generator. The results proved satisfactory for the clock inputs up to 100 Mhz. Clocking rates higher than 100 MHz suffered from noise and distortion due to the properties of the solder contact.

Once a working clock circuit was operating, power V_{EE}, ground V_{CC}, and termination voltage V_{TT} connections were applied but only limited parts of each system

functioned correctly. The subsequent action was a methodical step by step test for conductivity. Use of a detailed schematic was required and the only guide to the component placement on the board was the board silk screen. The approach was to correct one system at a time, first addressing power, ground, termination and clock connections and then the higher order functions. The operation of the manual clocking circuitry proved vital to the troubleshooting of the entire PCB particularly in diagnosing bad components. Pin by pin current and voltage measurements were required to track down some of the bad components and connections. Of the 1800 plus surface mount contacts over 80 pins were still unconnected due to bad solder contacts. The similarity of the ECL packages (F100K 28 pin PCC) and the similarity of the resistor/capacitor packages (RC1206 and CC1206) contributed to instances of the wrong component being soldered in place. The procedure to correctly remove a 28 pin surface mount device requires specialized equipment which the U.S. Naval Postgraduate school lacks. With the correct tool, all 28 pins are heated simultaneously allowing the chip to be lifted directly off the board. Lacking the specialized equipment, the approach used was to heat each pin one by one and vacuuming off the solder. The procedure was repeated on each contact moving around the package until the package could be lifted off from the PCB. Although all damaged and incorrect components were successfully removed and replaced, the probability for compound failures was high. The pads on the surface of the PCB become volatile at 425 degrees F. The soldering iron used operated at 700 degrees F. Although great care was taken to apply the iron to the solder connections, the heat conducted down to the pads. Specifically, during the removal process, some of the pads were inadvertently lifted off. Fortunately the pads that lifted off were 'no contact' pads and had no effect on the board operation. Had those pad been signal pads, signal integrity and board operation could have been jeopardized. The last verification was to ensure all signal lines were terminated with the proper resistor. There were only a couple of instances of resistors/capacitors missing or incorrectly installed.

G. FUNCTIONALITY

The total power consumption of the PCB components was high as expected. With 34 ECL components and over 150 terminating resistors and coupling capacitors I_{EE} current

required was 5 amps. In continual testing, the heat dissipation of the components was satisfactory and did not cause any system degradation. System logic was tested by loading address registers with each address twice and commanding read and write commands to each address. The test was conducted two times to verify both logic ZERO and logic ONE signals to the input data registers. Simultaneous commands were also tested to verify control signals for the shift registers would revert to a hold status. As for the output register group, the clock, power, termination and ground connections were functional and required a DRAM input to complete verification.

In preparation for testing the actual DRAM, the package leads were found to be on the side of the heat sink. If placed as constructed on the PCB, the heat sink would not have dissipated heat correctly and could jeopardize operation. To correct this error and retain proper pin out sequence for the chip, the leads were bent prior to cutting the leads to fit the board. Another mounting problem existed with the chip holder device designed by Ginter. The device failed to hold the leads firmly to the pads because the bracket surface contacted with the surrounding terminating resistors and coupling capacitors. A second piece of plastic had to be used to hold the leads to the board pads as shown in Figure 3.9.

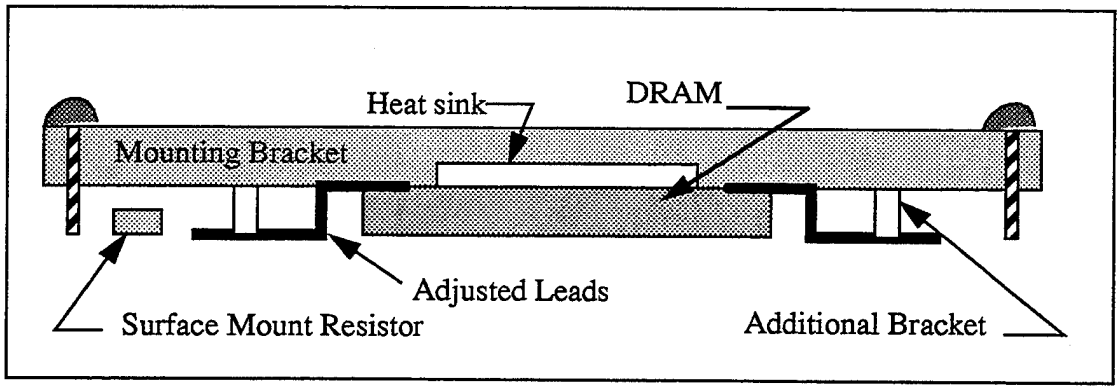
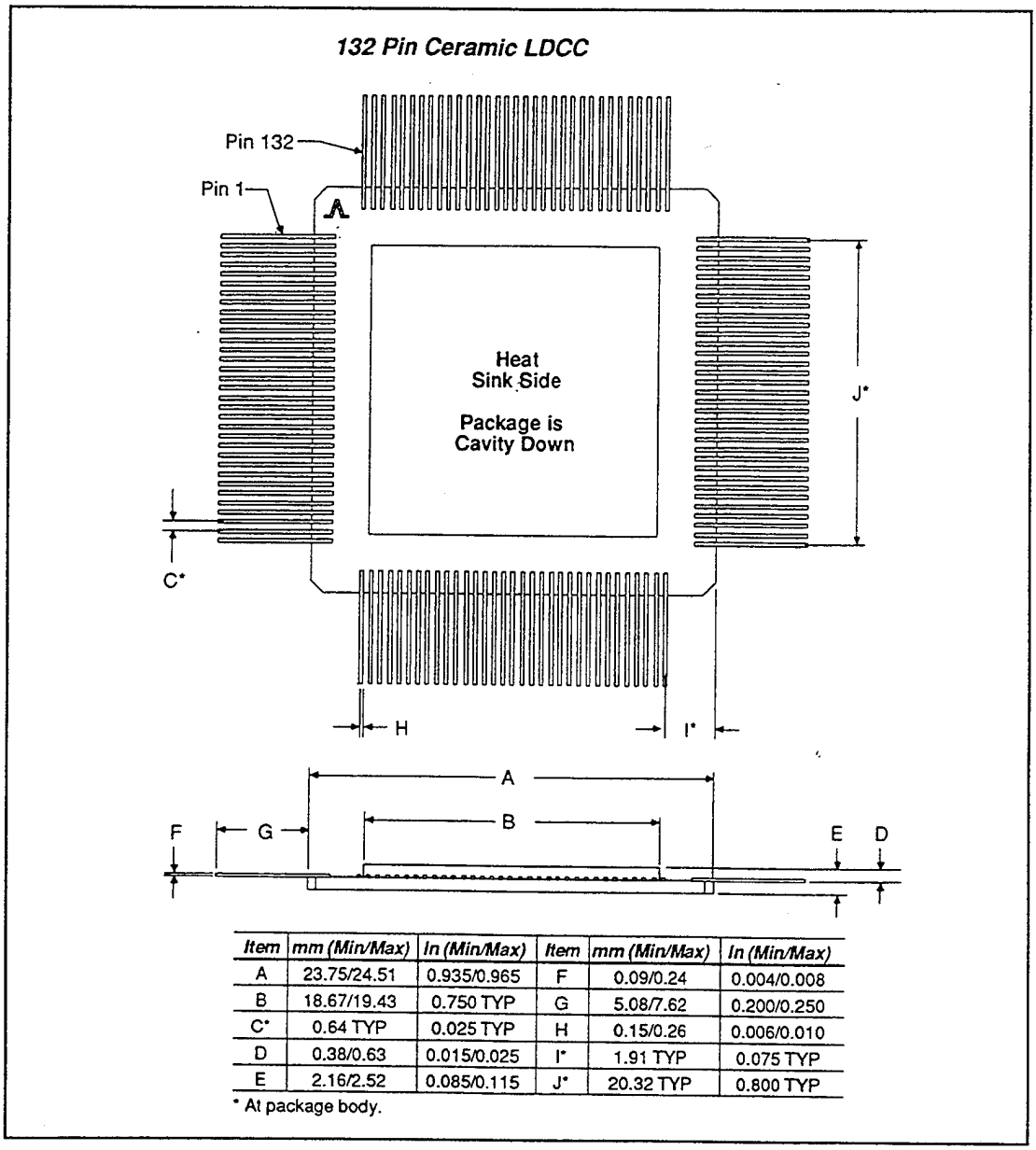


Figure 3.9. DRAM Chip Pin and Mounting Bracket Adjustment.

Once the holder was corrected the chip could be placed on the PCB. It was then that the fatal design flaw of the board was discovered.

Both Butler [Ref. 3] and Ginter [Ref. 4] documented the proper pin out of the DRAM and both included pin out orientation by Vitesse indicating pin 1 at the corner of the package as shown in Figure 3.10.



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	23.75/24.51	0.935/0.965	F	0.09/0.24	0.004/0.008
B	18.67/19.43	0.750 TYP	G	5.08/7.62	0.200/0.250
C*	0.64 TYP	0.025 TYP	H	0.15/0.26	0.006/0.010
D	0.38/0.63	0.015/0.025	I*	1.91 TYP	0.075 TYP
E	2.16/2.52	0.085/0.115	J*	20.32 TYP	0.800 TYP

* At package body.

Figure 3.10. Vitesse Semiconductor 132-Pin PLCC Package From Ref. [9].

The actual pin out orientation was that of the National Semiconductor F100K 300 series 28 pin PLCC with pin 1 centered in the package as shown in Figure 3.11.. The fault is attributed to the default pin orientation used by the TANGO PCB DESIGN software. To compensate for custom pin orientation, the pin out numbering must be specified. The only visible indication of the error is the small pin 1 identification mark in the TOP layer silk screen.

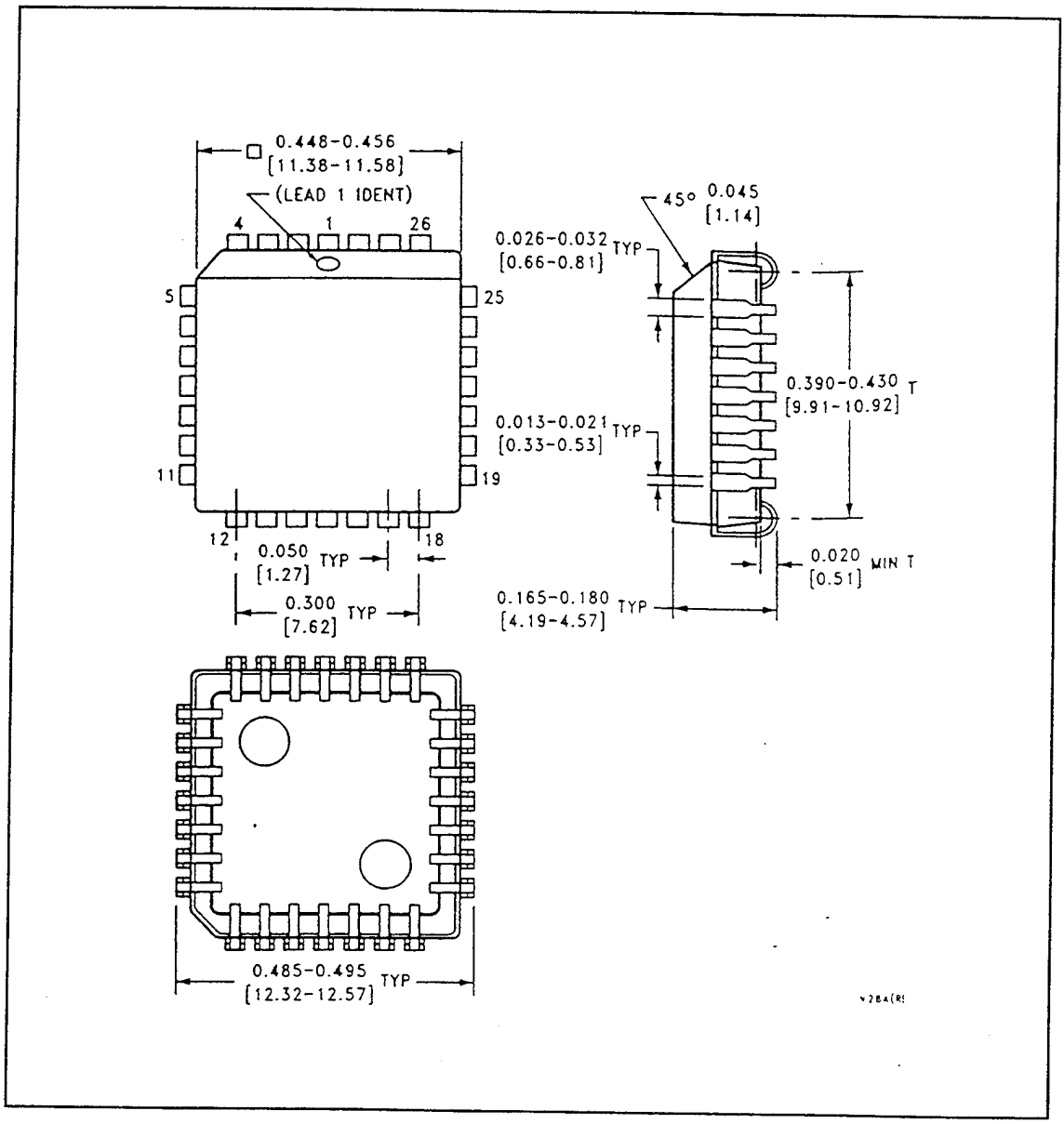


Figure 3.11. National Semiconductor 28-Pin PCC Package.

The actual PCB pin assignment is detailed in Table 3.2 page 29.

TABLE 3.2. DRAM Pin Assignment On PCB.

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	NC	34	NC	67	NC	100	NC
2	GND	35	NC	68	GND	101	D2(O)
3	DRDY(O)	36	GND	69	DAS(I)	102	NC
4	NC	37	NC	70	NC	103	NC
5	MBSY(O)	38	NC	71	NC	104	D3(O)
6	GND	39	GND	72	GND	105	NC
7	GND	40	NC	73	GND	106	NC
8	-2.0V	41	NC	74	-2.0V	107	NC
9	NC	42	GND	75	NC	108	NC
10	GND	43	NC	76	NC	109	NC
11	NC	44	GND	77	NC	110	GND
12	GND	45	-2.0V	78	GND	111	-2.0V
13	-2.0V	46	GND	79	NC	112	GND
14	NC	47	NC	80	NC	113	NC
15	GND	48	A1(I)	81	GND	114	NC
16	-2.0V	49	NC	82	NC	115	NC
17	NC	50	GND	83	NC	116	GND
18	RVREF	51	INCLK	84	NC	117	NC
19	GND	52	NC	85	GND	118	NC
20	GND	53	GND	86	GND	119	GND
21	-2.0V	54	D0(I)	87	-2.0V	120	VSS
22	NC	55	NC	88	NC	121	NC
23	WRITE(I)	56	D1(I)	89	NC	122	VREFB
24	READ(I)	57	GND	90	-2.0V	123	GND
25	NC	58	GND	91	NC	124	GND
26	NC	59	-2.0V	92	NC	125	-2.0V
27	REFRESH(I)	60	NC	93	D0(O)	126	NC
28	NC	61	D2(I)	94	NC	127	VREFD
29	NC	62	NC	95	NC	128	NC
30	A2(I)	63	GND	96	D1(O)	129	GND
31	NC	64	D3(I)	97	NC	130	NC
32	GND	65	NC	98	GND	131	NC
33	SUB	66	A0(I)	99	-2.0V	132	NC

IV. PCB IMPROVEMENT RECOMMENDATIONS

Although the PCB ultimately proved to be unusable, many lessons were learned during the testing that will contribute to future designs. Specifically, this chapter addresses recommendations that will improve the ease of assembly, repair, testing and functionality of new designs.

The first recommendation is to use the Cadence CAD suite in future PCB designs. The Cadence PCB application 'Allegro' is an industry standard and is compatible with all PCB manufacturers. Butler [Ref. 3] and Ginter [Ref. 4] utilized TANGO. Although fairly robust, the program lacked the ability to support multiple ground planes and lacked significant design rule checking. Errors in pad design were detected by the PCB manufacturer and corrected. Additionally, the newer versions of TANGO could not interpret older versions of PCB designs. Any redesign was forced to start at square one. The PCB designer, Allegro, within the Cadence CAD suite is available at the Naval Postgraduate School. The associated schematic editor, Concept, allows for circuit layout and offers a robust library of components of various package types. The accompanying tutorial makes Concept fairly easy to use. The Rapid Part Designer within Concept can be implemented for custom packages as in the DRAM or future chips. There is no requirement during the circuit layout phase for exact package dimensions, only package pin numbering is required. Net lists generated by the schematic editor can be imported to the PCB application to facilitate signal line connections and verify logic. The PCB designer allows for custom design of pads and stacks as well as footprints for SMT components. The PCB designer however, requires the exact dimensions of components as well as fabrication house requirements for pad swell, thermal relief sizes and anti-pad sizes.

The second recommendation is to verify the availability of components and minimum order size prior to fabricating the PCB. Ginter [Ref. 4] was not able to order some of the required components because of the order size and was forced to substitute components. The DIP switches used did not fit the pad footprint designed in the PCB. The

adjustment of the leads resulted in several bad and shorted connections. Designing with future high speed PCBs with exact component dimensions will ensure signal integrity.

The components used in future designs should be in a DIP package and mounted to the board with a DIP connector. National Semiconductor offers its F100K series 300 in a 24 pin DIP package. Since the Naval Postgraduate School lacked the ability to individually test 28 pin PCC components, each 28-pin component was soldered to the test platform without being tested. Using DIP packages, components could be easily plugged into the DIP connector easily and would facilitate the removal of bad components. Although there is a slight increase in package footprint and design rule distances for through-board vias, the ease of exact placement of the component, assured electrical connection as well as easier removal/replacement process make DIP components a better package in prototype designs. The space savings of SMT components are good for commercial sized production but are not conducive to the test and evaluation environment.

Additional refresh signal inputs are recommended to allow for a wider range of refresh values. Instead of porting just the last scaled signals to the refresh selector, signals from each of the three preceding scalers could be ported to a DIP switch allowing selection of a faster refresh rate. The faster refresh rates will allow testing of DRAMs with lower charge maintenance characteristics.

All high speed inputs to the PCB should incorporate SMA connector padstacks. As previously mentioned, the clock and refresh pads lacked integrated wire connectors and therefore suffered interference from the solder connection. The SMA coaxial wire connectors produce low noise/interference and generate minimal signal losses.

Future designs should continue the incorporation of a manual clock. Without control of individual clocking pulses, the operator has limited to no ability to troubleshoot circuits or verify functionality of the test equipment. Use of the debounced SPDT toggle was adequate and should also be incorporated in new designs.

The incorporation of some type of light emitting diode, LED, would have greatly facilitated reading logic levels on the data and address busses. Incorporating seven segment diodes for large memory array test platforms would enable quick reading of the address and

data buses as well as for the output data registers. The LEDs would require a separate power source on the PCB and would increase the size of the board. Granted, the individual will not be able to read the diodes when working with the automatic clock, but LEDs will greatly help in recording logic levels when using the manual clock.

Care should be taken when placing terminating resistors, capacitors and other components to allow for the use of a clamp or mount to hold the chip and its leads to the PCB. Allegro allows for the use of "keep-outs" which protect board area from signal line and component placement.

At this point of the research came the question to continue with testing and develop a completely new PCB or follow the initial research outline and design a follow-on memory cell. The decision was to continue memory cell design and verify whether using a diode as a memory storage device was a viable alternative to capacitor-based cells. The following chapters describe the design, simulation, layout and integration of the diode-based storage device.

V. DRAM MEMORY CELL IMPROVEMENT

The approach to cell improvement considered four aspects of the memory cell, charge storage, power consumption, speed and chip area. Previous work in the development of the cell lacked the use of HSPICE in the initial selection of storage cell types.The many benefits of using HSPICE in modeling GaAs circuits include superior convergence and more accurate modeling due to better approximations of GaAs secondary effects namely substrate voltage and leakage voltage. [Ref. 10] Vagts [Ref. 1] realized late in his work that the diode could be a possible contender for the premier storage device but did not pursue the analysis. This chapter investigates this possibility with comparisons to the present memory cell.

A. CAPACITIVE STORAGE CELL

Recall that the current memory cell is a single transistor cell that uses a capacitor as the charge storage device as seen in Figure 5.1.

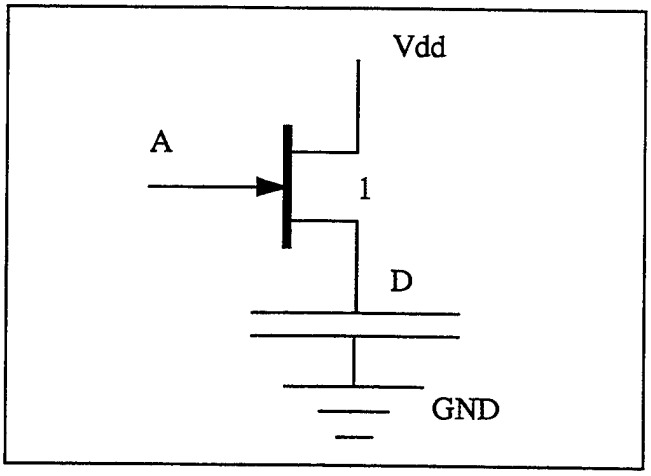


Figure 5.1. One Transistor RAM Cell with Capacitor.

Chip capacitors have an unfortunate property of occupying large areas in the VLSI design. For the present design, the capacitor was constructed using parallel plates that occupy a 52μm by 52μm area (2704 μm^2). Using GaAs, the designer has the ability to use up to four different layers of metal as well as gate metal. In the Vagts cell, three layers of metal

in addition to gate metal were incorporated. A cross sectional illustration of the capacitor cell is depicted in Figure 5.2.

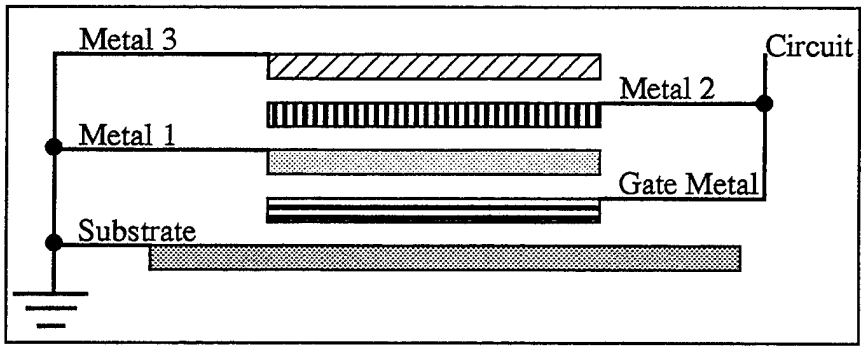


Figure 5.2. Capacitor Layout After Ref. [7].

An accurate evaluation of this multilevel metal configuration is not trivial. However, because of the large amount of multilevel metal layering in VLSI designs a simple closed-form solution is required. By applying an approach of 'primitive' structures, designers can achieve accurate estimations. The three capacitive components to any multilevel metal structure include line-to-ground, line-to-line and crossover capacitances. [Ref. 11] A simple evaluation of the capacitance for VLSI capacitors, treats the metal layers as infinitesimally thin parallel plates where the width of the plate is much greater than the distance above the ground plane given by Equation (5.1). [Ref. 12]

$$C = \frac{\varepsilon \times w}{h} \times \left[1 + \frac{2 \times h}{\pi \times w} \times \left(1 + \log\left(\frac{\pi \times w}{h}\right)\right)\right], \frac{w}{h} > 1 \qquad (5.1)$$

The result is a capacitance that accounts for just parallel plate and fringing capacitances. The approach underestimates the capacitance because it does not take into account the thickness of the plates. However, the error for the approximate formula is less than 5%. Calculation of the total capacitance is done by adding the parallel plate

capacitances using the following values in TABLE 5.1 for interlayer parallel and fringing capacitances.

TABLE 5.1. Vitesse Interlayer Capacitances After Ref. [10].

Top Layer	Bottom Layer	Parallel Plate Capacitance (fF/micron^2)	Fringing Capacitance (fF/micron)
Metal 3	Metal 3	0.051	0.048
Metal 3	Metal 3	0.033	0.035
Metal 3	Metal 3	0.028	0.030
Metal 3	Ohmic Metal	0.028	0.030
Metal 3	Substrate	0.022	0.035
Metal 2	Metal 1	0.073	0.049
Metal 2	Gate Metal	0.050	0.045
Metal 2	Ohmic Metal	0.050	0.045
Metal 2	Substrate	0.32	0.042
Metal 1	Gate Metal	0.127	0.051
Metal 1	Ohmic Metal	0.127	0.051
Metal 1	Substrate	0.052	0.044
Gate Metal	Substrate	0.076	0.045

A quick expression to evaluate capacitance C based on the fabrication structure previously illustrated together with Vitesse values is:

$$C = 0.675 \times L^2 + 1.06 \times L \qquad (5.2)$$

Measuring the parallel plates as 52μm square structures yields a total capacitance of 1880fF per cell.

B. DIODE STORAGE CELL

Unlike a silicon based MOSFET, the gate electrode in a GaAs MESFET is formed by depositing a metal, refractory metal silicide, or refractory metal nitride, directly on an

n-type GaAs channel. This pn junction however is quite different from silicon pn junctions. In GaAs, the majority carriers (electrons) provide the conduction current and reverse saturation current. The relative absence of minority carriers give the diode a low diffusion capacitance and provide for fast charge and discharge. Using the diode in a reversed-biased application of a pn junction yields a capacitive effect with nonlinear properties with respect to applied voltages. The nonlinearity suggests that a smaller diode may be used to provide the same capacitive effect of a larger capacitor.

Using the geometric size of a 1880fF capacitor as a constraint, enhancement and depletion type diodes were first evaluated and compared to the original capacitor. A diode is constructed simply by connecting the source and drain regions of the transistor to the sense transistor and connecting the gate of the transistor to ground. This creates a reversed biased Schottky diode. The diode and sense transistor pair create the basic one transistor memory cell as depicted in Figure 5.3.

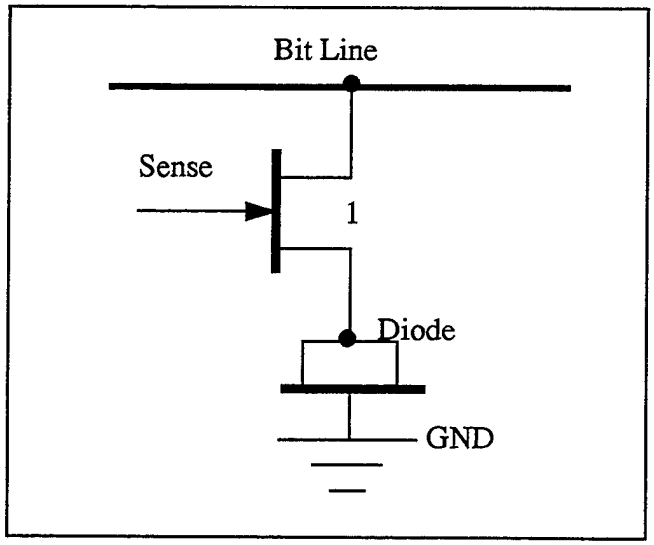


Figure 5.3. One Transistor RAM Cell with Diode.

The first simulations compared charge storage abilities of similarly sized enhancement and depletion n-type diodes. The enhancement diode exhibited unsatisfactory charge storage capabilities as shown in Figure 5.4.

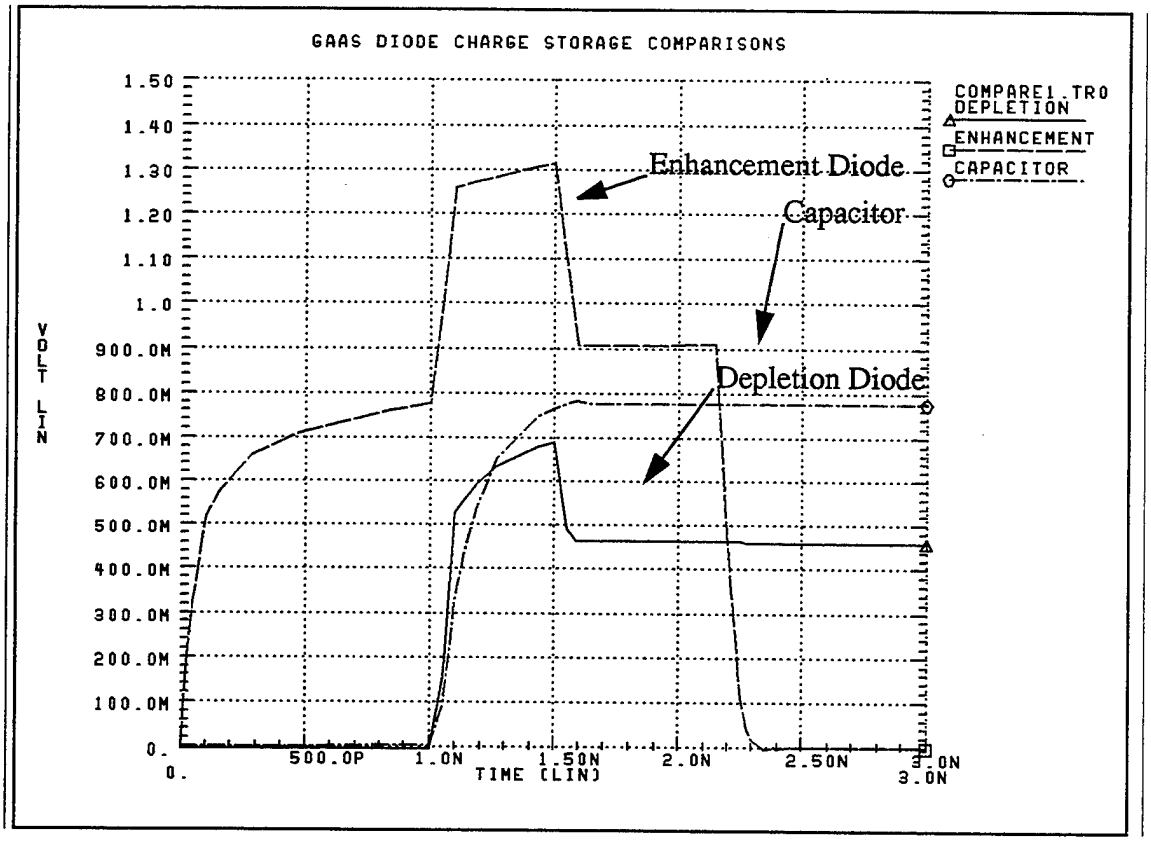


Figure 5.4. Diode Type Comparisons.

As expected, the enhancement diode charged faster and higher than the depletion diode but then rapidly lost its charge. The depletion diode charged at a comparable rate to the capacitor but failed to retain as high a charge as the capacitor. Specifically, once the charging voltage was discontinued, both diodes leaked a large portion of the original charge back through the sense transistor as it was turning off. The efficacy of the diode cell depends on as much charge as possible be maintained in the cell. To prevent or limit this discharge phenomenon, the approach was to lengthen the gates of the sense amplifier to reduce the transistor's transconductance. The next series of experiments tested this approach. Starting with an arbitrary depletion diode cell (gate length 10μm and a gate width

of 50μm), the sense transistor gate lengths were varied from minimum length (0.8μm) to an arbitrary value of 30μm. Results of the tests indicated a trade-off between the initial charge of the diode and the charge maintenance. Converse to expectations, the reduced transconductance of the sense transistor did not mitigate the initial charge drain and adversely affected the charging of the diode as shown in Figure 5.5.

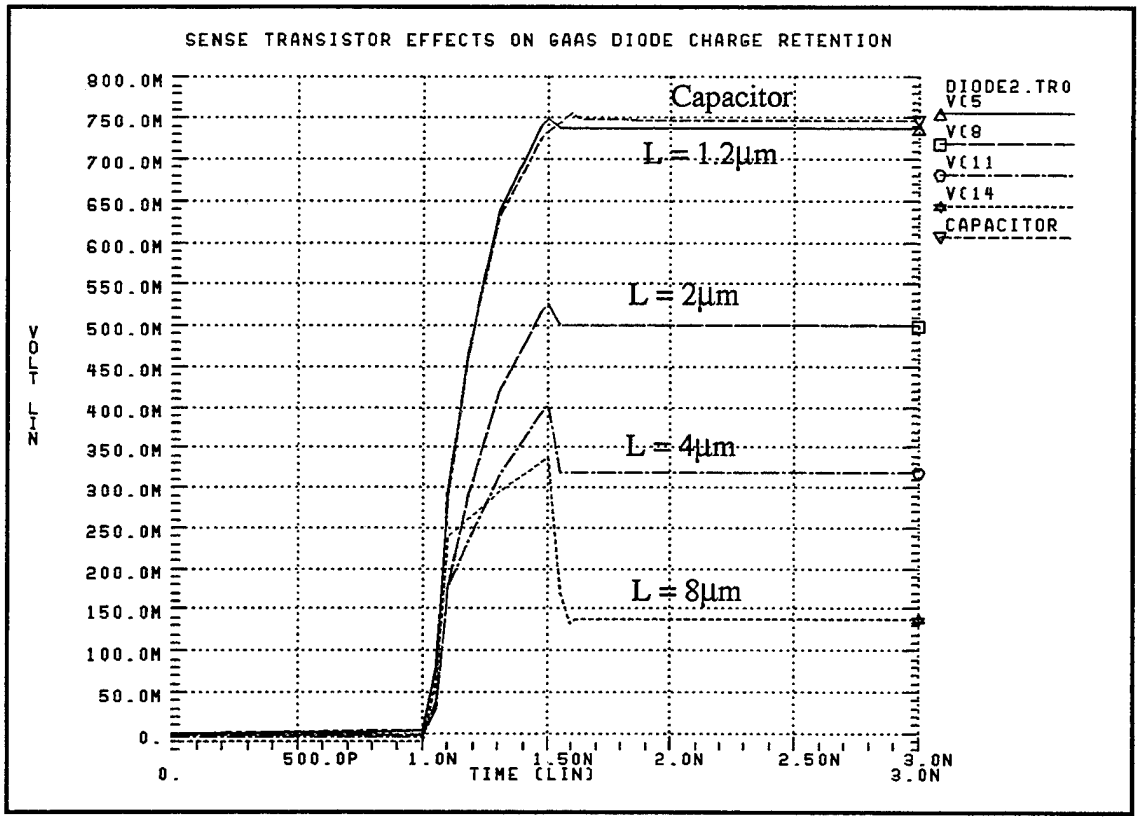


Figure 5.5. Sense Transistor Effects on Initial Charge.

However, the sense transistor did play a significant role in the charge retention of the diode. Specifically, the gate length was proportional to quality of charge maintenance. The sense transistor with a gate length of 1.2μm made our diode comparable to the

capacitor. The sense transistor with a gate length of 2μm clearly became a superior configuration for duration times exceeding 1μs seen in Figure 5.6.

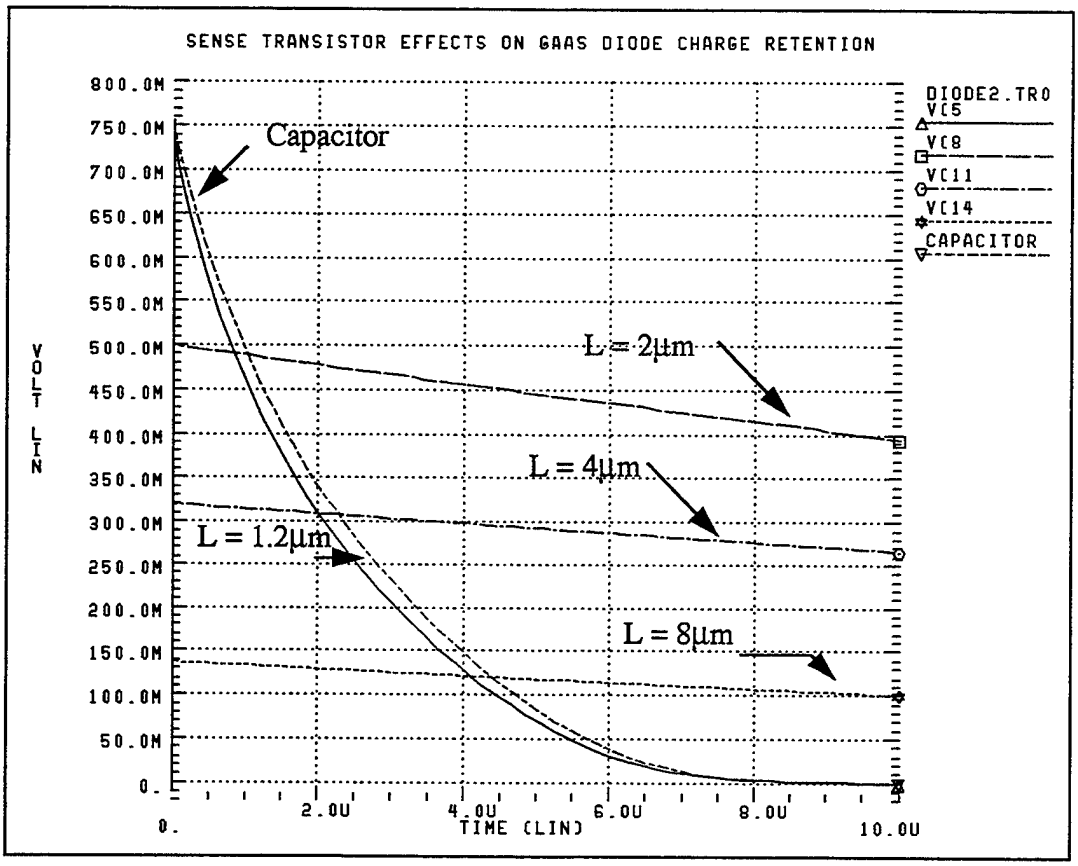


Figure 5.6. Sense Transistor Effect on Charge Retention.

The next approach was to vary the depletion diode gate lengths to improve charge maintenance. Using a sense transistor previously developed, simulations were performed on memory cells with depletion diode gate lengths varied from minimum size 0.8μm to 42μm. 42μm was chosen as a limit to the geometric size of the diode. Although the capacitor in the cell designed by Vagts was 52μm square, the maximum size of the diode was limited to 42μm to take into account minimum design rule sizing. Specifically, gate metal overlap must be 0.8μm, minimum active area is 2.0μm and minimum ohmic metal width 2.4μm are some of the constraints. Using a 42μm diode the storage cell final size equaled the capacitor size of 52 square microns. The simulations on the different gate lengths presented a trade off between read/write times and initial charge levels in the

memory cells. Since read/write times remain fixed, the initial charge values were inversely proportional with gate length. Figure 5.7 indicates that diode gate lengths less than 34μm exhibited better initial charging than the capacitor storage cell.

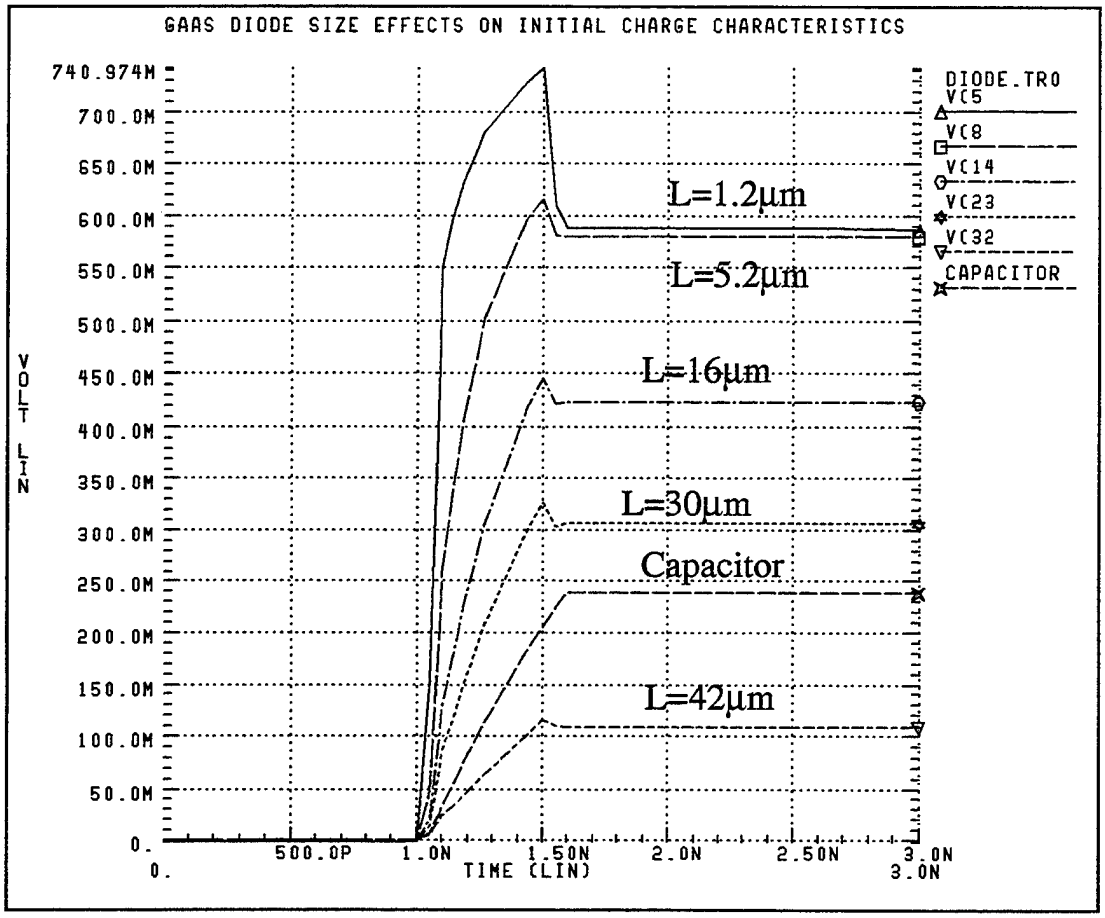


Figure 5.7. Diode Gate Length Effects on Initial Charge.

The next simulation compared the diode gate length charge maintenance characteristics. The results indicate that the diode storage devices tend to have a flat discharge slope compared the exponential decay of the capacitive cell. The quick charge and relatively flat discharge slope suggest that the GaAs diode used in a reversed biased application display nonlinear capacitive characteristics. The charge maintenance characteristics increased dramatically for gate lengths up to 30μm. After 30μm, the cost-benefit of charge maintenance starts to be outweighed by the size of the component. A comparison to the original capacitor cell illustrates the benefits of the diode cell approach

shown in Figure 5.8. Based on the results, a 30μm diode was selected as the storage device and was used in the development of memory cell support.

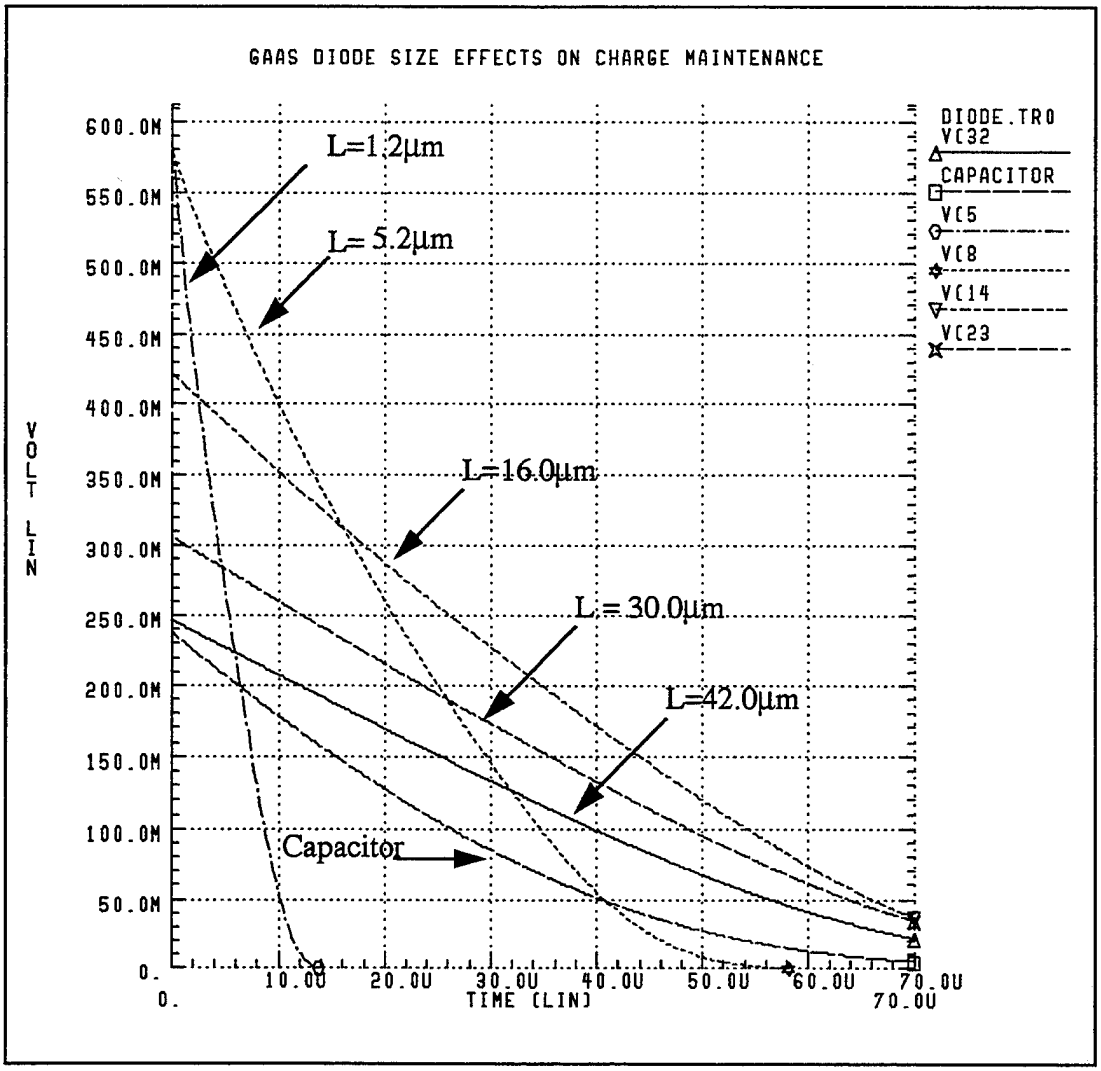


Figure 5.8. Diode Gate Length Effects on Charge Maintenance.

C. SUPPORTING CIRCUITS

Support circuitry is required to enable read and write operations as well as improve the speed. Like the original cell, this cell incorporates a structure based on circuits presented by Foss and Harland. [Ref. 13] In this arrangement, pull up and pull-down transistors provide for the read and write of a logic value ONE and ZERO respectively. But, in addition to read and write support, a sense amplifier is needed to reduce the time for the

read/write operations and pre-charge support is needed to preserve memory cell voltages and prolong refresh cycles.

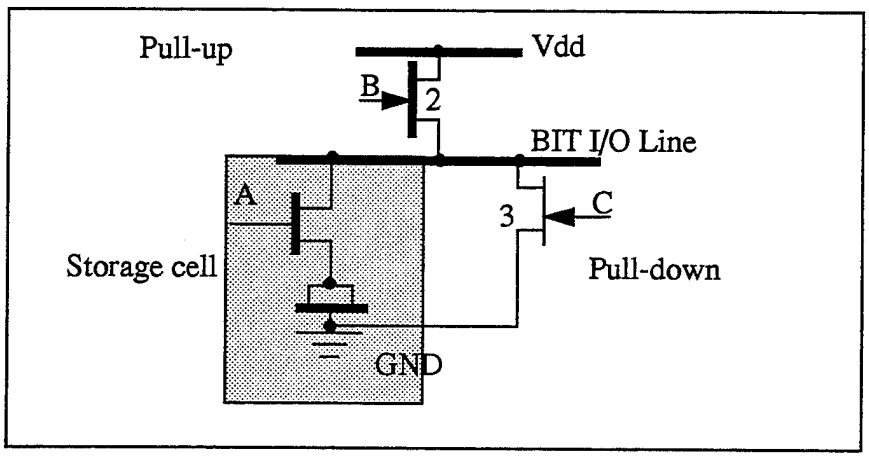


Figure 5.9. Memory Cell with Read Write Support.

1. Sense Amplifier

The goal was to reduce the size of the sense amplifier without affecting the speed of operation. The development of a clamped-bit-line sense amplifier proved effective in achieving sub-nanosecond response times in silicon circuits. The key to this approach was to isolate the bitline capacitance to a node that had minimal effect on the speed of the circuit. [Ref. 13] This approach was not suitable for a design upgrade since the number of transistors grew from 5 to 11. The next approach was to investigate relationships between size of the sense transistors and pull-up transistors in the sense amplifier. Gate sizes of the transistors were reduced to 0.8μm and simulations proved smaller transistors were faster although power consumption increased slightly. Further simulations found the ideal

dimensions for the individual transistors. Figure 5.10 illustrates the sense amplifier construction.

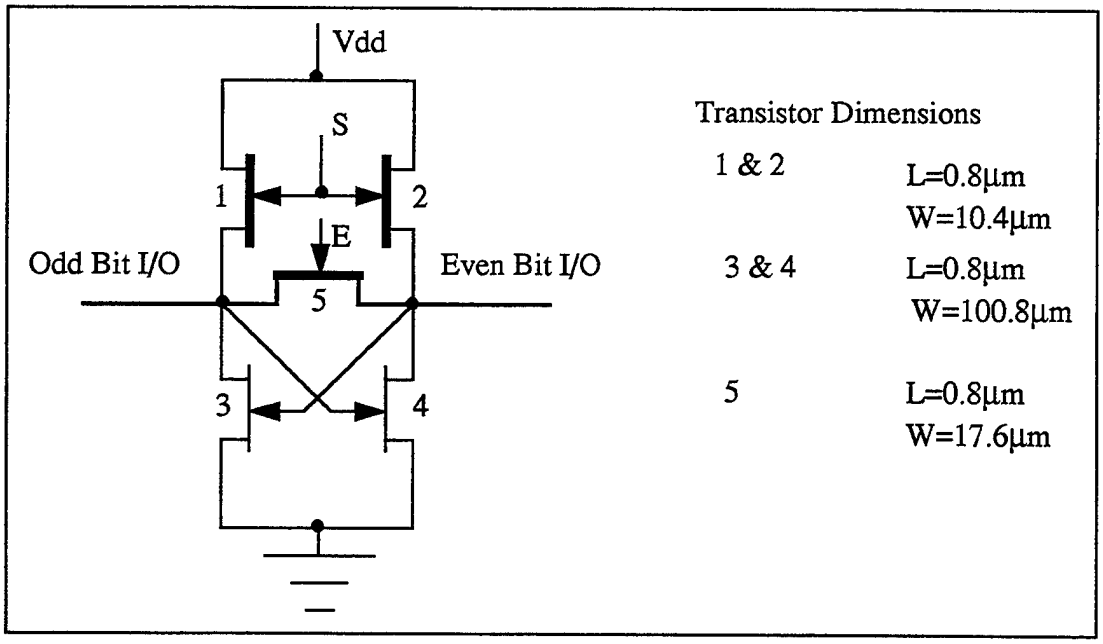


Figure 5.10. Sense Amplifier.

In Figure 5.11 on page 46, a logic ONE has previously been stored in a memory cell and is now read. The sense amplifier detects the small difference in voltage levels between the memory cell and its associated dummy cell and pulls the bitline associated with the memory cell to the full logic ONE level while the compliment bitline is pulled to the opposite level or ZERO logic. The simulation, using a 666MHz clock, requires 4mW

of power during the READ operation. Simulations were conducted at both 25 and 85 degrees Centigrade with negligible differences in power and time readings.

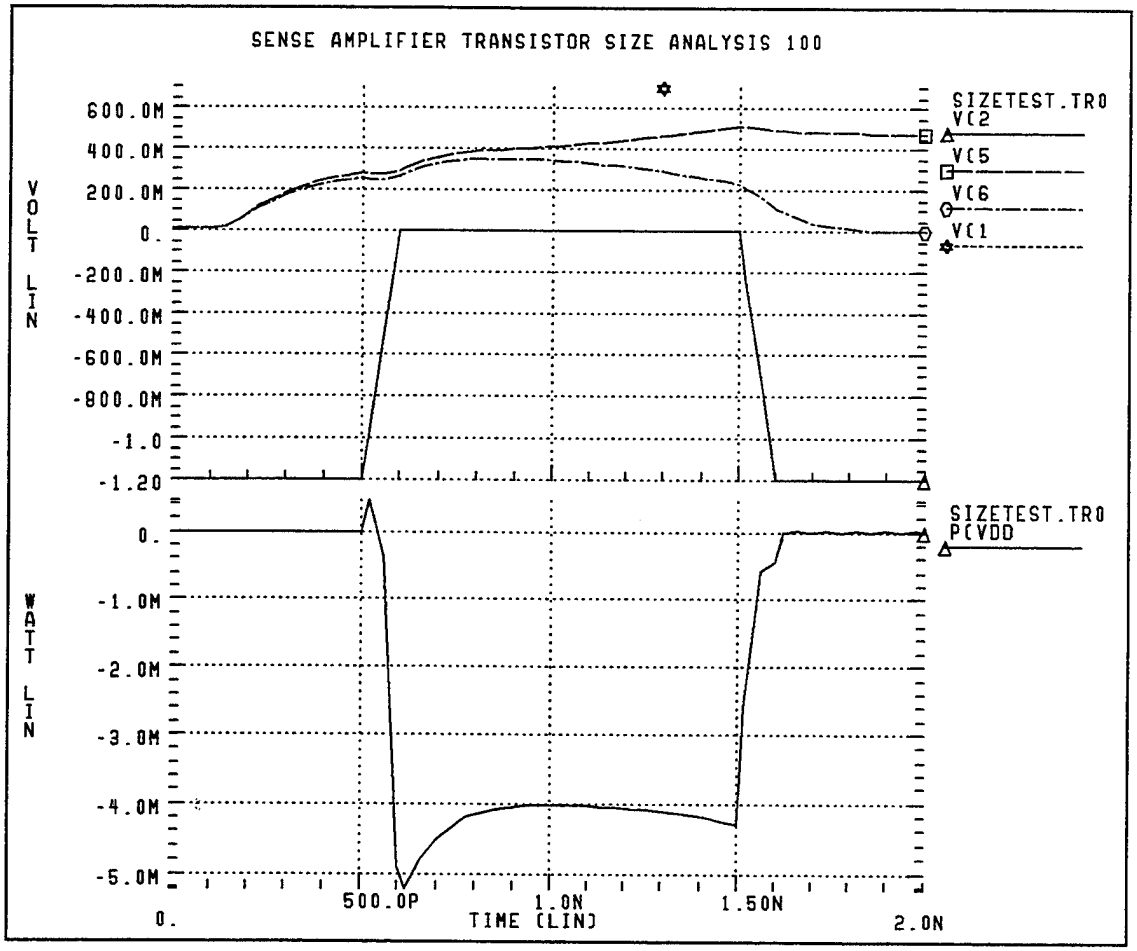


Figure 5.11. Sense Amplifier Operation and Power Requirement.

2. Dummy Cells and Pre-Charge Support

The sense amplifier requires a dummy cell to compare with the storage cell. Dummy cells were also redesigned to eliminate any need for capacitors. The new dummy cells used depletion fets as diode capacitors and were sized to achieve similar properties to the 70pF capacitors used in previous designs. The result was a small dfet with a gate length of 2.0μm and width of 4.0μm. The last support structures to be added included sense transistors for the pre-charge of both bit-lines and dummy cells. Pre-charge voltages were designed for a maximum of 700 mV for the bitline pre-charge and 260 mV for the dummy cell. Based on these maximums, existing precharged sense transistors were resized to a

minimum gate length of 0.8μm while gate width was kept at 3.0μm. Speed was not at issue since pre-charge values were relatively low. Power consumption on the pre-charge sense signal lines was negligible. Redesign of pull-up and pull-down transistors followed a similar approach, reducing the gate lengths to 0.8μm but this time enlarging gate width to 150.0μm and 20.0μm respectively. With the structure defined, preliminary simulations were conducted by read and write operations for both logic ONE and logic ZERO values. Simulations were based on a 666 MHz signal (3μm period) with equal signal rise and fall times of 100ps. The WRITE ONE operation required the most power with a peak of 11.9 mW and average power of 5.4 mw. The WRITE ZERO operation power requirements were negligible. In both cases, the peak power requirement for the cell sense transistor was 1.1 mW. Figure 5.12 shows the write simulation for logic ONE while Figure 5.13 on page 48 shows the write simulation for logic ZERO.

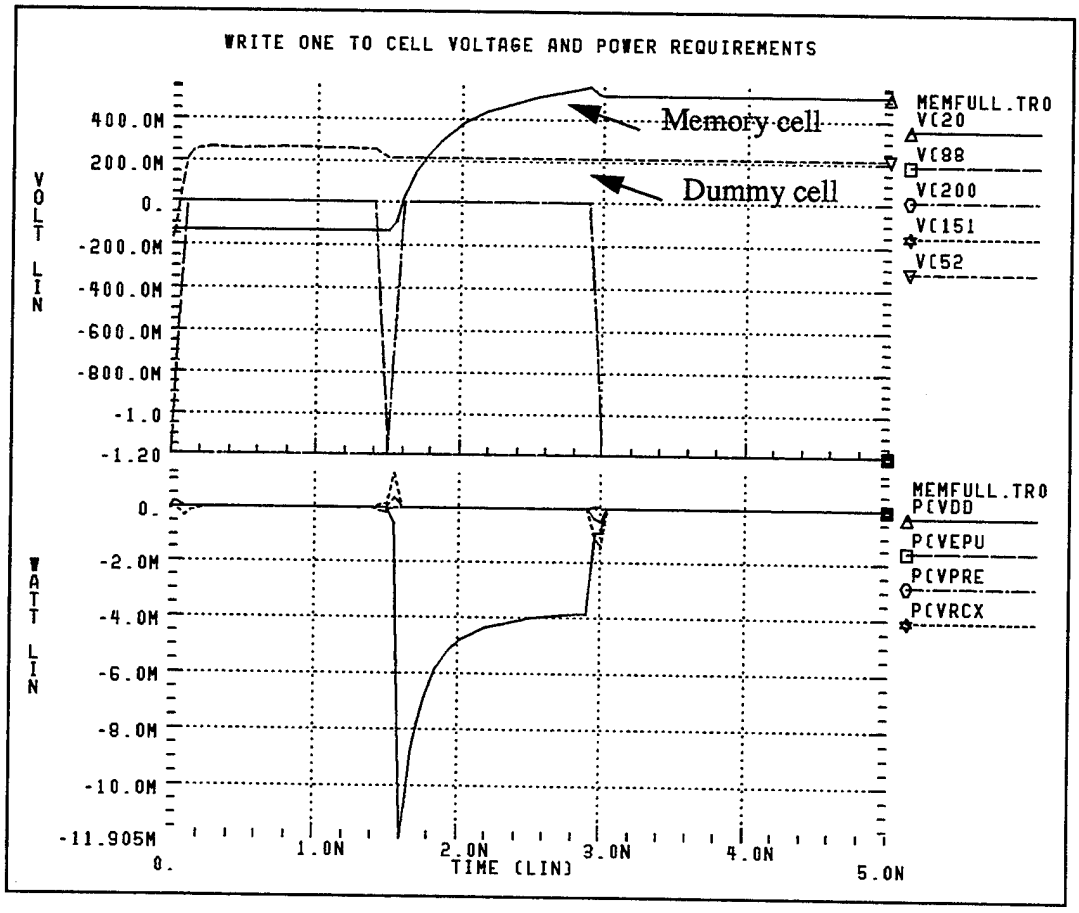


Figure 5.12. WRITE ONE Voltage and Power Requirements.

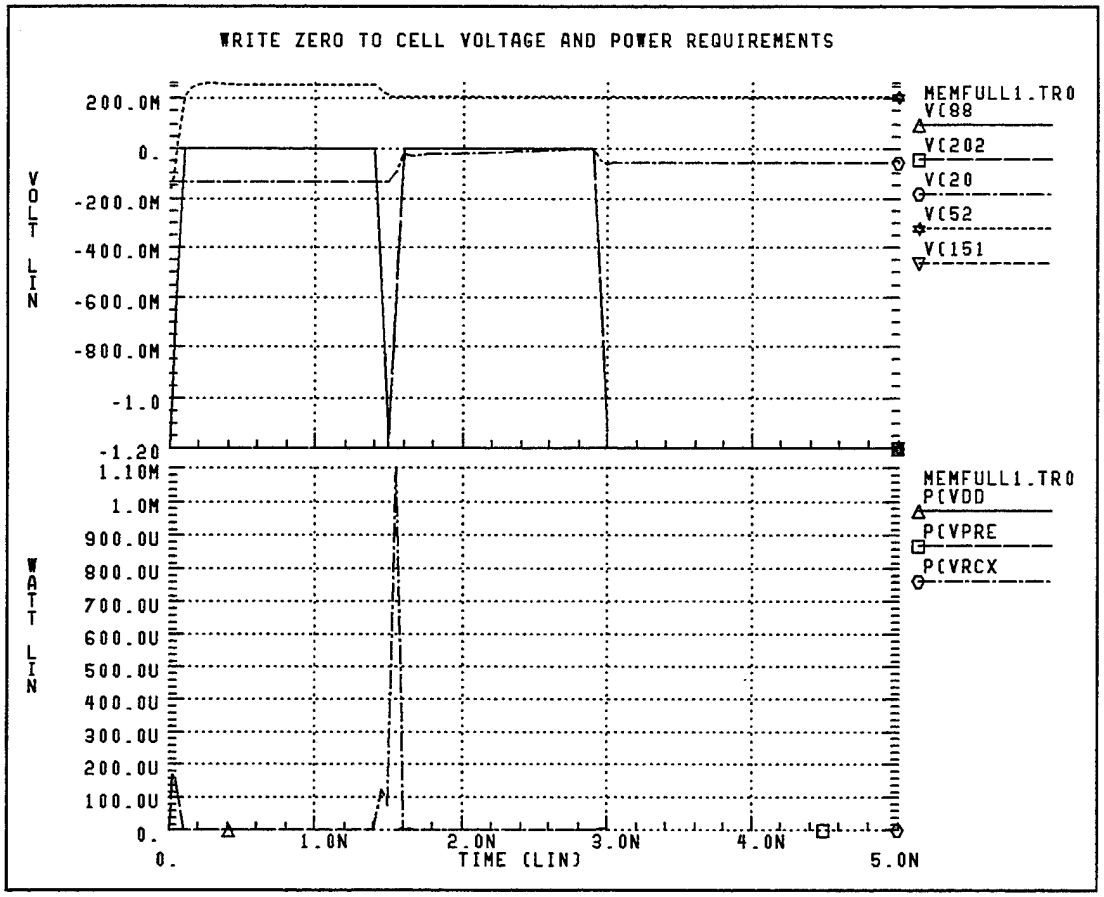


Figure 5.13. WRITE ZERO Voltage and Power Requirements.

Further simulations of READ operations indicated power requirements were proportional with the length of time following the previous WRITE or REFRESH operation. A 3 ms power requirements measured a peak power of 7.5 mW and average power of 4.5 mW. Following successful simulations, design sizes for memory cell and support VLSI layout were established. The final memory cell architecture is depicted in Figure 5.14 on page 49. The following chapter will discuss the VLSI layout of the memory cell.

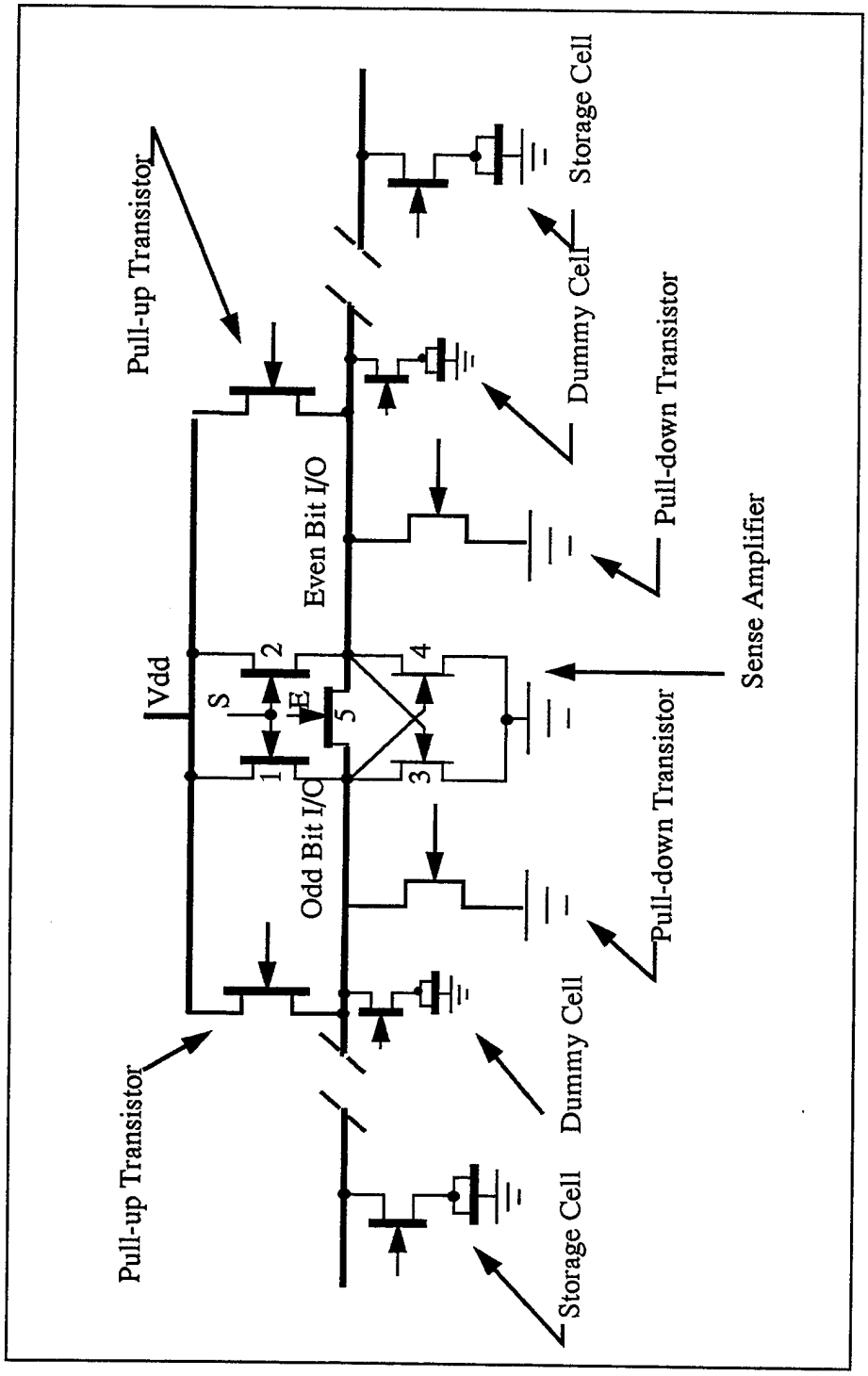


Figure 5.14. Complete Memory Architecture.

VI. DRAM VLSI LAYOUT

A goal of the VLSI layout of the diode-based memory cell was increased modularity. That is, to design layout in a way to reduce wiring interconnect between the individual cells and the support structures. Vagts previously designed a single bit/ 8-address cell with no common connections to build larger arrays. Morris used 4 separate implementations of the cell to build a 32-bit array and required a considerable amount of interconnect routing. Following Manhattan design, the new storage and support structures were built using horizontally oriented metal to route common signal and control lines. The requirement of the sense amplifier for closely balanced bitline capacitance promoted symmetry in the design. The storage cells were stacked vertically above and below the support cell and connected to the support cell through vertically oriented bitlines. Figure 6.1 illustrates the vertical bitline and horizontal signal line orientation of the storage cell.

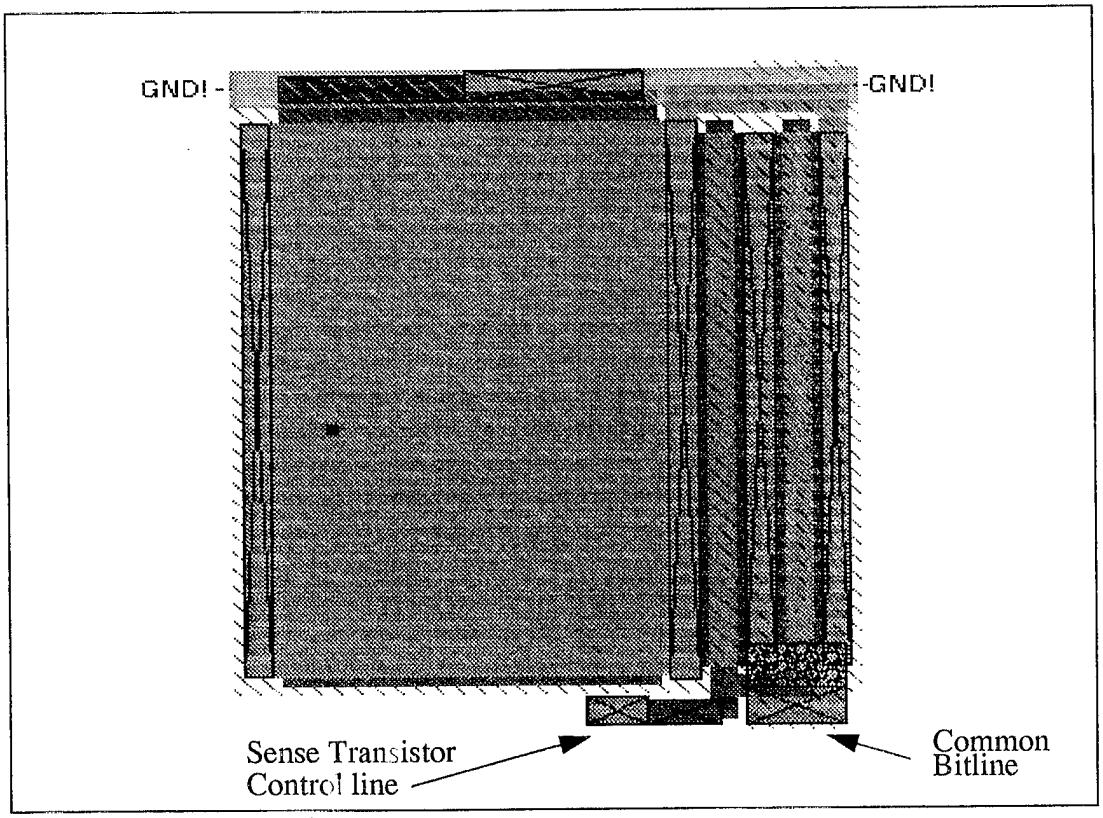


Figure 6.1. Diode-Based Storage Cell Layout.

The approach to building the supporting structures of pull-up, pull-down, sense amplifier and dummy cells was also based on a symmetric approach with common connections vertically to accomodate bitline and horizontal connections to connect support structures of other memory bits. Figure 6.2 illustrates the design of the support structure.

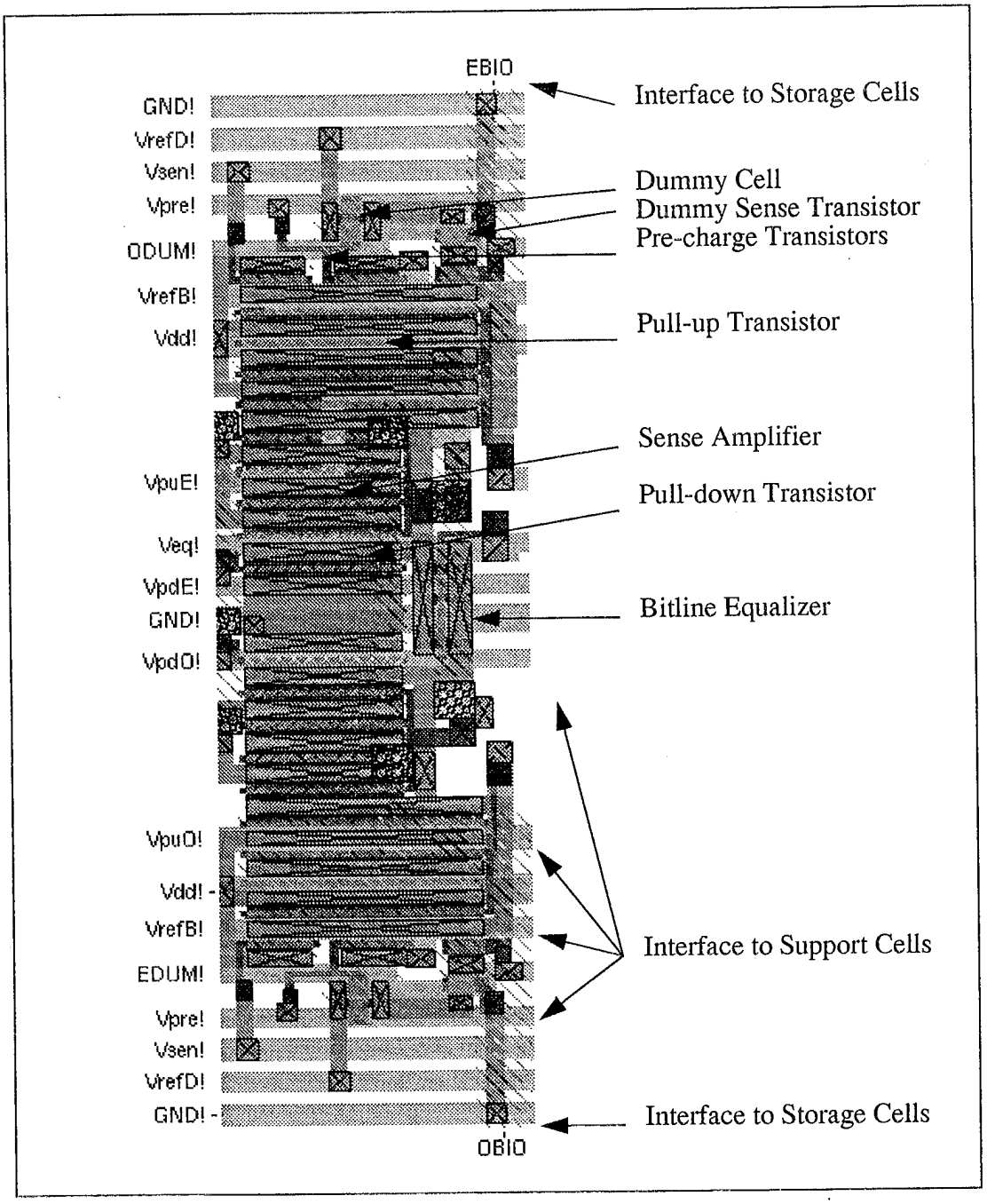


Figure 6.2. Support Cell Layout.

Real space savings are realized when building large arrays of memory components. To accomodate the current chip structure, a 32-bit array was constructed. A space savings of over 25% was realized in the memory footprint alone. Additional space savings comes from the absence of external intercell wiring. The array is depicted in Figure 6.3 with a size comparison made to the capacitor-based 8-bit array.

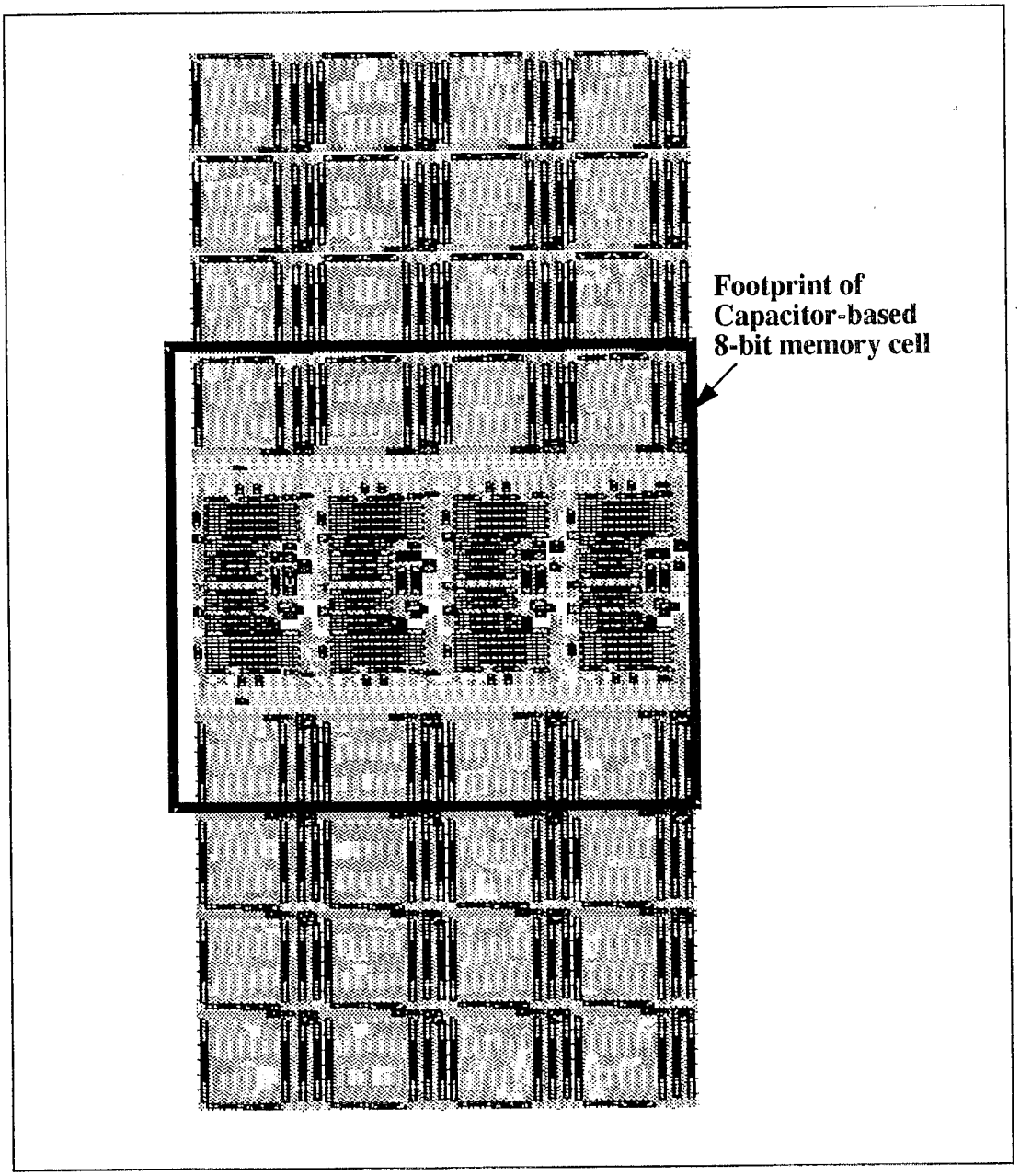


Figure 6.3. 32-Bit Memory Array Layout.

A critical factor in the design of the layout as well as the signal routing to incorporate the new cell into the design was the maximum current limit for the respective metal lines. The following table depicts foundry design guide.

TABLE 6.1. Maximum Current Limits for Metal Lines From Ref. [10].

Layer	R_S	Maximum Current Limit I_{cl}			(mA/μm)
		DC	AC	Peak	ΔW(μm)
Gate Metal	0.5 - 1.5	5.0	5.0	25.0	0.4
Ohmic Implant	180 - 220				
Ohmic Metal	<10	0.3	0.3	0.6	0.0
Metal 1	<0.07	1.0	1.0	5.0	0.2
Metal 2	<0.05	1.4	1.4	7.0	0.0
Metal 3	<0.025	2.8.	2.8	14.0	0.0

The maximum current in a metal line is calculated using Equation (6.1).

$$I_{MAX} = I_{cl} \times (W - \Delta W) \qquad (6.1)$$

Where W is the drawn line width and ΔW is the process control factor. Maximum current limits in Table 6.1 are valid for a maximum operating temperature of 85 degrees Centigrade. Based on the maximum current limits, Vdd interconnect width was increased to supply the required current. The increased interconnect requirement was accomplished by distributing Vdd interconnect vertically on both sides of the support structure. A similar configuration was performed for Ground. All other interconnect exceeded size requirements for maximum power. Future designs could optimize cell integration by reducing interconnect to absolute minimum widths to meet maximum current limits. Appendix D contains a complete interconnect diagram of the cell incorporated into the GaAs chip.

VII. CONCLUSIONS

This thesis presented three separate but related issues. It reviewed a GaAs DRAM design incorporating a single transistor, capacitor-based storage cell. Following the review, an evaluation and functional testing of an ECL testbench for the GaAs DRAM was performed. Last, a new storage cell design incorporating a diode-based storage cell was developed.

The failure of the ECL testbench, due to pin-out orientation, leaves the DRAM still untested. However, the ECL based testbench proved fully functional and could be used to test new chip designs if the chip pin-out orientation matches the pin-out of the testbench. In order to test the existing DRAM, a completely new PCB will have to be designed. Future designs of a PCB testbench based on the work of Butler [Ref. 3] and Ginter [Ref. 4] can be assured of success. Designers are advised to utilized an industry standard PCB design application like 'Allegro' from Cadence. All high speed inputs to the PCB should be ported through SMA connectors. Refresh inputs should allow for a wide range of refresh rates. It is essential to determine the exact component dimensions as well as to ensure component availability prior to submitting final designs. The signal lines from the chip pads as well as support components should be placed to accommodate a clamp or similar device used to secure the chip to the testbench. The importance of the use of a manual clock integrated into the design can not be overemphasized. And finally, extreme care must be given when final checking netlists and pin-out orientations in the PCB.

The follow-on design of the GaAs single-transistor memory cell proved the depletion diode to be a viable alternate as a capacitive storage element. The nonlinear capacitive characteristics of the reversed biased Schottky diode allowed for a smaller dimensioned element. The design simulations demonstrated that the physical dimensions of the sense transistor in the memory cell had substantial effects on charge storage and maintenance. A balanced memory cell was achieved through an iterative, trial and error process ultimately succeeding in improvement over the capacitor-based cell. Improvement

of charge retention increased from an average of 3 ms to 3.4 ms allowing for reduced refresh rates and additional power savings. The greater charge retention and flatter charge dissipation slope also afforded an opportunity to use lower pre-charge voltages also increasing the power savings. However, there was a trade off in transistor size and power required for READ, WRITE and REFRESH operations. The shorter gate lengths and widths increased power requirements in the bitline pull-up and sense amplifier transistors but allowed simulations up to 666 MHz. Temperature continues to adversely affect the charge retention of the diode-based storage device. The compact design and modular layout approach afforded a size savings of over 25% for a 32-bit array. The 32-bit array was integrated in with the existing GaAs DRAM high-level circuits however, the interconnect proved to be substantial and voided most of the space savings enjoyed by the new modular memory array. Future GaAs DRAMs should continue a modular, hierarchal approach to redesigning high-level circuits. The modularity will reduce interconnect and provide room for larger memory arrays. With high-level redesign, the space savings should accommodate a memory array of at least 128 bits. The larger memory array would require a modification of the counter within the refresh circuit. Counters would now count from 00000 to 11111, addresses 0 to 31. The decoder circuit would also require redesign to handle 5-bit logic. The speed performance of the GaAs DRAM memory cell is very impressive and warrants continued research and development. As new applications and fabrication techniques are developed, GaAs will grow to be more prevalent in electronic designs.

APPENDIX A. GaAs DRAM HIGH LEVEL CIRCUITS

This appendix contains block diagrams of the DRAM high level circuits developed in earlier research. The high level circuits include: Two-Phase Non-Overlapping Clock, One-Of-Eight Decoder, Eight Stage Counter, DRAM Refresh, Decoder Driver, Output Logic, Operation Priority Logic, Memory Busy, Data Ready, Write Logic, Pad Receiver, and Driver Pad Circuits.The new diode-based storage cell was designed to accommodate signals generated by the existing circuitry.

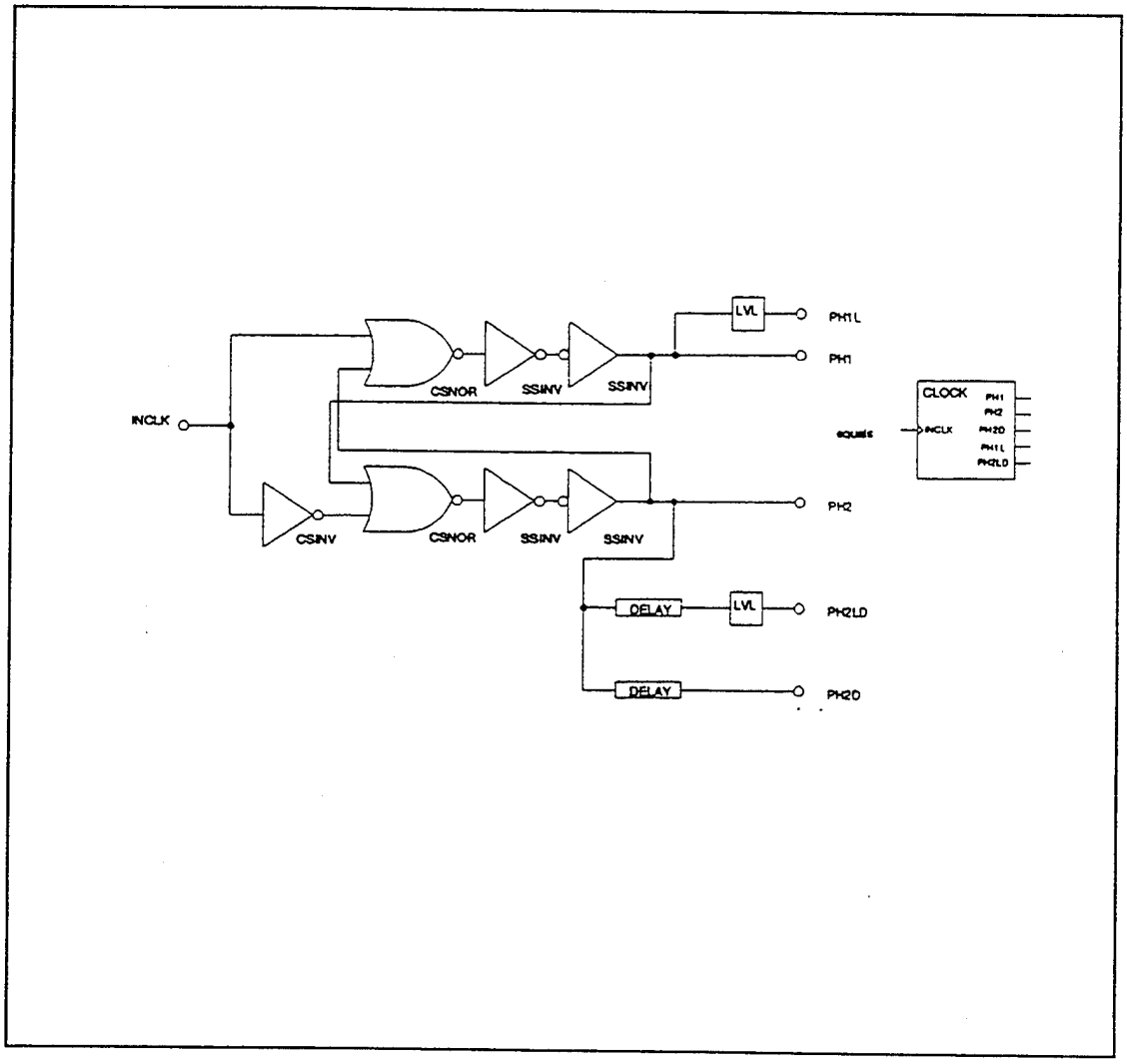


Figure A.1. CLOCK Circuit From Ref. [4].

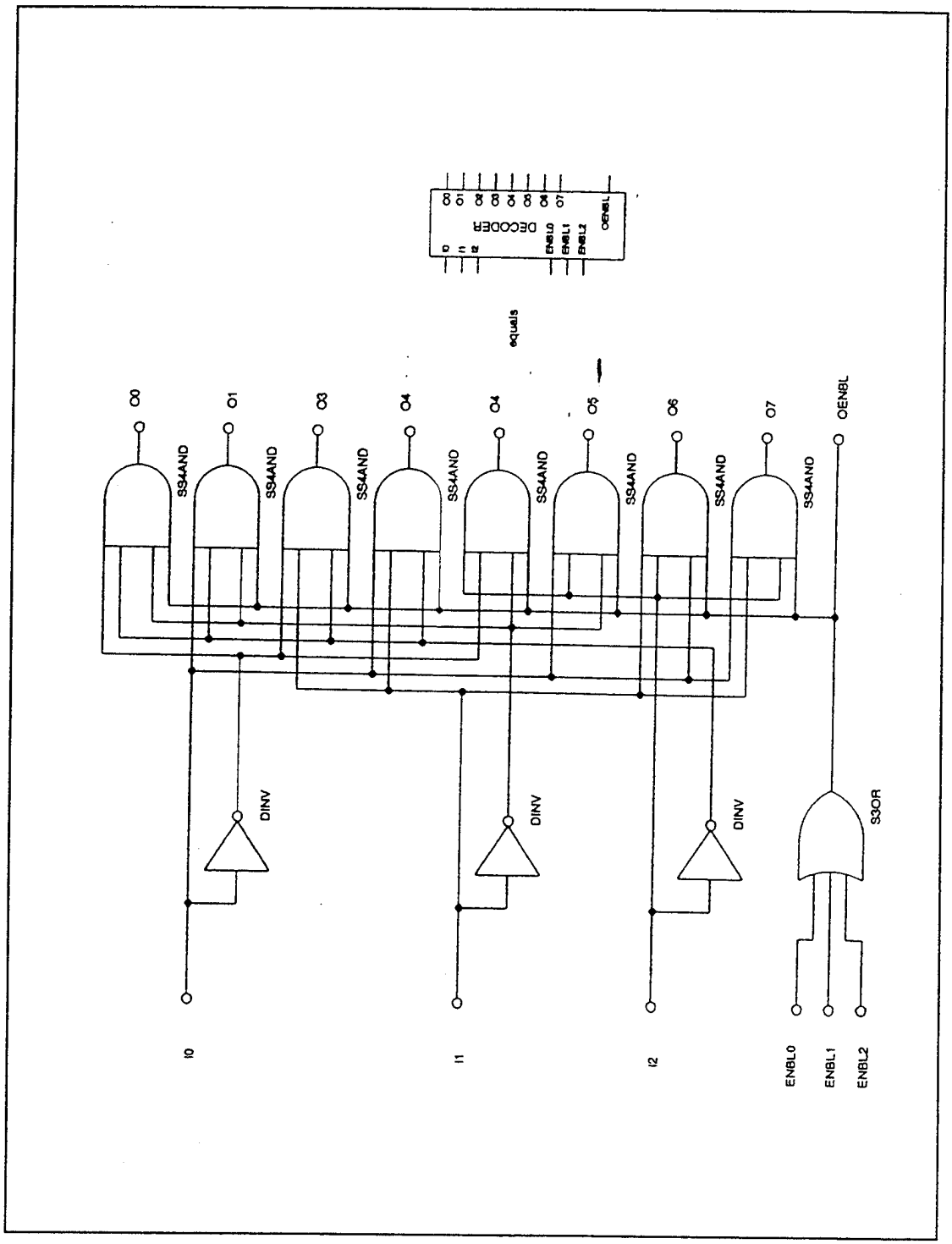


Figure A.2. DECODER Circuit From Ref. [4].

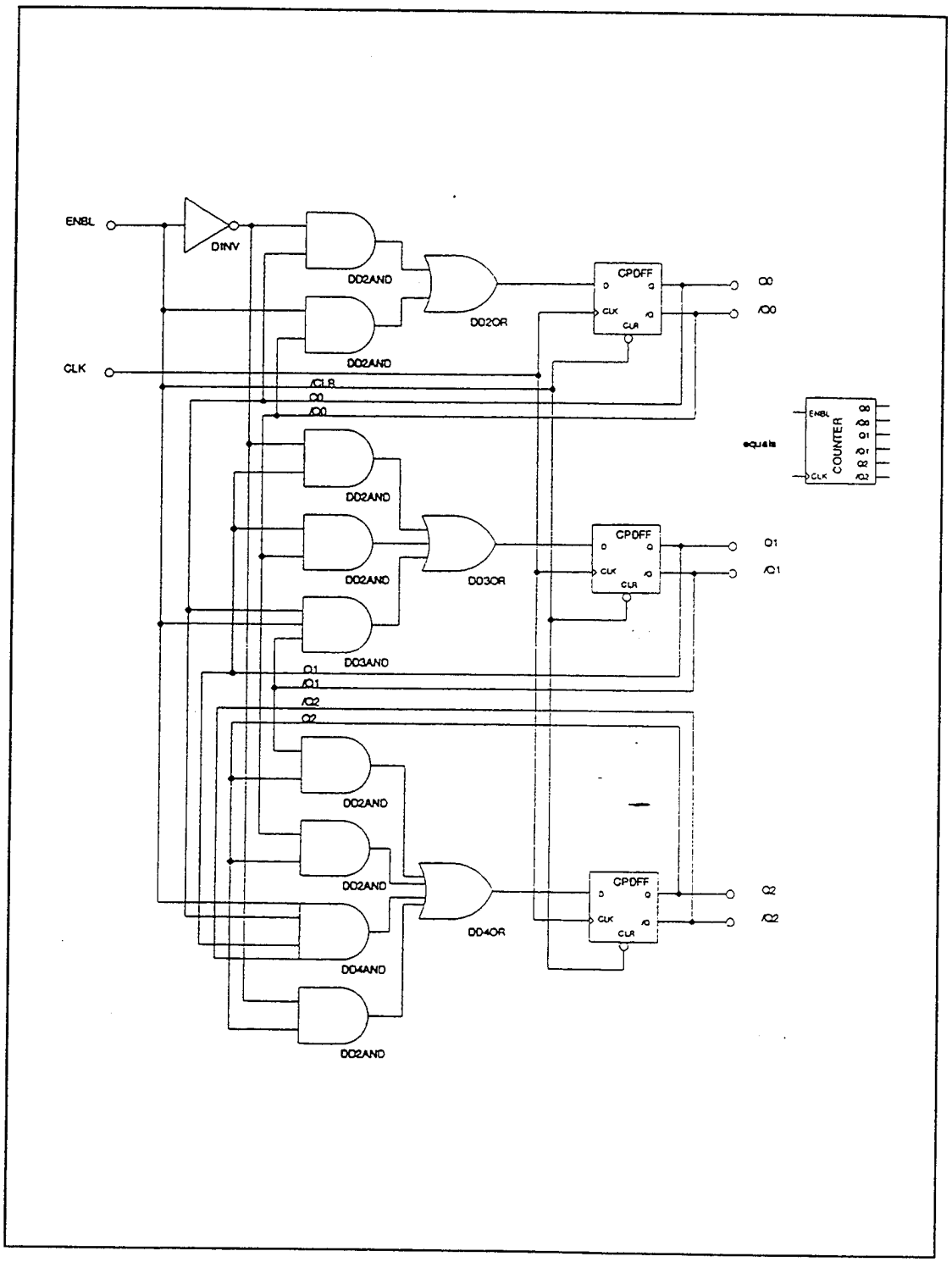


Figure A.3. COUNTER Circuit From Ref. [4].

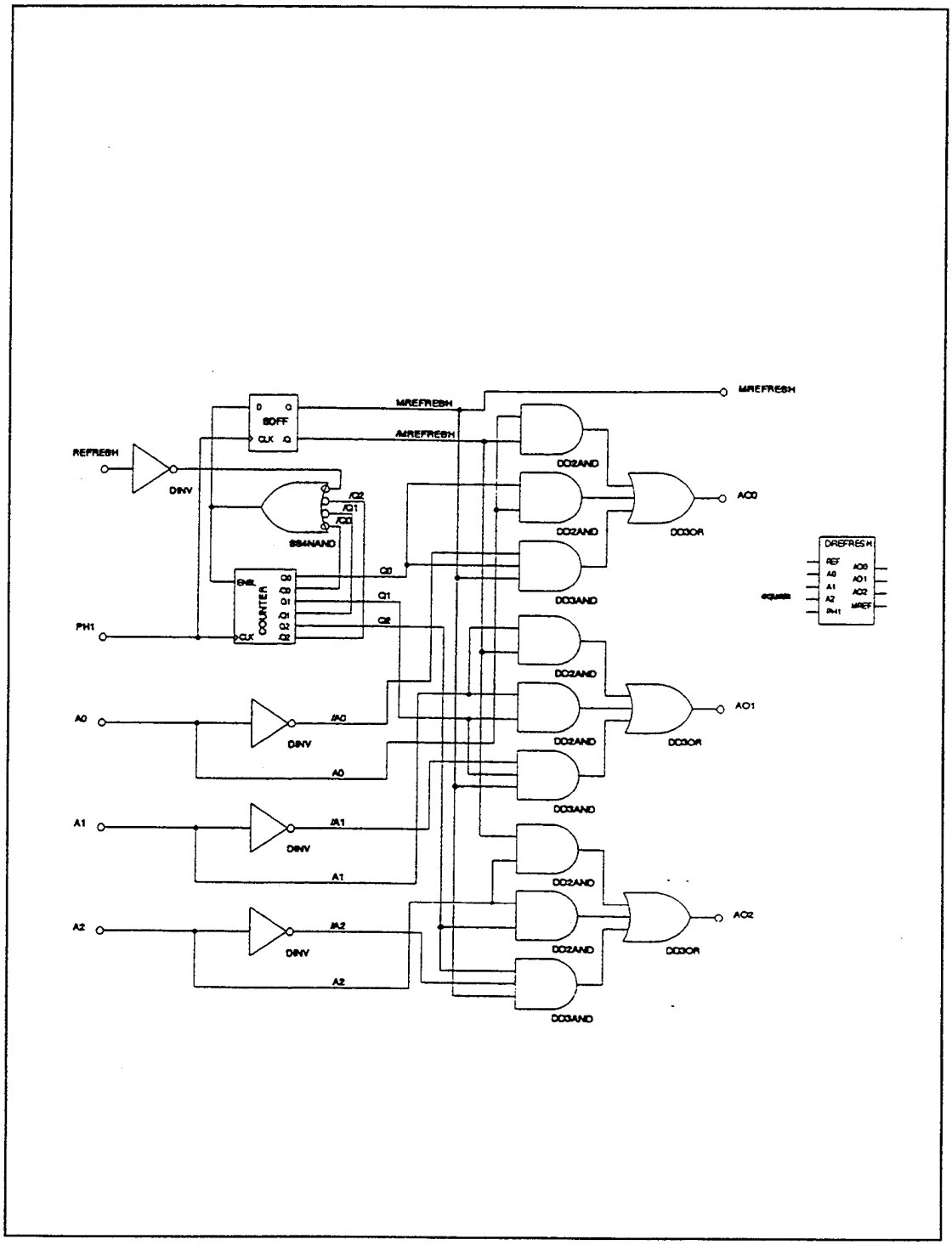


Figure A.4. DREFRESH Circuit From Ref. [4].

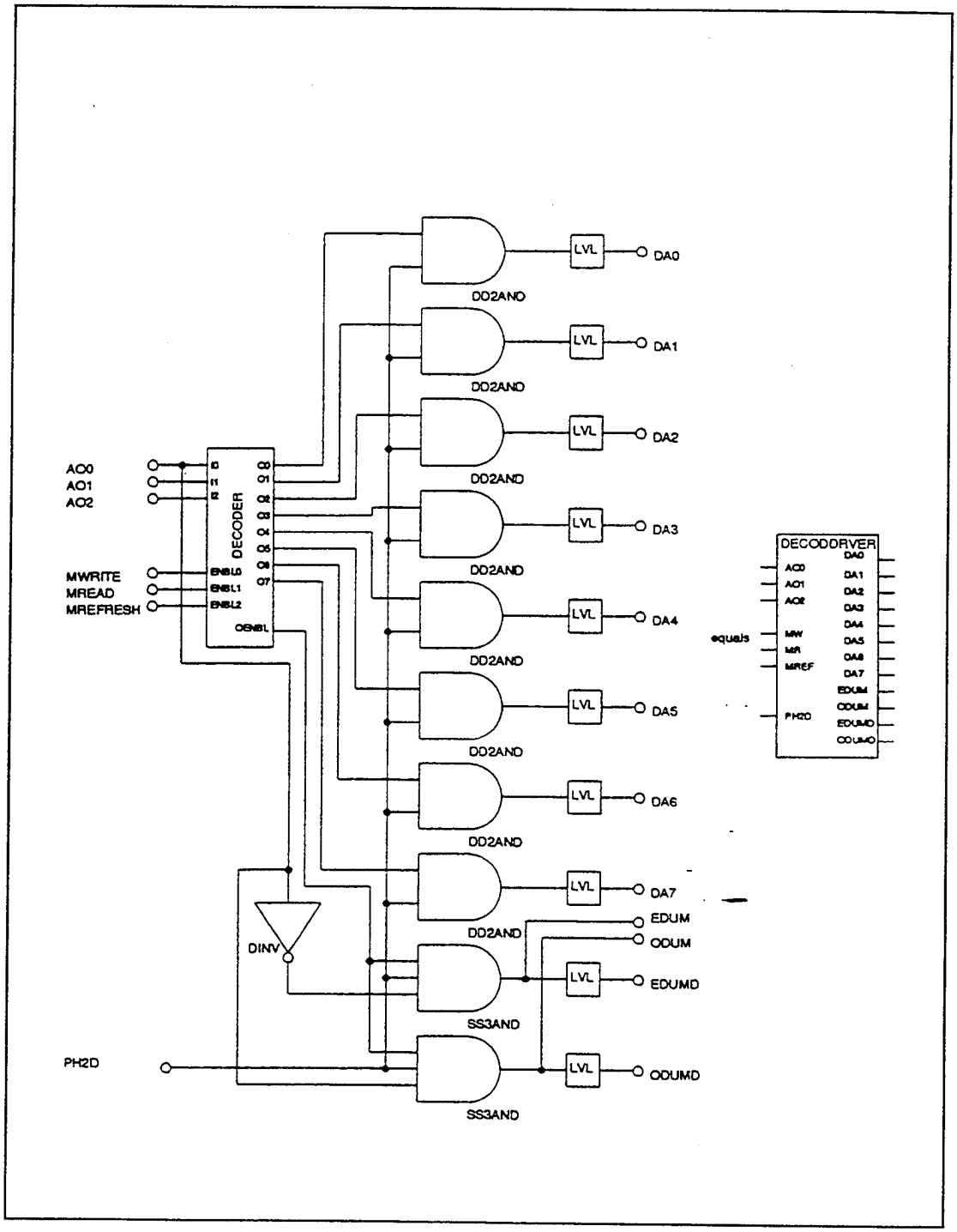


Figure A.5. DECODDRVER Circuit From Ref. [4].

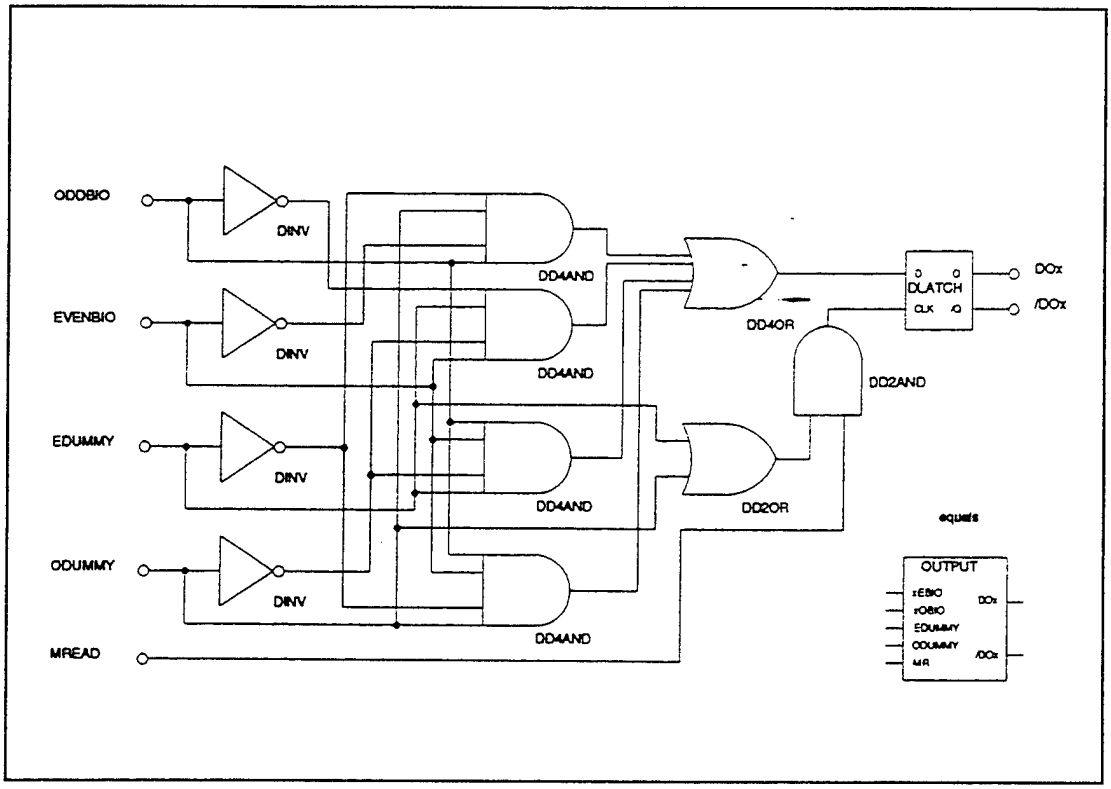


Figure A.6. OUTPUT Circuit From Ref. [4].

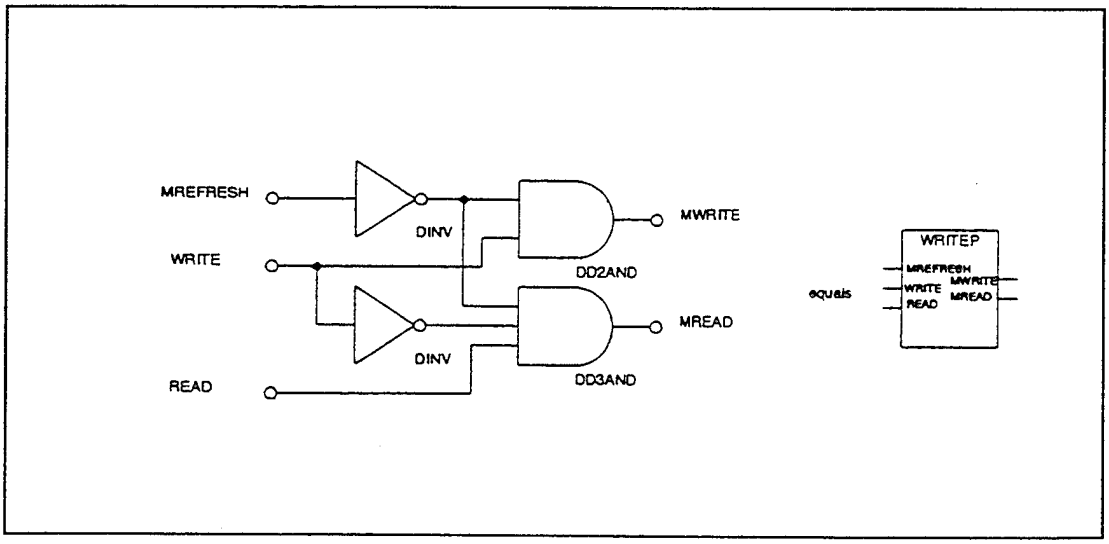


Figure A.7. WRITEP Circuit From Ref. [4].

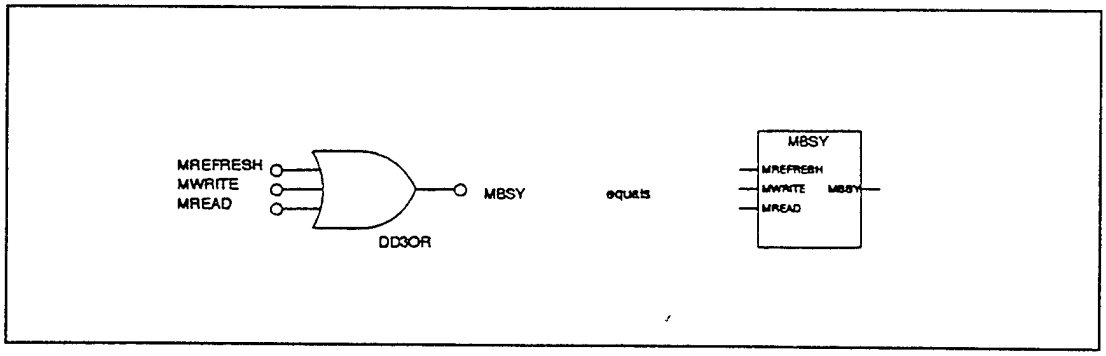


Figure A.8. MBSY Circuit From Ref. [4].

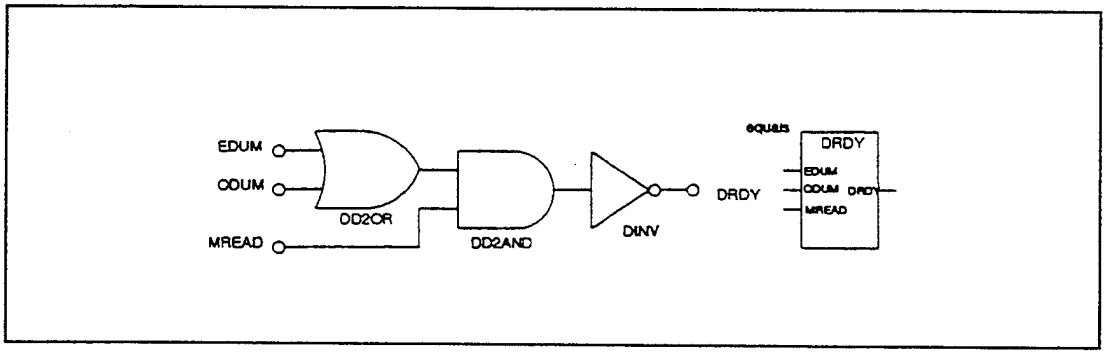


Figure A.9. DRDY Circuit From Ref. [4].

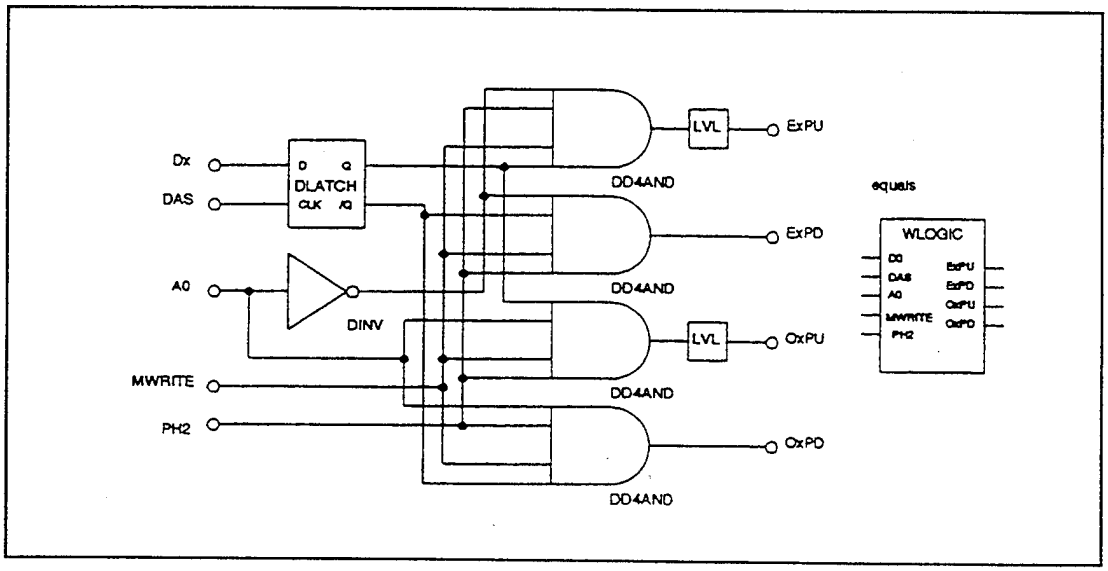


Figure A.10. WLOGIC Circuit From Ref. [4].

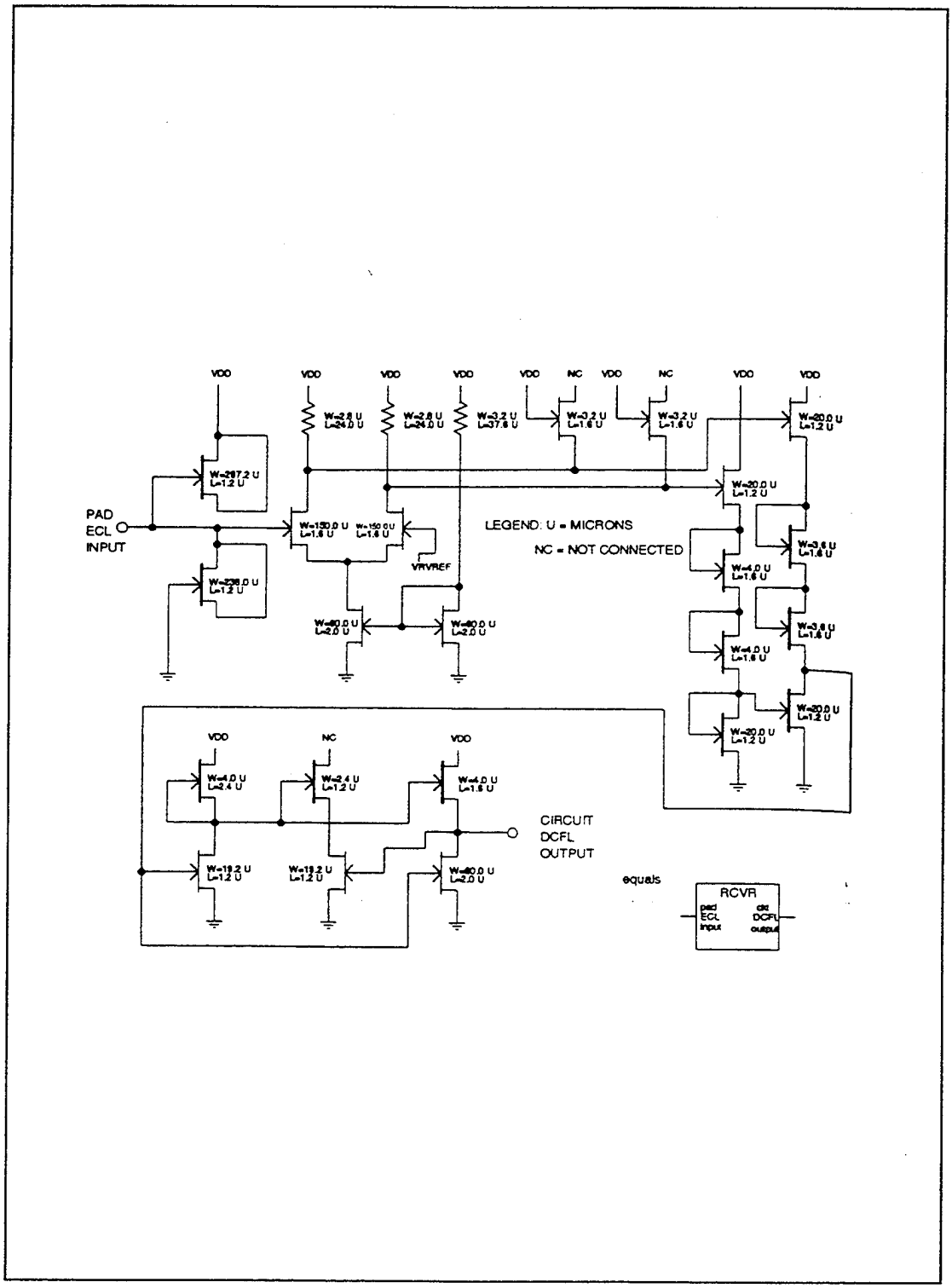


Figure A.11. PADRCVR Circuit From Ref. [4].

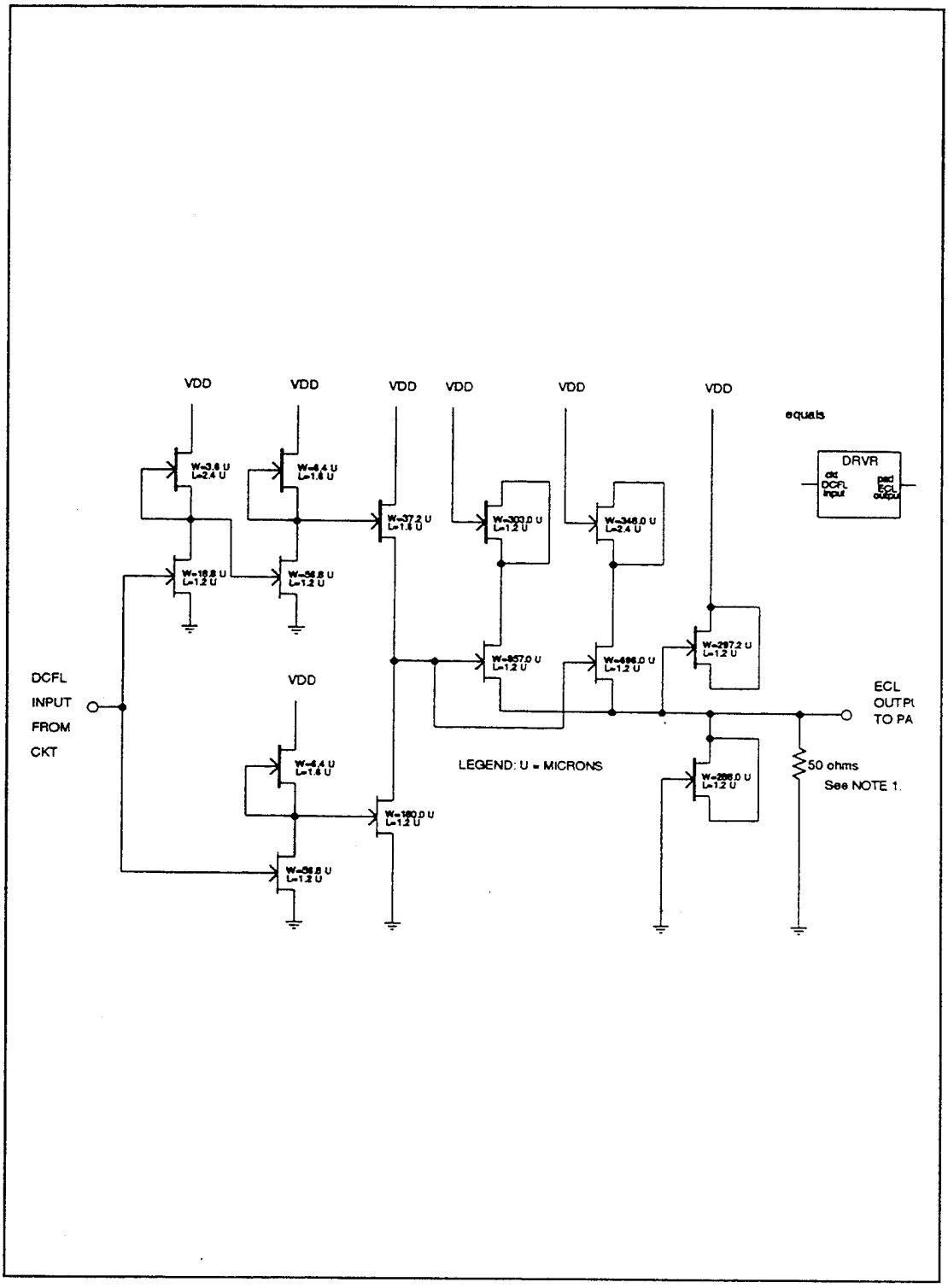


Figure A.12. DRVRPAD Circuit From Ref. [4].

APPENDIX B. PRINTED CIRCUIT BOARD COMPONENTS

This appendix contains National Semiconductor F100K series 300 ECL components used in the fabrication of the six layer printed circuit board test bench. All components were packaged using a 28 Lead Plastic Chip Carrier, PCC. The surface mount device provides for a smaller device footprint and the symmetry reduces the effects of skew. The 28 pins allow for additional V_{CC} pins which also reduce skew by providing extra paths for output signal return currents to ground. Layout dimensions are illustrated in Figure B.1.

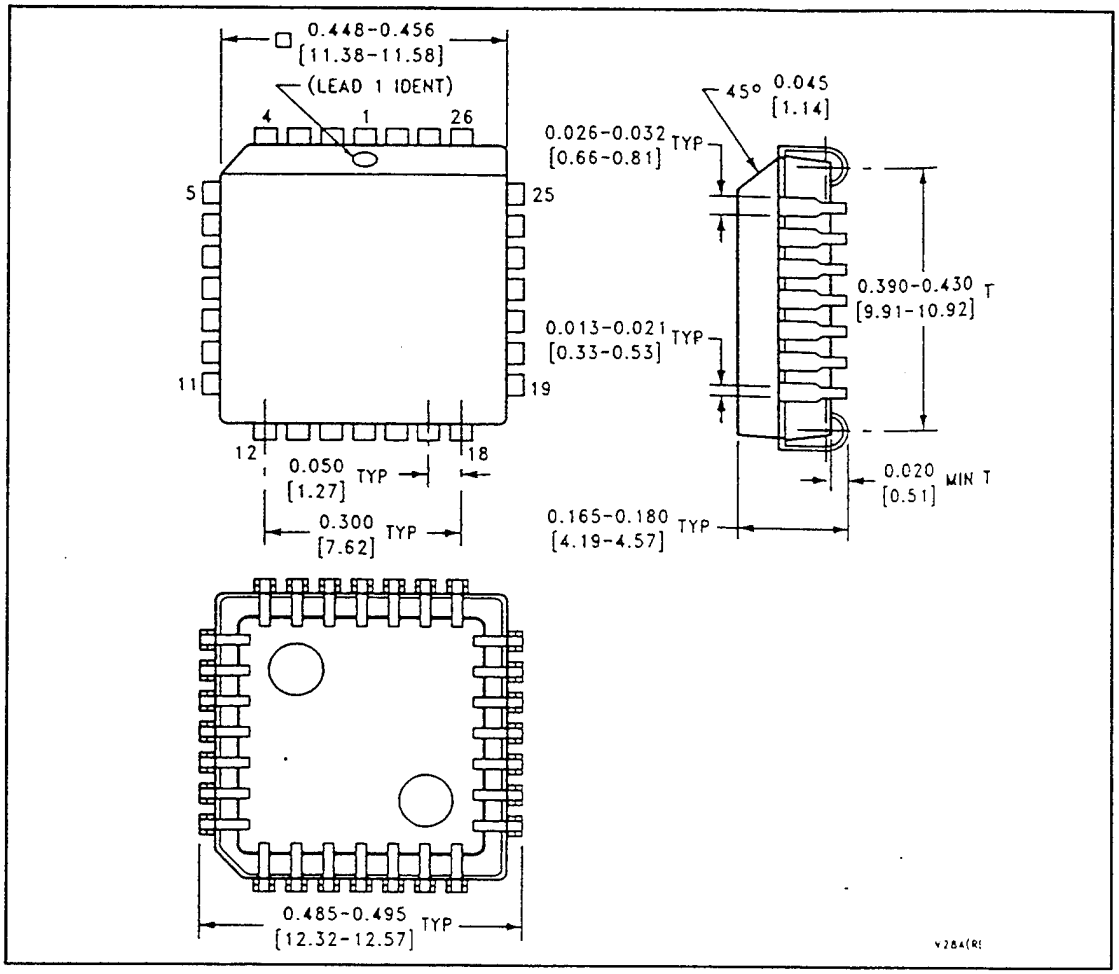


Figure B.1. 28-Pin PCC Package From Ref. [8].

The following figures contain general descriptions, features, logic symbols, truth table and connection diagrams for the six basic components used in the PCB design. The

components include: 100302 2-Input OR/NOR Gate, 100304 AND/NAND Gate, 100313 Quad Driver, 100331 Triple D Flip-Flop, 100336 4-Stage Counter/Shift Register and 100341 8-Bit Shift Register. Complete voltage information can be found in the F100K ECL Series 300 Databook. [Ref. 8]

Low Power Quint 2-Input OR/NOR Gate

General Description

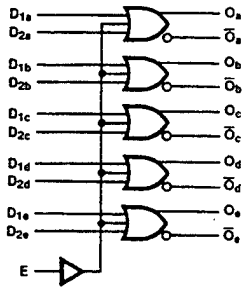
The 100302 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 43% power reduction of the 100102
- 2000V ESD protection
- Pin/function compatible with 100102
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol



TL/F/10580–1

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
E	Enable Input
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

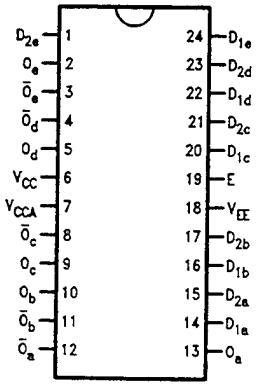
Truth Table

D_{1X}	D_{2X}	E	O_X	$\overline{O}_X$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

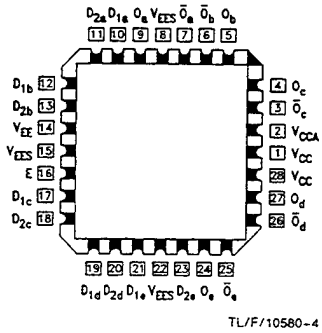
H = HIGH Voltage Level
L = LOW Voltage Level

Connection Diagrams

24-Pin DIP/SOIC

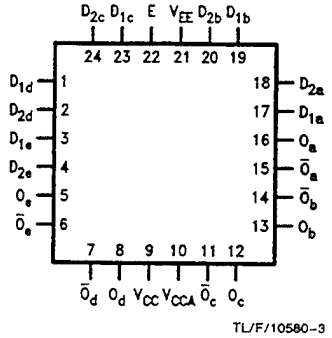


28-Pin PCC



TL/F/10580–4

24-Pin Quad Cerpak



TL/F/10580–3

Figure B.2. 100302 2-Input OR/NOR Gate From Ref. [8].

100304
Low Power Quint AND/NAND Gate

General Description

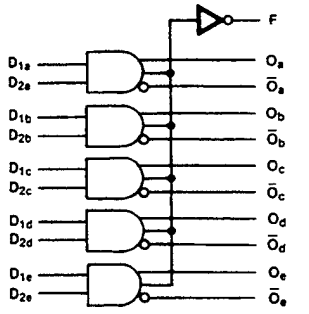
The 100304 is monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs. All inputs have 50 kΩ pull-down resistors.

Features

- Low Power Operation
- 2000V ESD protection
- Pin/function compatible with 100104
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol



TL/F/10581–1

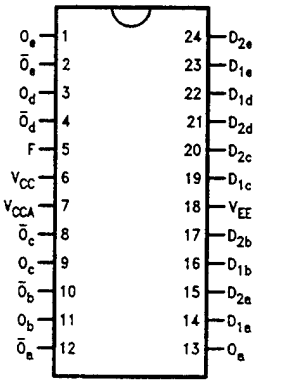
Logic Equation

$$F = \overline{(D_{1a} \bullet D_{2a}) + (D_{1b} \bullet D_{2b}) + D_{1c} \bullet D_{2c}) + (D_{1d} \bullet D_{2d}) + (D_{1e} \bullet D_{2e})}.$$

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
F	Function Output
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

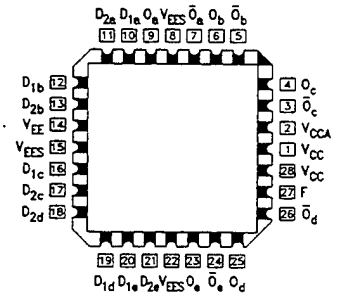
Connection Diagrams

24-Pin DIP



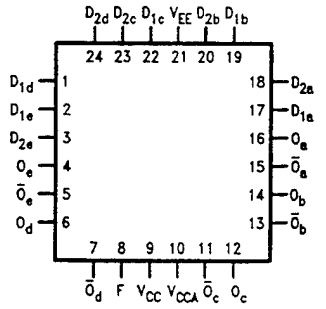
TL/F/10581–2

28-Pin PCC



TL/F/10581–4

24-Pin Quad Cerpak



TL/F/10581–3

Figure B.3. 100304 AND/NAND Gate From Ref. [8].

100313
Low Power Quad Driver

General Description

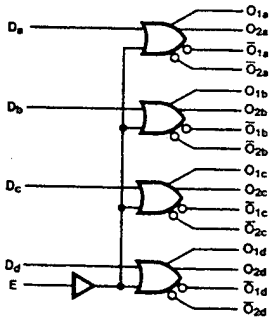
The 100313 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 50% power reduction of the 100113
- 2000V ESD protection
- Pin/function compatible with 100113 and 100112
- Voltage compensated operating range = −4.2V to −5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

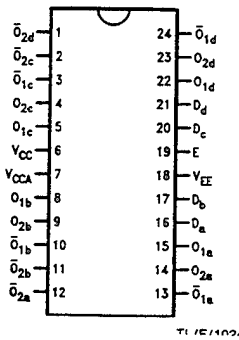


TL/F/10249–3

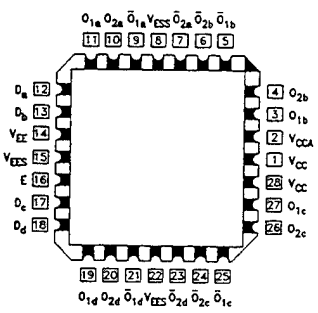
Pin Names	Description
D_a–D_d	Data Inputs
E	Enable Input
O_{na}–O_{nd}	Data Outputs
$\overline{O}_{na}$–$\overline{O}_{nd}$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP/SOIC

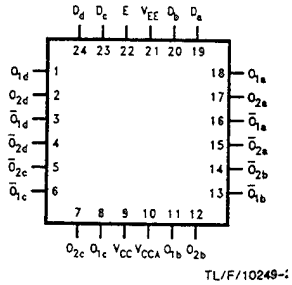


28-Pin PCC



TL/F/10249–4

24-Pin Flatpak



TL/F/10249–

Figure B.4. 100313 Quad Driver From Ref. [8].

100331
Low Power Triple D Flip-Flop

General Description

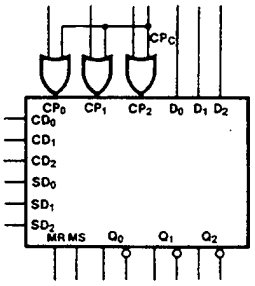
The 100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the 100131
- 2000V ESD protection
- Pin/function compatible with 100131
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol

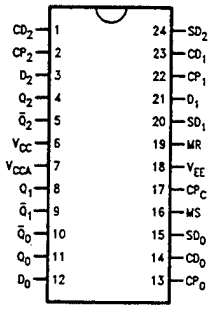


TL/F/10262–1

Pin Names	Description
CP_0–CP_2	Individual Clock Inputs
CP_C	Common Clock Input
D_0–D_2	Data Inputs
CD_0–CD_2	Individual Direct Clear Inputs
SD_n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

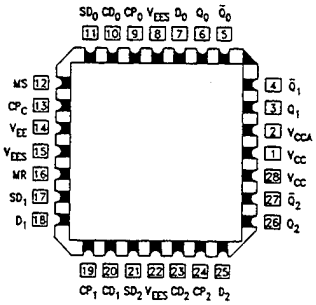
Connection Diagrams

24-Pin DIP/SOIC



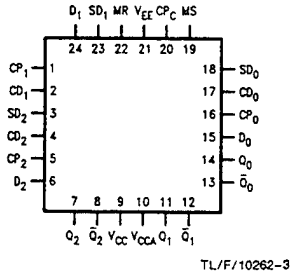
TL/F/10262–2

28-Pin PCC



TL/F/10262–4

24-Pin Quad Cerpak



TL/F/10262–3

Figure B.5. 100331 Triple-D Flip-Flop From Ref. [8].

100336
Low Power 4-Stage Counter/Shift Register

General Description

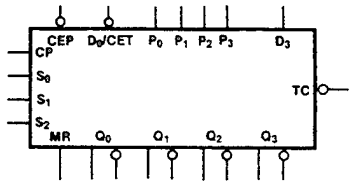
The 100336 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multistage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation, D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50 kΩ pull-down resistors.

Features

- 40% power reduction of the 100136
- 2000V ESD protection
- Pin/function compatible with 100136
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code: See Section 6

Logic Symbol

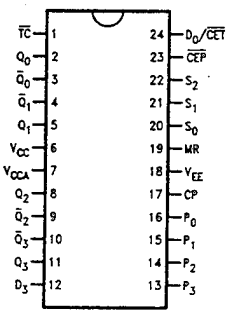


TL/F/10584–1

Pin Names	Description
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0–S_2	Select Inputs
MR	Master Reset Input
P_0–P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0–Q_3	Data Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complementary Data Outputs

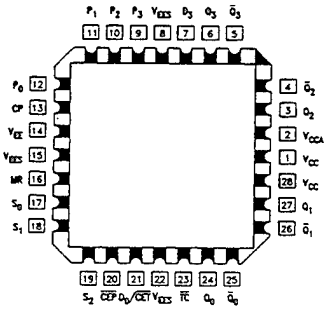
Connection Diagrams

24-Pin DIP/SOIC



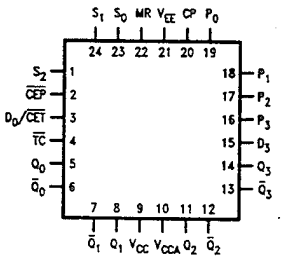
TL/F/10584–2

28-Pin PCC



TL/F/10584–4

24-Pin Quad Cerpak



TL/F/10584–3

Figure B.6. 100336 4-Stage Counter/Shift Register From Ref. [8].

100341
Low Power 8-Bit Shift Register

General Description

The 100341 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

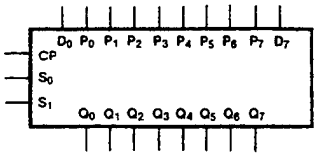
The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the 100141
- 2000V ESD protection
- Pin/function compatible with 100141
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range

Ordering Code: See Section 6

Logic Symbol

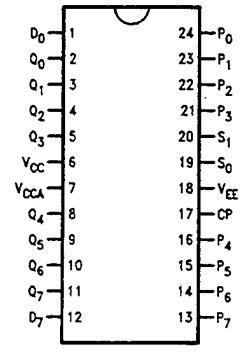


TL/F/9880-1

Pin Names	Description
CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0–P_7	Parallel Inputs
Q_0–Q_7	Data Outputs

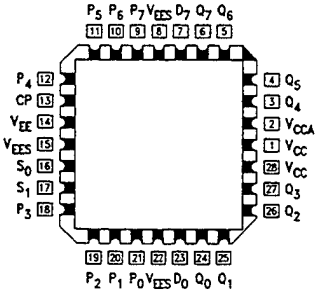
Connection Diagrams

24-Pin DIP/SOIC



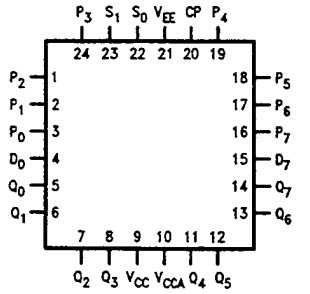
TL/F/9880-2

28-Pin PCC



TL/F/9880-4

24-Pin Quad Cerpak



TL/F/9880-3

Figure B.7. 100341 8-Bit Shift Register From Ref. [8].

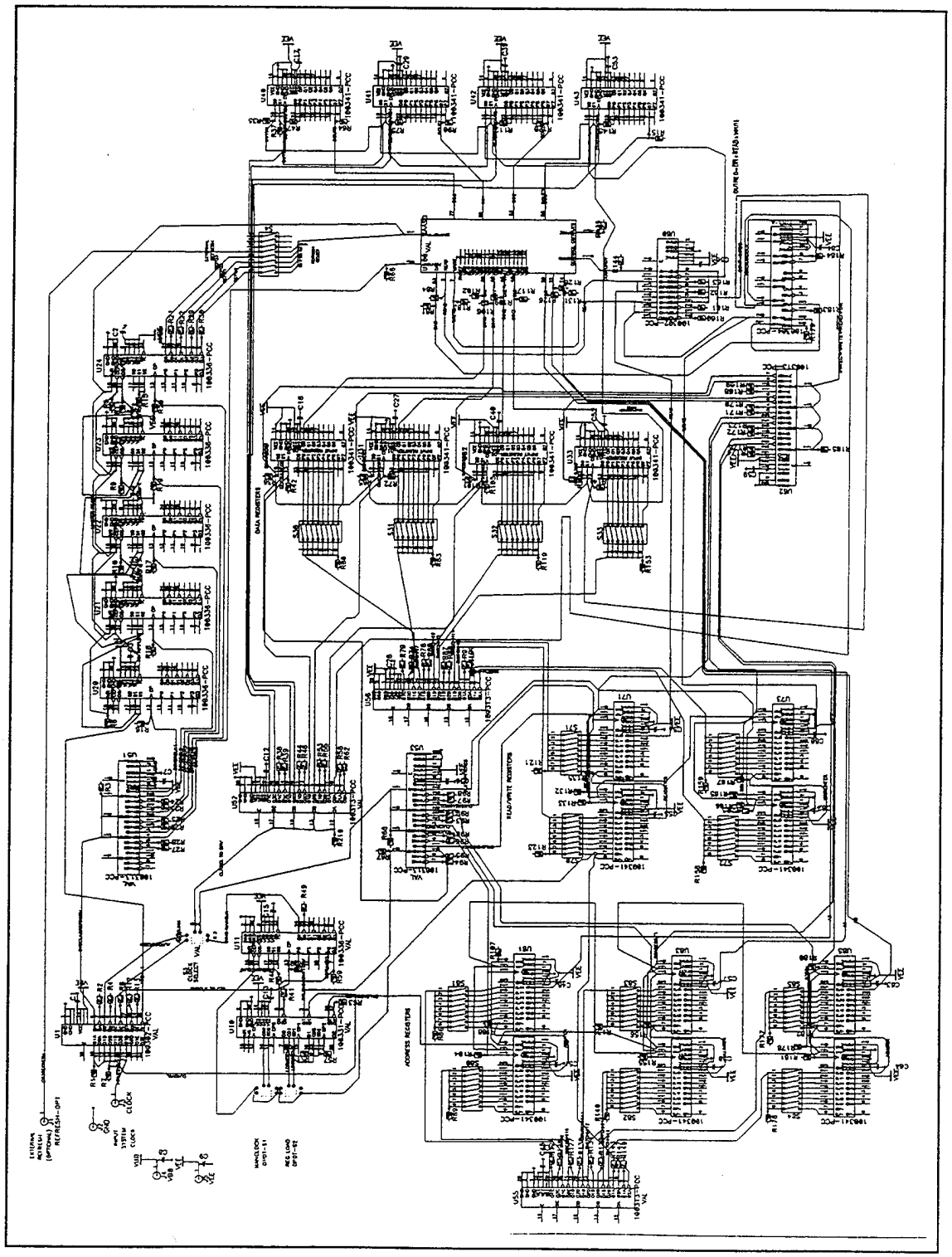


Figure B.8. Printed Circuit Board Schematic From Ref. [6].

APPENDIX C. HSPICE FILES

This appendix contains test files used to make comparisons and evaluations on various types and configurations of the GaAs One Transistor Memory Cell. Initially both enhancement and depletion type diodes were tested with depletion type being superior. The next set of tests contained comparisons of diodes with various gate lengths. A direct relationship between diode gate length and charge maintenance was achieved up to 30 microns. Gate lengths longer than 30 microns displayed a poor return for the increase in size.

A. HSPICE FILE FOR DIODE TYPE COMPARISON

```
**********************************************************
*      file: compare1.sp
*      HSPICE Simulation to compare charge storage
*      capabilities in GaAs Enhancement and
*      Depletion Diodes J* = * * * dp1.3 l=2.8 w=52
*
**********************************************************
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect


* Controls signals for the One-Transistor Model with Diode
**********************************************************

* Ideal power signal to bitline
*******************************

Vb1 3 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)

Vb10 30 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)

Vb11 33 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)

* vw* is the Read/Write Pulse for Diode models
************************************************
```

```
Vw1 4 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)

Vw10 31 0 PULSE(0 0.63 1000PS 100PS 100PS 400PS 10mS)


* vw2 is the Read/Write Pulse for the capacitor model
**************************************************

Vw11 34 0 PULSE(-1.2 0 1000PS 100PS 100PS 500PS 10mS)
* One Transistor Model with Diode
**********************************

* Note each group uses a different diode gate length
* with gate width set to w = 52.0

j1  3  4  5  0  dp1.3  l=2.8  w=150.0
j2  5  0  5  0  dp1.3  l=2.8 w=52.0
c2  3  0  1000FF


j19  30  31  32  0  dp1.3  l=2.8  w=150.0
j20  32  0  32  0  enh.2  l=8.0 w=152.0
c11   0  1000FF

* One Transistor Model with Capacitor
**************************************

j21  33  34  35  0  dp1.1  l=1.2 w=150.0
c1   35  0  1880FF
c12  33  0  1000FF

* This is the Temperature Flag that sets simulation temp to
* 85 degrees centigrade
.temp 85.0

* The .probe command ensures that only the listed siganls are saved
* for evaluation
.probe v(3) v(5) v(32) v(35)

* The .tran command tells the simulation to run for 3000 nanoseconds
* and save data recordings every 50000 picoseconds
.tran 100n 1ms
```

```
* The following line sets up the scale of devices to microns
* enables HSPLOT interface
* prints table of single plate nodal capacitances
* and reduces output to just the probe variables
.options scale=1E-06 post captab gmindc=1E-11 probe
.end
```

B. HSPICE FILE TO TEST GATE LENGTH CHARACTERISTICS

```
**************************************************************
*
* file: diode.sp
* HSPICE Simulation to Compare Variations of Diode Size in
* One-Transistor Model with fixed sense transistor of
* J* = * 4 * 0 dp1.3 l=2.8 w= 150.0 to existing One-Transistor
* Model with Capacitor.
*
**************************************************************
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect


* Driving Control Signals


* Controls signals for the One-Transistor Model with Diode
**********************************************************

* Ideal power signal to bitline
*******************************

Vb1 3 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
Vb2 6 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
Vb3 9 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
Vb4 12 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
Vb5 15 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
Vb6 18 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
Vb7 21 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
Vb8 24 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
Vb9 27 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
Vb10 30 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)
```

```
Vb11 33 0 PULSE(0 2 0 100PS 100PS 2000PS 10mS)

* vw* is the Read/Write Pulse for Diode models
**************************************************

Vw1 4 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)
Vw2 7 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)
Vw3 10 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)
Vw4 13 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)
Vw5 16 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)
Vw6 19 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)
Vw7 22 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)
Vw8 25 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)
Vw9 28 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)
Vw10 31 0 PULSE(-1.2 0 1000PS 100PS 100PS 400PS 10mS)


* vw2 is the Read/Write Pulse for the capacitor model
**************************************************

Vw11 34 0 PULSE(-1.2 0 1000PS 100PS 100PS 500PS 10mS)

* One Transistor Model with Diode
***********************************

* Note each group uses a different diode gate length
* with gate width set to w = 52.0

j1  3  4  5  0 dp1.3  l=2.8  w=150.0
j2  5  0  5  0 dp1.1  l=1.0 w=52.0
c2  3  0  1000FF

j3  6  7  8  0 dp1.3  l=2.8  w=150.0
j4  8  0  8  0 dp1.3  l=5.2 w=52.0
c3  6  0  1000FF

j5  9  10  11  0 dp1.3  l=2.8  w=150.0
j6  11  0  11  0 dp1.3  l=12.0 w=52.0
c4  9  0  1000FF

j7  12  13  14  0 dp1.3  l=2.8  w=150.0
j8  14  0  14  0 dp1.3  l=16.0 w=52.0
c5  12  0  1000FF
```

```
j9  15  16  17  0  dp1.3  l=2.8  w=150.0
j10  17  0  17  0  dp1.3  l=20.0 w=52.0
c6  15  0  1000FF

j11  18  19  20  0  dp1.3  l=2.8  w=150.0
j12  20  0  20  0  dp1.3  l=26.0 w=52.0
c7  18  0  1000FF

j13  21  22  23  0  dp1.3  l=2.8  w=150.0
j14  23  0  23  0  dp1.3  l=30.0 w=52.0
c8  21  0  1000FF

j15  24  25  26  0  dp1.3  l=2.8  w=150.0
j16  26  0  26  0  dp1.3  l=34.0 w=52.0
c9  24  0  1000FF

j17  27  28  29  0  dp1.3  l=2.8  w=150.0
j18  29  0  29  0  dp1.3  l=38.0 w=52.0
c10  27  0  1000FF

j19  30  31  32  0  dp1.3  l=2.8  w=150.0
j20  32  0  32  0  dp1.3  l=42.0 w=52.0
c11  0  1000FF

* One Transistor Model with Capacitor
**************************************

j21  33  34  35  0  dp1.1  l=1.2 w=150.0
c1  35  0  2400FF
c12  33  0  1000FF

* This is the Temperature Flag that sets simulation temp to
* 85 degrees centigrade
.temp 85.0

* The .probe command ensures that only the listed siganls are saved
* for evaluation
.probe v(3) v(5) v(8) v(11) v(14) v(17) v(20) v(23)
.probe v(26) v(29) v(32) v(35)

* The .tran command tells the simulation to run for 3000 nanoseconds
* and save data recordings every 50000 picoseconds
```

```
.tran 100n 1ms

* The following line sets up the scale of devices to microns
* enables HSPLOT interface
* prints table of single plate nodal capacitances
* and reduces output to just the probe variables
.options scale=1E-06 post captab gmindc=1E-11 probe
.end

*********************************************************
```

C. HPSICE FULL CELL CHARACTERISTICS

```
*     file: memfull.sp
*     HSPICE Simulation for preliminary tests to confirm
*     read ONE operation and power requirements
*     new GaAs DRAM cell design
*
*********************************************************
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect


* Power sources for sense transistor
* Vdd is main power
* Vrefb is pre-charge for bit-line
* Vrefd is precharge for dummy cells
* Ve is gate voltage to equalizer
*******************************************

Vdd 1 0 2.0
Vref1 777 0 0.7    $ Bit-line precharge voltage
Vref2 888 0 0.26   $ Dummy-cell precharge voltage

*Vopu is the Odd BIT I/O Pull-up
Vopu 201 0 -1.2V

*Vepu is the Even BIT I/O Pull-up
*Vepu 200 0 -1.2V


*Vopd is the Odd bit line pull down
```

```
Vopd 203 0 0.0V


*Vepd is the Even bit line pull down
Vedd 202 0 0.0V


*Vsen is the sense amplifier sense signal
*VrcX is the read/write signal to memory cell X
*Vpre is the bitline/dummy-cell precharge & equalization signal

Vsen 189 0 -1.2V
Vrc1 152 0 -1.2V  $ Control signal for address 1
Vrc2 153 0 -1.2V  $ Control signal for address 2
Vrc3 154 0 -1.2V  $ Control signal for address 3
Vrc4 155 0 -1.2V  $ Control signal for address 4
Vrc5 156 0 -1.2V  $ Control signal for address 5
Vrc6 157 0 -1.2V  $ Control signal for address 6
Vrc7 158 0 -1.2V  $ Control signal for address 7

*Vrc signals are Read/Write signals to memory cells

Vpre 88 0  PULSE(-1.2 0 0PS 100PS 100PS 1300PS 1000ns) $precharges bitlines
Vepu 200 0 PULSE(-1.2 0 1500PS 100PS 100PS 1300PS 1000ns) $one enters even bitline
VrcX 151 0 PULSE(-1.2 0 1500PS 100PS 100PS 1300PS 1000ns) $reads one into even
mem-cell

* The following transistors make up the memory array

* The following transistors make up the sense amplifier
*************************************************************
j0  1   189  98  0  dp1.1 l=0.8 w=9.0   $ sense transistor
j1  1   189  99  0  dp1.1 l=0.8 w=9.0   $ sense transistor
j2  98   88  99  0  dp1.1 l=0.8 w=20.0  $ equalizing transistor
j3  98   99   0  0  enh.1 l=0.8 w=100.0 $ switching transistor
j4  99   98   0  0  enh.1 l=0.8 w=100.0 $ switching transistor

* The following transistors make up the memcell support
*************************************************************
j5  1   201  99  0  dp1.1 l=0.8 w=150.0  $ odd bit I/O pull up transistor
j6  1   200  98  0  dp1.1 l=0.8 w=150.0  $ even bit I/O pull up transistor
j7  99  203   0  0  enh.1 l=0.8 w=20.0   $ odd bit I/O pull down transistor
j8  98  202   0  0  enh.1 l=0.8 w=20.0   $ even bit I/O pull down transistor
```

```
j9  777  88  99  0  dp1.1 l=0.8 w=10.0  $ odd bit I/O precharge transistor
j10 777  88  98  0  dp1.1 l=0.8 w=10.0  $ odd bit I/O precharge transistor
j11 888  88  53  0  dp1.1 l=0.8 w=3.0   $ odd dummy-cell precharge transistor
j12 888  88  52  0  dp1.1 l=0.8 w=3.0   $ even dummy-cell precharge transistor
j13 99  151  53  0  dp1.1 l=2.0 w=6.0   $ odd dummy-cell sense transistor
j14 98  152  52  0  dp1.1 l=2.0 w=6.0   $ even dummy-cell sense transistor
j15 53   0  53  0  dp1.2 l=2.0 w=4.0   $ odd dummy-cell
j16 52   0  52  0  dp1.2 l=2.0 w=4.0   $ even dummy-cell

* The following transistors make up the memory cell
*************************************************************
j17 99  152  21  0  dp1.2 l=2.0 w=100.0  $ odd memory cell sense transistor
j18 98  151  20  0  dp1.2 l=2.0 w=100.0  $ even memory cell sense transistor
j19 21   0  21  0  dp1.3 l=30.0 w=52.0  $ odd memory cell
j20 20   0  20  0  dp1.3 l=30.0 w=52.0  $ even memory cell

j21 99  154  23  0  dp1.2 l=2.0 w=100.0  $ odd memory cell sense transistor
j22 98  153  22  0  dp1.2 l=2.0 w=100.0  $ even memory cell sense transistor
j23 23   0  23  0  dp1.3 l=30.0 w=52.0  $ odd memory cell
j24 22   0  22  0  dp1.3 l=30.0 w=52.0  $ even memory cell

j25 99  156  25  0  dp1.2 l=2.0 w=100.0  $ odd memory cell sense transistor
j26 98  155  24  0  dp1.2 l=2.0 w=100.0  $ even memory cell sense transistor
j27 25   0  25  0  dp1.3 l=30.0 w=52.0  $ odd memory cell
j28 24   0  24  0  dp1.3 l=30.0 w=52.0  $ even memory cell

j29 99  158  27  0  dp1.2 l=2.0 w=100.0  $ odd memory cell sense transistor
j30 98  157  26  0  dp1.2 l=2.0 w=100.0  $ even memory cell sense transistor
j31 27   0  27  0  dp1.3 l=30.0 w=52.0  $ odd memory cell
j32 26   0  26  0  dp1.3 l=30.0 w=52.0  $ even memory cell

* This is the Temperature Flag that sets simulation temp to
* 85 degrees centigrade
.temp 85.0
```

```
* The .probe command ensures that only the listed signals are saved
* for evaluation
.probe  v(88) v(200) v(151) v(98) v(99) v(20) v(21) v(52) v(53)
.probe tran p(Vdd) p(Vpre) p(Vepu) p(VrcX) power
.probe I(Vdd) I(Vpre) I(Vepu) I(Vrcx) current

* The .tran command tells the simulation to run for 1000 nanoseconds
* and save data recordings every 1 nanosecond
.tran 1ns 1000ns

* The following line sets up the scale of devices to microns
* enables HSPLOT interface
* prints table of single plate nodal capacitances
* and reduces output to just the probe variables
.options scale=1E-06 post captab gmindc=1E-6 probe
.end
```

APPENDIX D. MAGIC FILES

This appendix contains a small depiction of the modified DRAM chip. Complete files are located in chip, storage, support, padring, clock drivr1, driver2, cm2, cm3, refresh, output and cell MAGIC files.

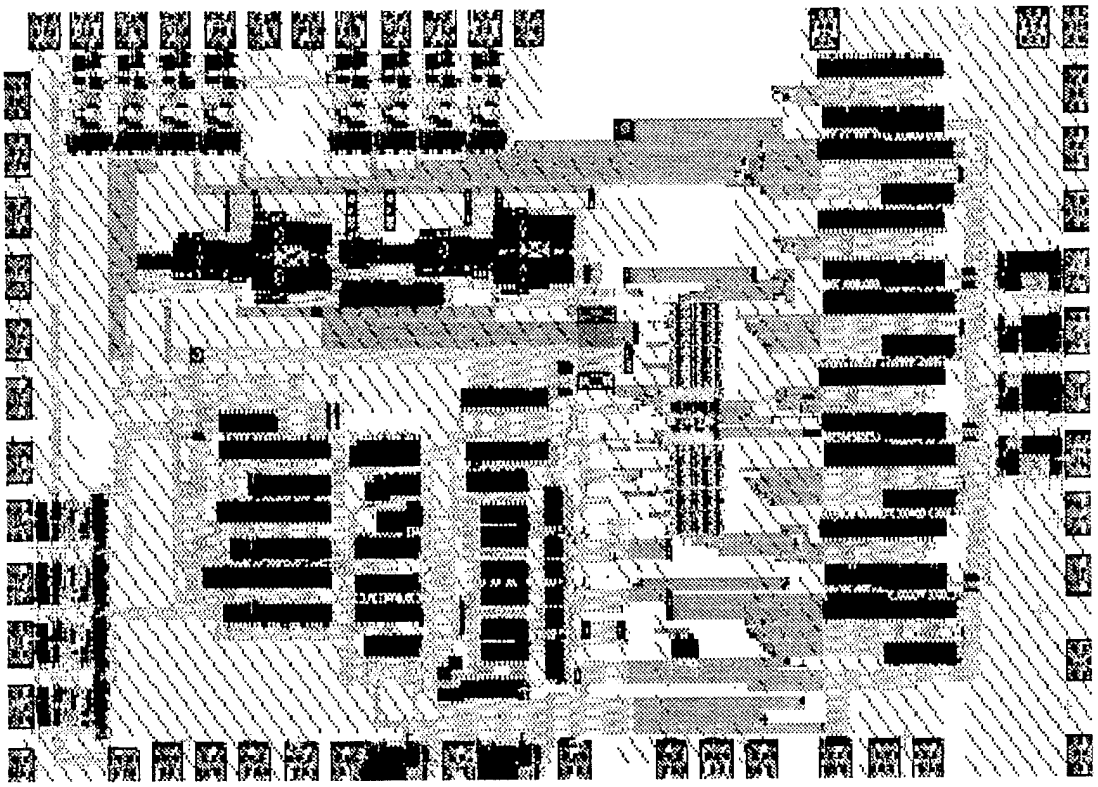


Figure D.1. Modified GaAs DRAM

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