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Navy Satellite (PANSAT)

Space Systems Academic Group

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NAVAL POSTGRADUATE SCHOOL
PETITE AMATEUR NAVY SATELLITE
NASW-4435
(PANSAT)

NASA/USRA University Advanced Design Program
Final Design Report
Summer 1989

Naval Postgraduate School
Space Systems Academic Group
Monterey, California

(NASA-CR-186049) PETITE AMATEUR NAVY
SATELLITE (PANSAT) Final Report (Naval
Postgraduate School) 21 p CSCL 22B

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NAVAL POSTGRADUATE SCHOOL PETITE AMATEUR NAVY SATELLITE (PANSAT)

A. BACKGROUND

The Naval Postgraduate School's (NPS) Space Systems Academic Group (SSAG) is designing and developing a small communications satellite for launch aboard the Shuttle as a Complex Self-Contained Payload (CSCP). The objectives of PANSAT are three-fold. First, PANSAT will provide an ideal educational tool for the officer students at NPS supporting Space Systems Engineering and Space Systems Operations with hands-on hardware development. Secondly, the satellite will provide digital store-and-forward communications, or Packet Radio, for the amateur radio community. The third objective is to provide a low-cost, space-based platform for small experiments.

PANSAT will be launched from the Shuttle at a nominal altitude of 200 nmi. and an inclination of at least 37°. The satellite weight is 150 lbs. Since there is no attitude control, eight dipole whip antennas will be used to provide isotropic ground coverage for communications. FM digital communications will be used with up-link and down-link on a single frequency in the amateur band of 144 to 146 MHz or 437 to 438 MHz. A maximum 50 kHz of bandwidth is envisioned for the satellite. The expected lifetime of the satellite is 1 1/2 to 2 years before atmospheric reentry. The PANSAT design consists of the following:

- Communications Subsystem (COMM)
- Computer, or Data Processor & Sequencer (DP&S)
- Power Subsystem
- Structure Subsystem
- Experiment Payload

B. DESIGN SUMMARY

Much of the design and analysis has already been completed on PANSAT in the areas of the computer subsystem and structure subsystem. Further detailed design of the power and communications subsystems will naturally follow with an assigned frequency. The initial design and detailed specifications of the subsystems are as follows.

1. Communications (COMM)

The COMM design began with an application for a frequency allocation within the amateur band of 144 to 146 MHz through the Naval Electromagnetic Spectrum Center (NAVEMSCEN). Pursuant to the NAVEMSCEN response, formal coordination with the Radio Amateur Satellite Corporation (AMSAT) was made in the form of a proposal for PANSAT as an amateur satellite. The proposal is currently under review.

The amateur frequency bands are desirable for PANSAT because atmospheric attenuation contributes very little to path losses associated with the link equations [Ref. 1: p. 45]. For example a 144 MHz signal received at 0° elevation (line-of-sight) from a satellite in a 200 nmi circular orbit has a free space loss of 142.5 dBW whereas the atmospheric attenuation is only 1.06 dBW. In working with the amateur community, PANSAT will support the AX.25 communications protocol [Ref. 2], a standard for amateur digital communications. In addition, exercising up-link and down-link on a single frequency is hoped to reduce ground coverage interference which is a major regulatory concern.

2. Data Processor & Sequencer (DP&S)

Design issues for the processor [Ref. 3] include commonality, upward compatibility, and a real time clock. Commonality deals with choosing a

processor which is currently available and in extensive use. In addition, high level language compilers must be available. The processor should be upwardly compatible for ease of expansion for more demanding future missions, including multiple processor configurations. A real time clock is required for specific scheduled events in the satellite's mission.

Although PANSAT will be in a Low Earth Orbit (LEO), prime consideration is given for a microprocessor which is available in a radiation hardened version. This is important in the concern for upward compatibility as well as guarding against single event upsets (SEU). The processor selected is based on the Intel 8086 processor [Ref. 4] which is available in a CMOS radiation hardened version, (the Harris 80C86RH) [Ref. 5]. Processor interfaces will be required with the communications subsystem, power subsystem, experiments, and structure subsystem for available space. The mission requirements of PANSAT allow the processor to run in the minimum mode utilizing a single processor, fewer support chips, and having direct control over read and write signals.

As stated earlier, the AX.25 communications protocol will be implemented to support the standard for amateur digital communications. The AX.25 protocol is a bit oriented protocol and is a variation of the X.25 protocol but having additional address bits to accommodate the user call signs and any repeaters. AX.25 uses go back N format, where N is eight. The throughput, ρ , for this format is given by [Ref. 6: p. 222]:

$$\rho = \frac{1-P}{1 + \frac{2T_p P}{T_f}}$$

- P : Frame error probability given by: $P = 1 - (1 - P_b)^{Nb}$
 P_b : Probability a single bit is in error

- Nb*: Number of bits in a frame
Tf: Time required for transmission of a frame
Tp: Propagation and processing delay

Assuming a ten percent overhead, a minimal AX.25 frame will have 20 bytes of overhead and 1600 bits of information. As bit error rate increases, throughput drops rapidly. Frame error probability for AX.25 can be reduced by decreasing frame size, however, the 20 byte overhead cannot be avoided. Overhead could actually increase to as much as 76 bytes if addressing through repeaters is used. As long as single bit error probability remains below 3×10^{-4} , throughput for AX.25 is acceptable. Implementation of the AX.25 protocol can be done using a CMOS serial communications controller (SCC) [Zilog Z80C30 or Z85C30] [Ref. 6: p. 222] chip which requires low power and is expected to be released late 1989 in a high-reliability JAN version.

Communication tasks required of the processor include adding messages to the buffer, retrieving messages from the buffer, listing buffer messages, issuing satellite commands or loading a program, and transmitting telemetry data. The DP&S must also have positive control of the transmitter. This is a necessary function to eliminate RF ground interference should the transmitter fail in the transmitting mode. Housekeeping duties will include monitoring such things as the voltage on battery packs, charging current, power supply current draw, and bus voltage.

Memory for the DP&S is divided into three sections. The first section is the fixed storage (PROM) holding the operating system kernel. The other two sections are the vital RAM which holds system vital data, and non-vital RAM which holds the messages and telemetry data. The PROM and vital RAM will be high-reliability versions if not radiation hardened.

A watchdog timer will be used to safeguard against processor failure and subsequent transmitter keying [Ref. 7]. The timer will be reset by the processor in periodic intervals during normal operation. A completed countdown of the watchdog timer will initialize the processor and secure control of the transmitter. The periodic timer count reset will not be an interrupt function but rather a normal function of the operating system. The watchdog timer circuit can be accomplished by using a 82C54RH programmable interval timer. Other peripherals in the DP&S include analog/digital (A/D) converters and parallel input/output (I/O) capability. Figure 1 shows the DP&S system concept.

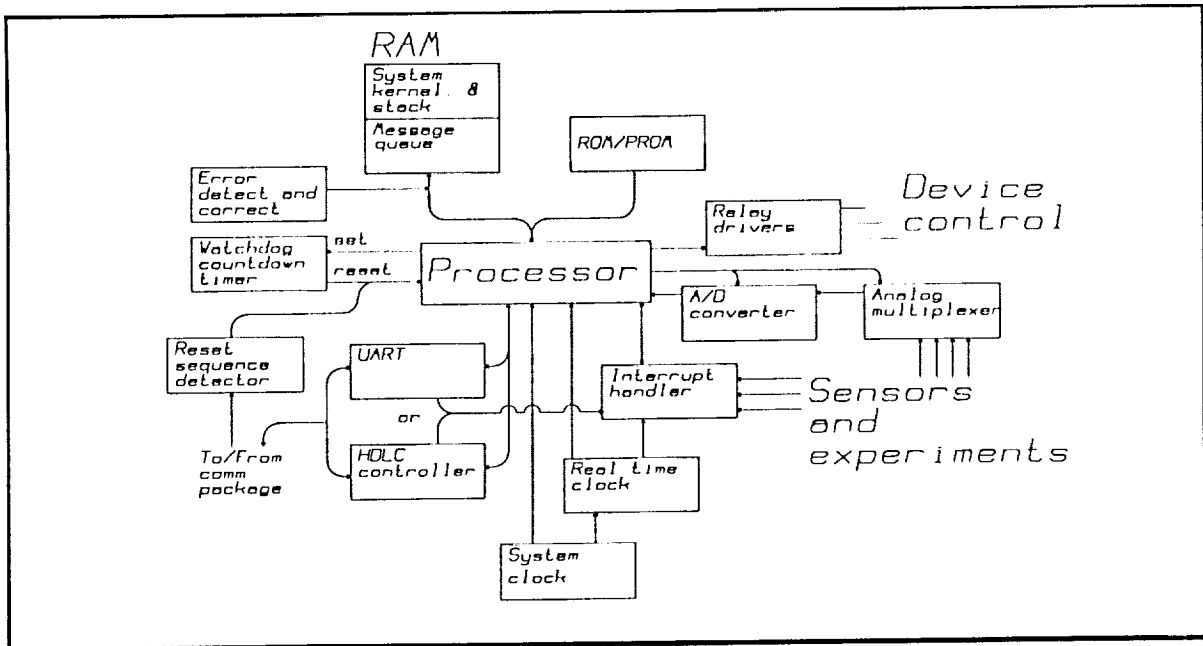


Figure 1. PANSAT DP&S System Concept

Software requirements for PANSAT include developing the operating system kernel and device drivers. Programming will be done in the Ada language which is the Department of Defense standard. Development of the kernel includes creating the interrupt routines, and user interface shell. Device drivers will be responsible for controlling mass storage, radio communications, experiment(s) and sensors, and power control. Software testing will be an

important consideration for breadboarding the DP&S hardware. Development of software flow charts will begin in the Summer quarter 1989.

3. Power

Power will be provided by a 12 volt unregulated bus from solar cells and batteries. Seventeen exposed panels will permit thirty-two (32) 2 cm x 4 cm cells per panel, or 256 cm² per panel for solar energy collection. Terrestrial batteries will be used to lower costs. This will require housing the batteries in a sealed container for safety and to accommodate the environmental specifications of the batteries. Using lead-acid batteries, six battery packs of six (2 volt, 5 Ah) cells each can fly on PANSAT having a total of 360 watt-hours capacity. Lead-acid batteries have been flown on the GLOMR satellite and a number of Shuttle Get Away Special (GAS) payloads as a matter of record. Terrestrial type Nickel-Cadmium batteries are also being investigated since they have shorter recharging times. Long cycle life is an important factor for charge and discharge periods while surveying applicable batteries. Some of the data requirements for battery use are as follows [Ref. 8: 14D1, p.2].

- Discharge voltage as a function of time under actual loads
- Charge voltage and current as functions of time under actual conditions, (or required for particular cell if conditions are as yet unavailable)
- Overcharge current requirements
- Quantity of electrical energy available from the battery at critical points in the mission and assurance availability exceeds requirements at all other times
- Rate of heat evolution as a function of time under the actual charge & discharge conditions expected; and a complete temperature profile of the battery as a function of time
- Impedance and phase-shift characteristics of the battery as a function of frequency
- Efficiency of the battery's energy storage and its associated electronics
- Probability of battery failure as a function of time and conditions of use
- Battery voltage transients for critical load changes

Orbital characteristics affect the power subsystem mainly in establishing the thermal environment the satellite will face and the amount of solar energy flux. For the satellite in a circular orbit at 200 nmi (370 km) altitude, the approximate time of eclipse is 36.2 min. (2172 sec), or 39.4 % of the period (ignoring inclination). Since the satellite is in LEO and will be tumbling, the thermal environment may not be a great concern. However, an analysis will be needed to determine the range of temperatures the satellite will encounter in order to select subsystem components or allow for active thermal control where applicable.

While in the sun, the average power is expected to be about 19.5 W assuming a tumbling rate of 0.1 rad per sec. and solar cell efficiency of 12 %. This should be more than adequate for normal operation. While in darkness, PANSAT will need to rely on power from its batteries. The power budget and further detailed design will proceed when the communications frequency has been assigned and communications components have been selected.

4. Structure Subsystem

The PANSAT structure will be aluminum 6061-T6 and fabricated at NPS. The design uses modularity to ease fabrication. Five (5) structural elements are used: two (2) plates, eight (8) support structures, four (4) plate supports, four (4) lower support struts, and two (2) end blocks. A wood mock-up of the structure has been completed showing allowable subsystem envelopes. The total weight of the structure will be about 45 lbs.

A finite element analysis of the structure was done using GIFTS interactive software to show that PANSAT will survive loads of ± 9 g's translational accelerations in the X (and X+Y) direction, and ± 14 g's in the Z direction. See Figure 2. The loads prescribed are found in the GAS Safety Manual for a GAS payload [Ref. 9: p.A5]. Results show that the structural

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deflections remain in the linear regime. Stress concentrations occur in the corners of the frame-like support structures. Because of the magnitudes of those stress concentrations the lower struts were added.

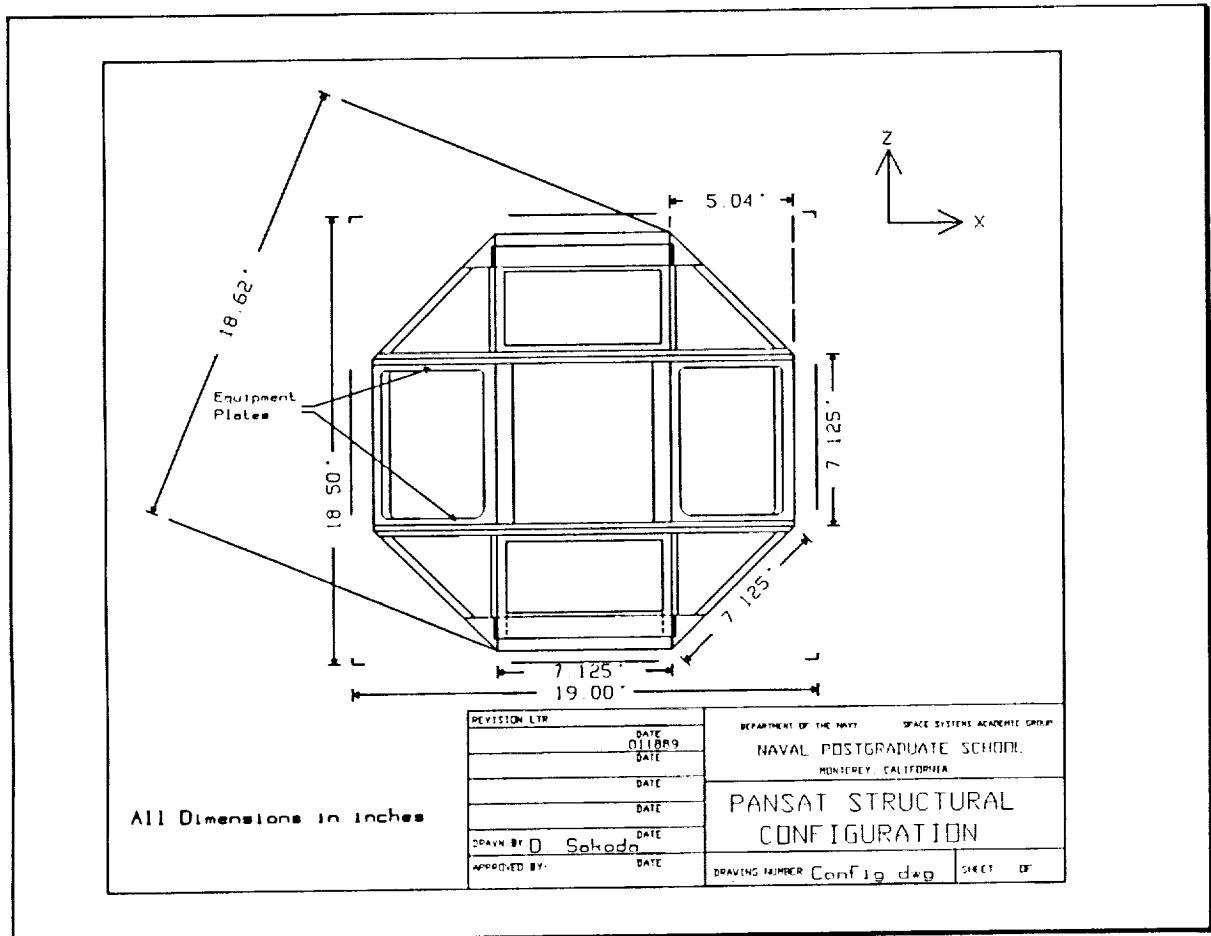


Figure 2. PANSAT Structural Configuration.

Future work for the structure subsystem include fabrication of the actual flight structure and performing dynamic & vibration testing. Structural testing will begin early 1990 at NPS. Currently, test plans are being developed within the capabilities of NPS facilities. The major portion of testing will deal with qualification testing. Additional testing may be required and can be done at the Naval Research Laboratory. The test plan will need to include test objectives, type and number required, data required from each test, degree of confidence

required, duration of each test, test sequence relative to design schedule, and facilities required.

5. Experiment Payload

PANSAT will be designed to support small experiments which have minimal power, weight, and space requirements. The major experiment will test on-orbit annealing of radiation damaged solar cells [Ref. 10]. Solar cells show recovery, (or annealing), from radiation damage when heated to extreme temperatures. By using a process called forward biased current annealing the temperatures required for annealing can be lowered appreciably. This gives hope for extending the life of solar cells resulting in considerable cost savings for future space systems. Three candidate solar cell types have been identified; namely, silicon, gallium arsenide, and indium phosphide.

The experiment has already been developed and is currently in the testing phase. Modifications have already improved size and weight of the experiment since its initial testing. The payload is an autonomous Motorola 68701 based experiment with 64 k of static RAM and 16 k of ROM. Fifteen (15) cells will be tested with a sixteenth cell used as a sun sensor. A novel circuit design for calculating current-voltage (I-V) curves will be used with curve accuracies within 2 mV from 12 bit analog to digital converters.

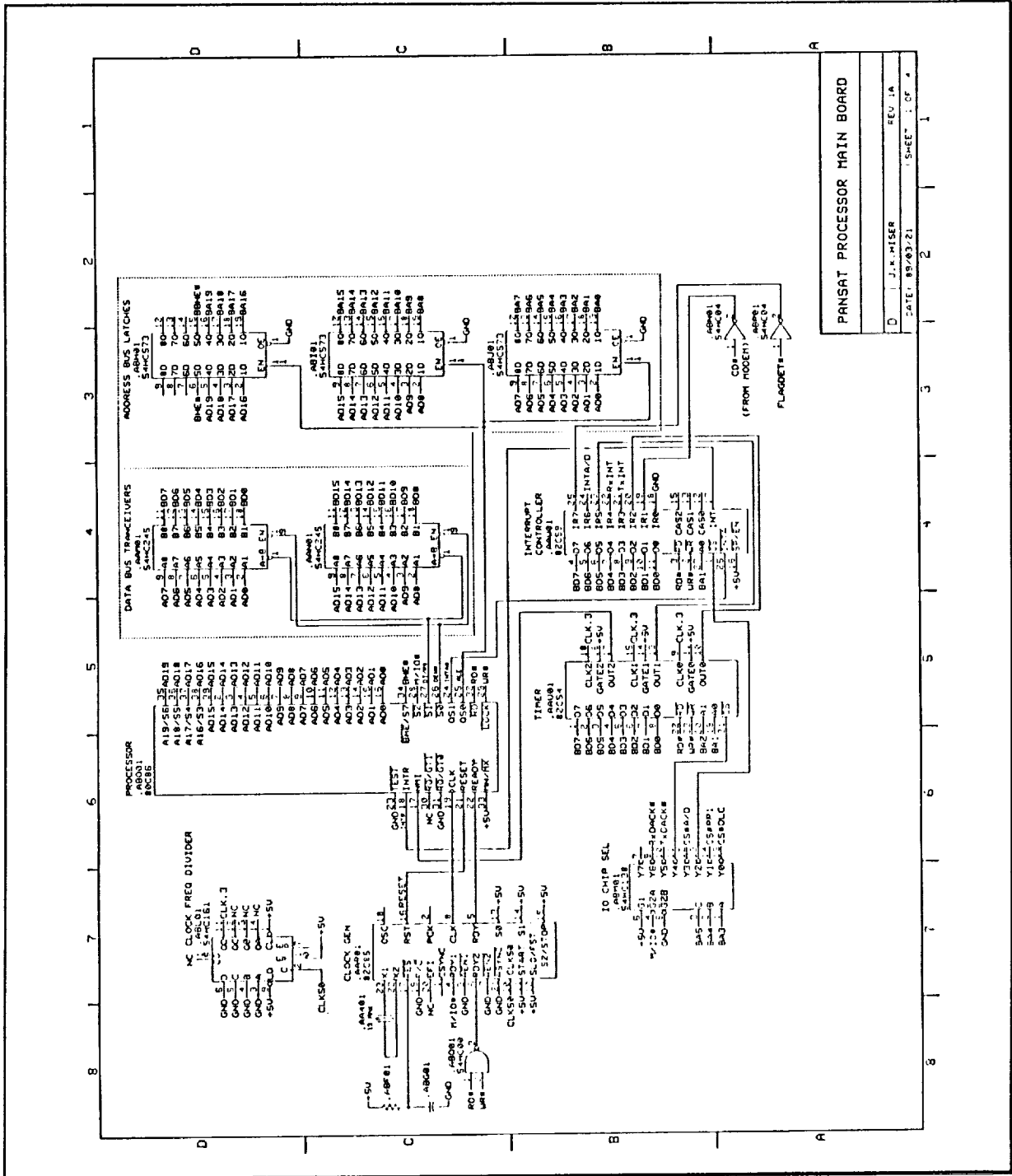
An additional experiment that may fly aboard PANSAT will test the new technology of Ferroelectric memory. This technology is attractive for space applications since it is inherently radiation tolerant, non-volatile and has high density. An actual experiment is still in the conceptual phase however. The major concerns for Ferroelectric memory devices are retention and endurance. If these issues can be overcome, Ferroelectric memory devices promise to be the unequivocal choice in solid state memory for space applications.

C. CONCLUSION

PANSAT development has begun with the satellite processor design and structural design. The groundwork for the other subsystem designs has been established articulating on initial design requirements. The project is currently funded by NPS under research for continuing satellite design studies at \$ 18 k, FY 89. Future funding will be provided by NASA/USRA, NPS and other sources to be determined. The total cost of hardware is expected to be \$ 100 k with a delivery date of July 1991. PANSAT was ranked #14 of 19 experiments at the Navy Space Test Program (STP) call for experiments, May 1989. As an academic exercise, PANSAT promises a wealth of knowledge and experience for the student officers involved. PANSAT also will provide a valuable asset for low cost access to space.

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APPENDIX



PANSAT PROCESSOR MAIN BOARD			
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Fig. A1. Processor Main Board

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The main processor board contains the 8086 μ processor, watchdog timer circuit, data bus transceivers, interrupt controller, and real time clock.

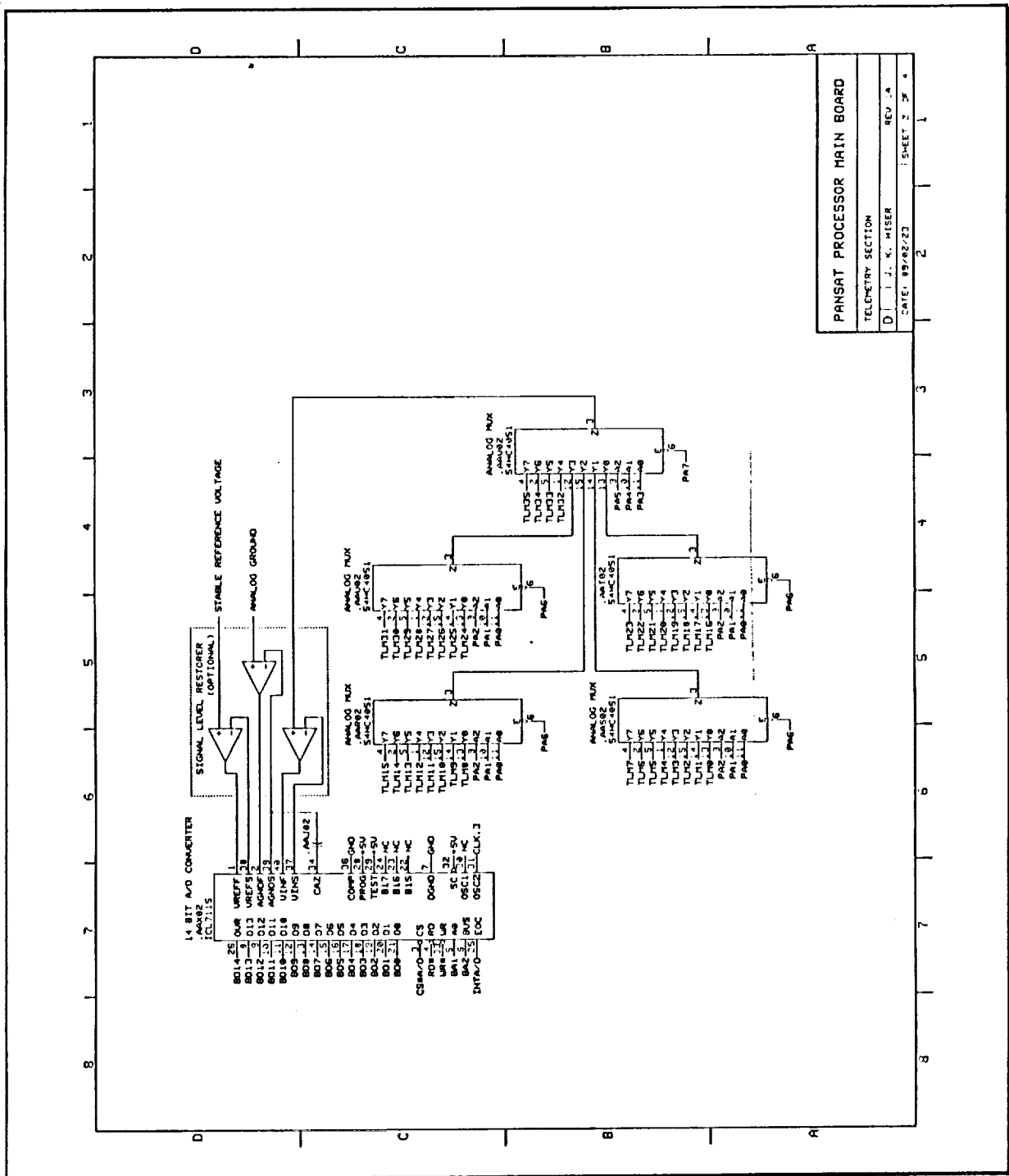


Fig. A2. Telemetry Section, (A/D converters)

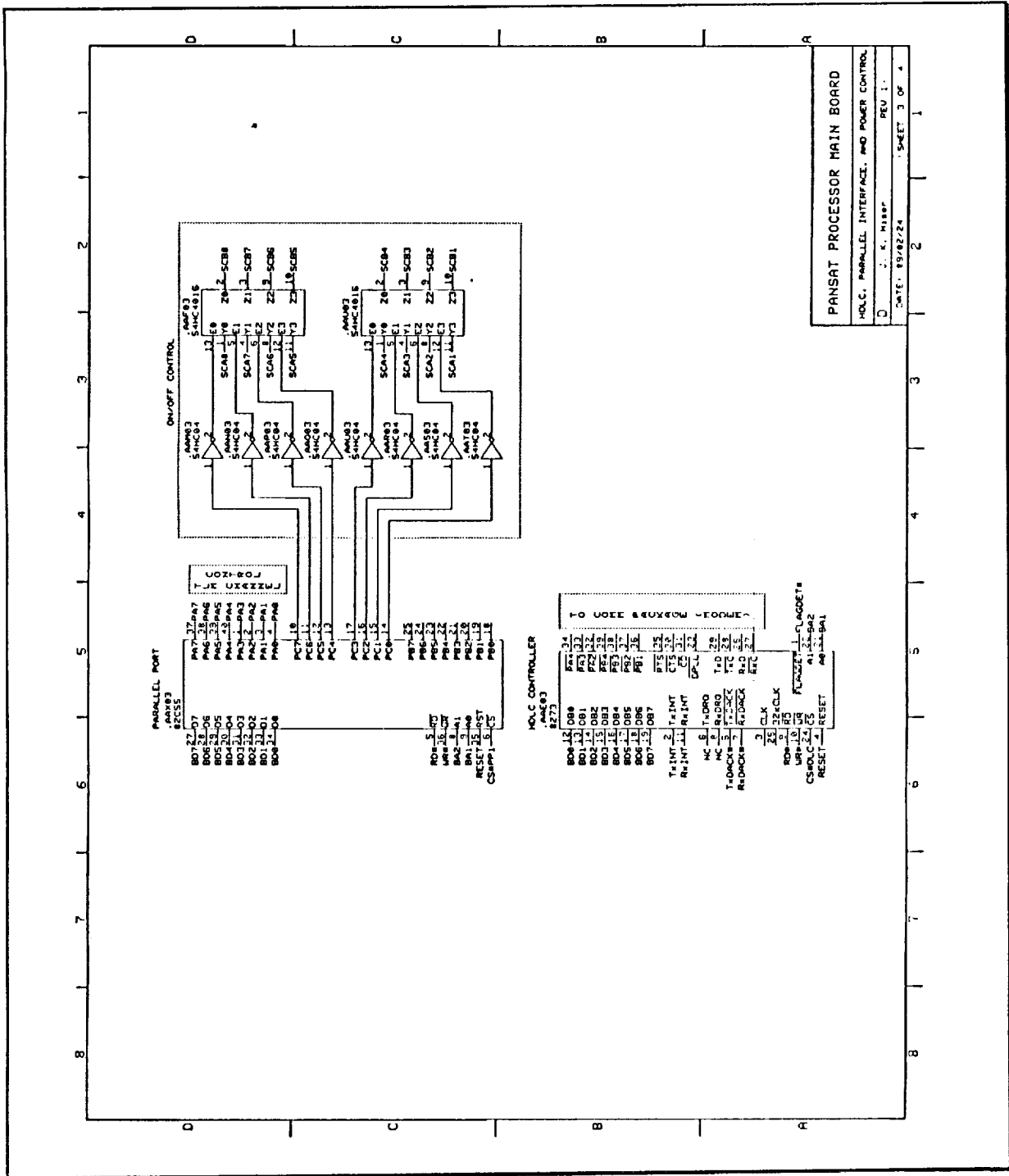


Fig. A3. HDLC, Parallel Interface, and Power Control

The HDLC 8273 protocol controller will be replaced by a CMOS version, SCC chip.

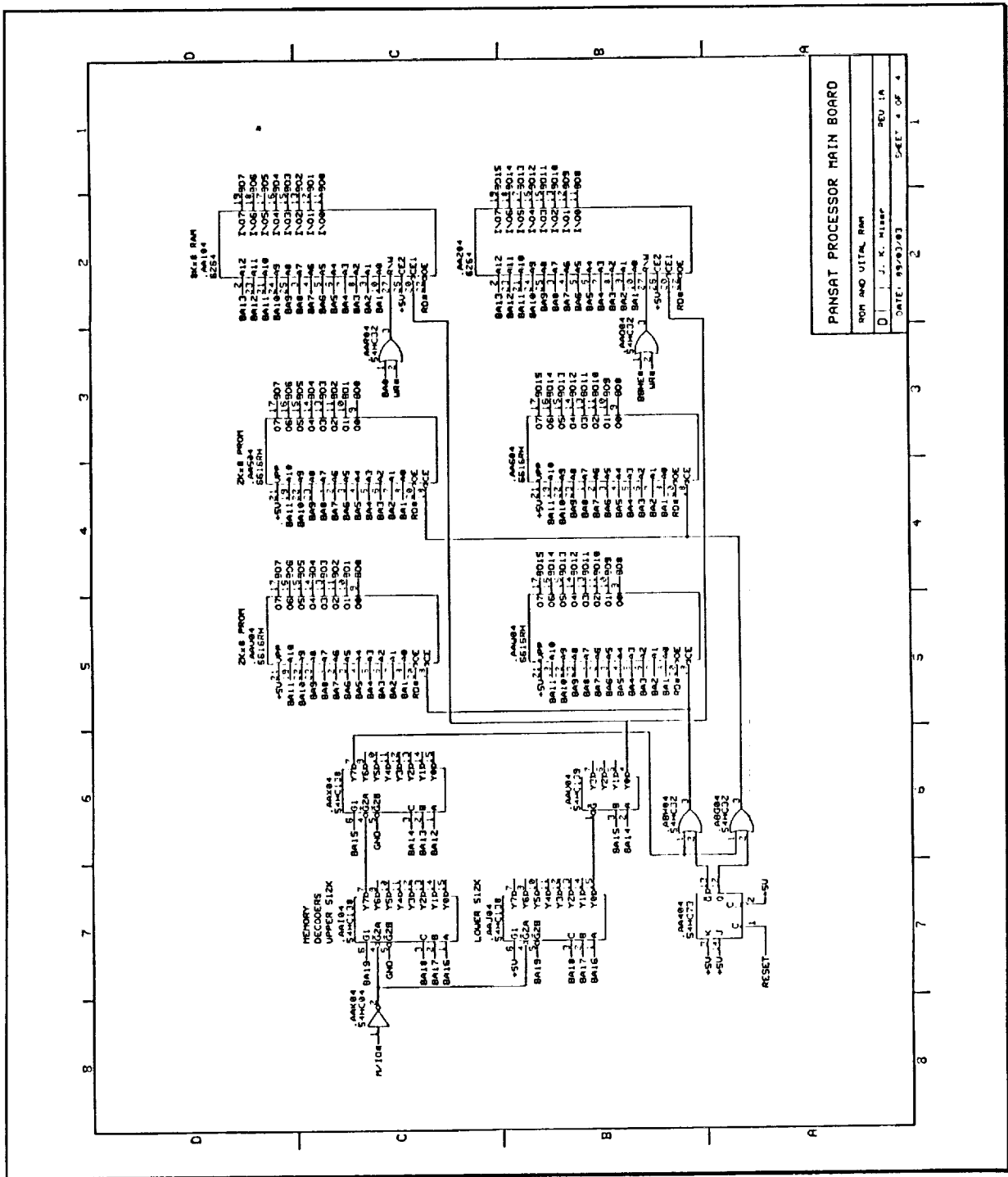
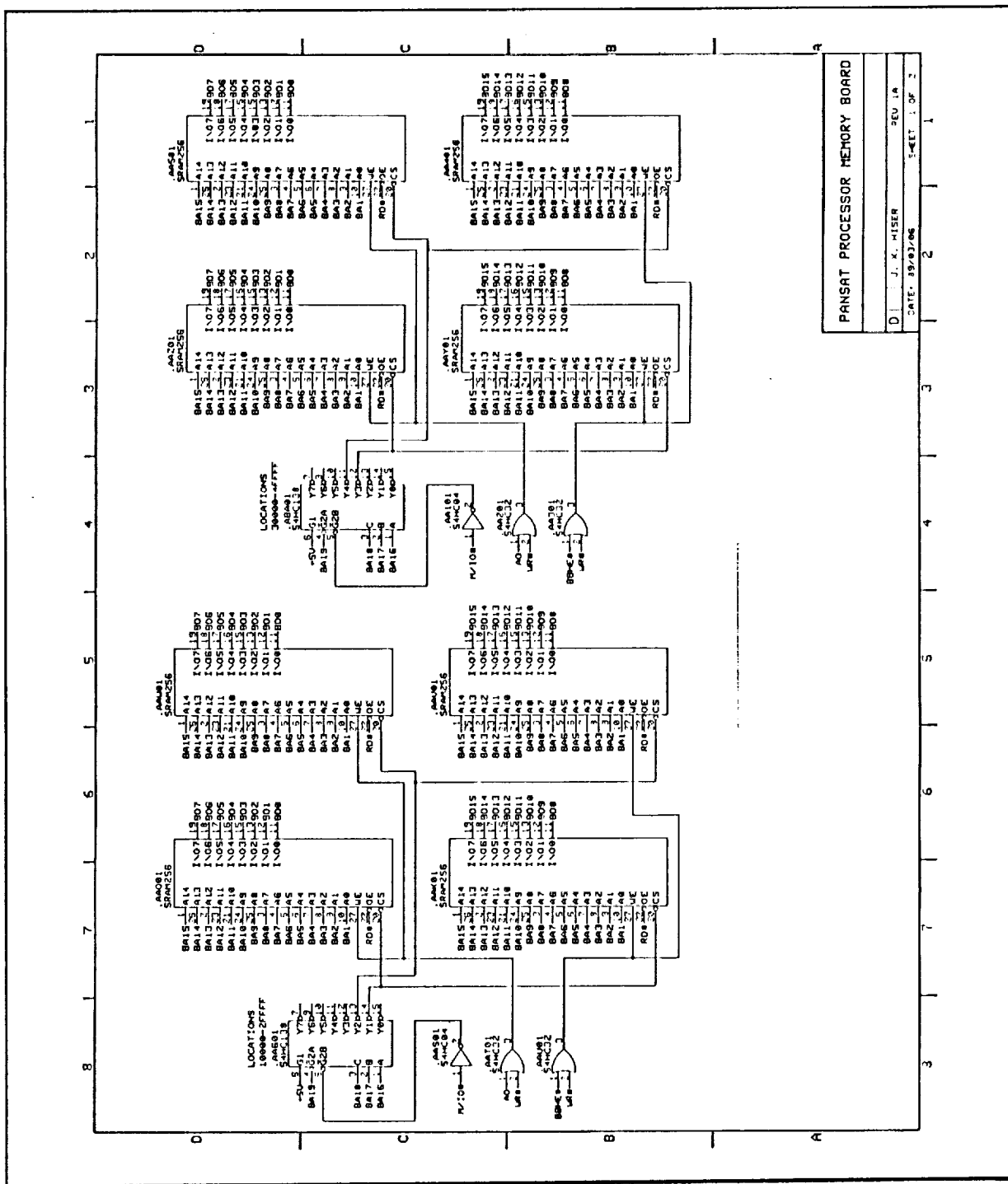


Fig. A4. ROM and Vital RAM
Radiation hardened components are designated by the 'RII' suffix.

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PANSAT PROCESSOR MEMORY BOARD
D | J. K. WISER | REV. 1A
DATE: 10/03/66 | SHEET 1 OF 2

Fig. A5. PANSAT Memory Board (Non-vital RAM)

Two boards will be used. Reliability is designed in by dividing the memory into four sections. Reliability is further attained by addressing where bad memory locations can be at the bottom of the stack.

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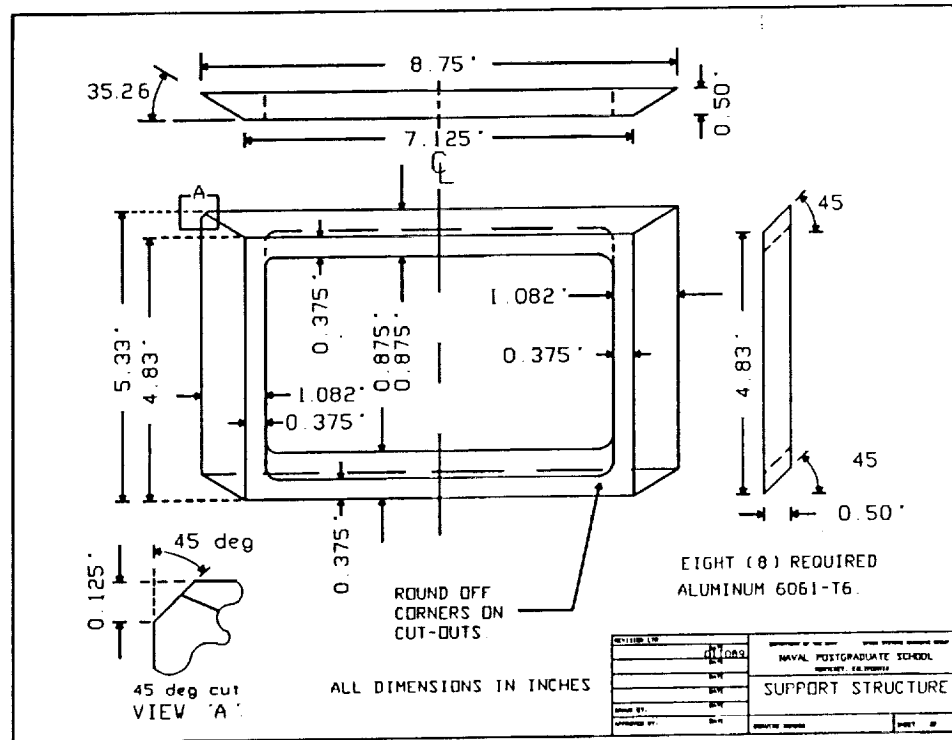
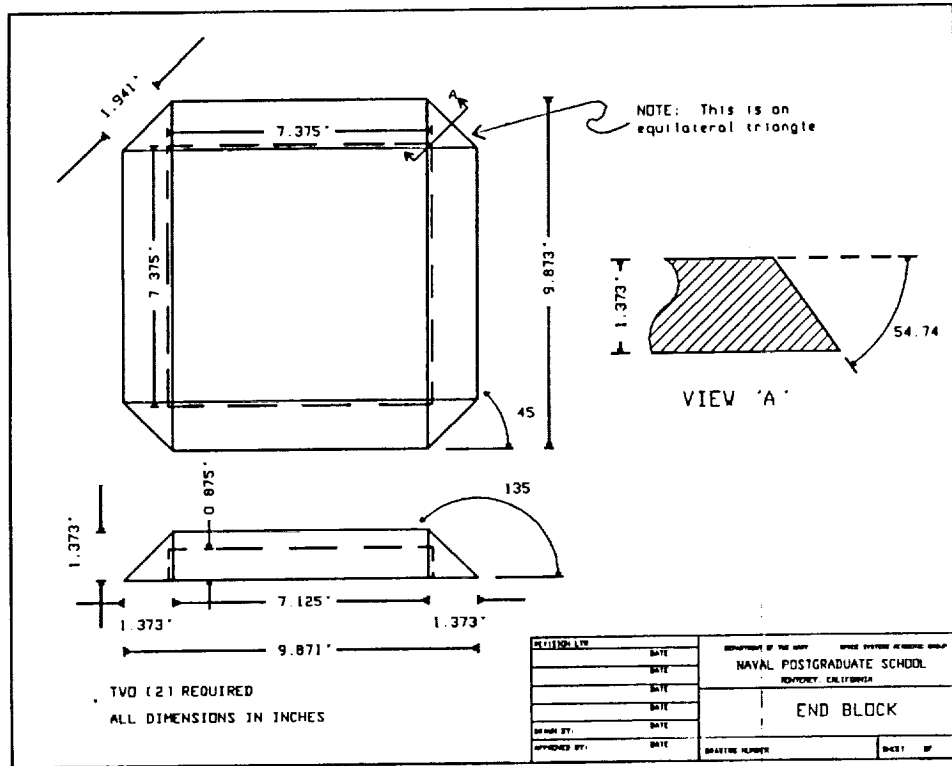


Fig. A6. PANSAT Structural Elements.

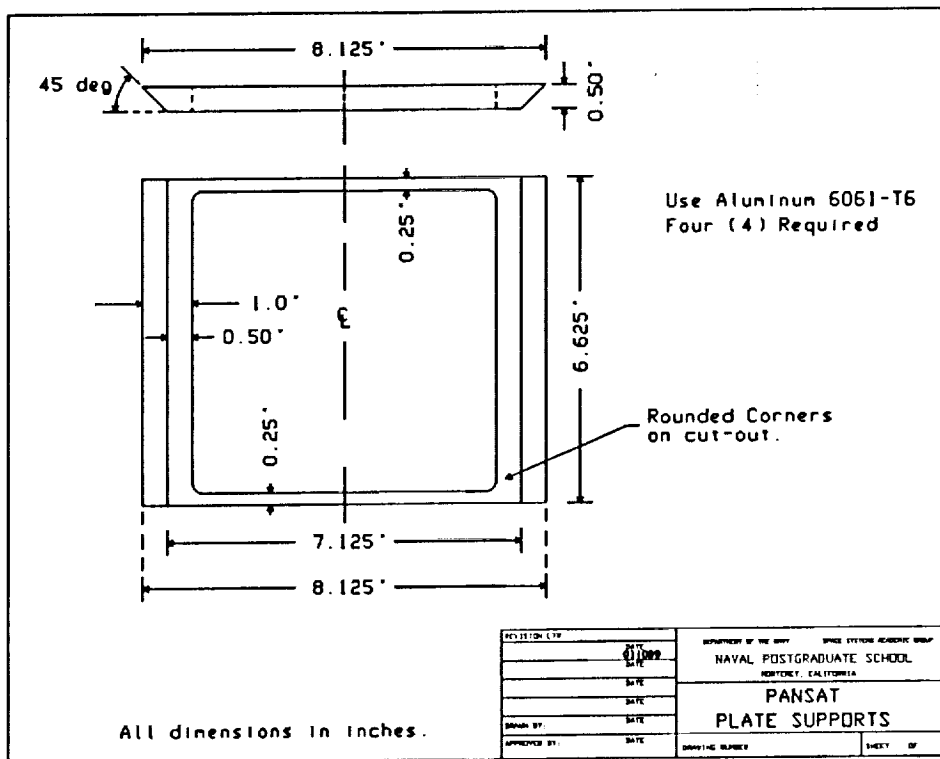
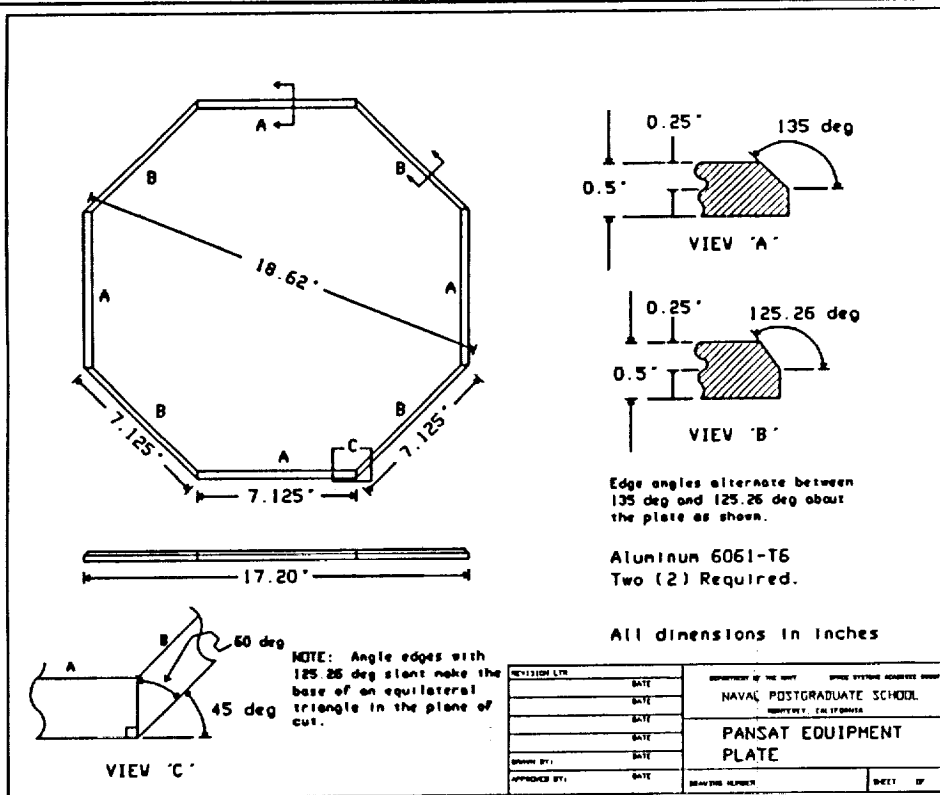
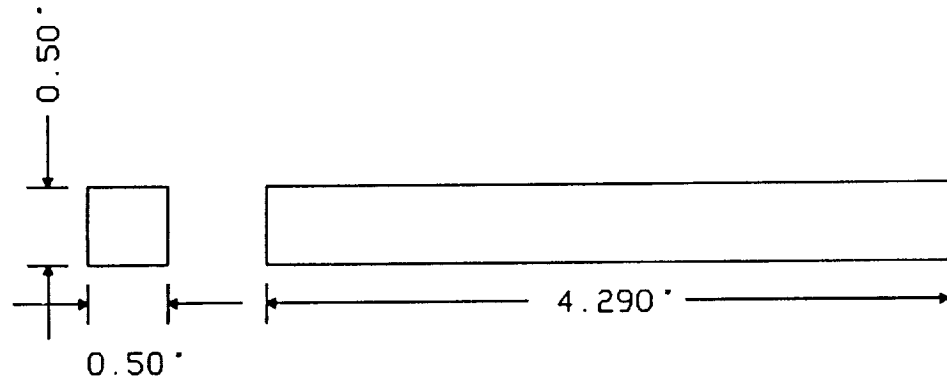


Fig. A7. PANSAT Structural Elements.

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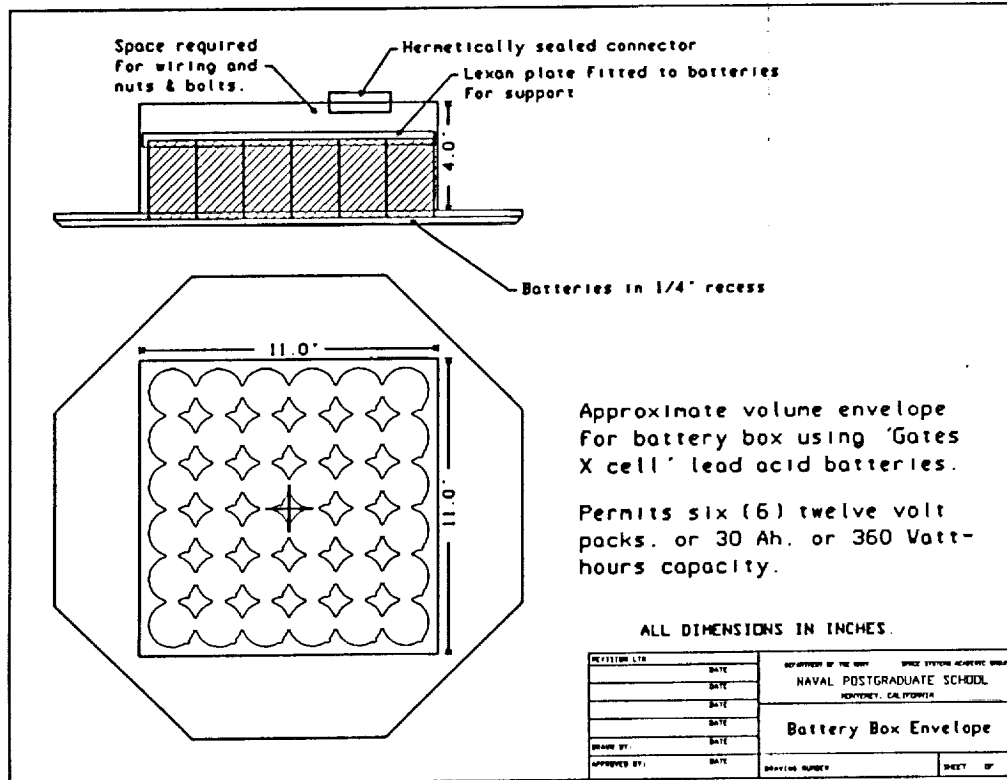
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Aluminum 6061-T6
Four (4) Required

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		MONTEREY, CALIFORNIA	
		LOWER SUPPORT STRUT	
DRAWN BY:	DATE:	DRAWING NUMBER:	SHEET OF:
APPROVED BY:	DATE:		



Approximate volume envelope
for battery box using 'Gates
X cell' lead acid batteries.

Permits six (6) twelve volt
packs, or 30 Ah, or 360 Watt-
hours capacity.

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DESIGNER: LTR	DATE:	DEPARTMENT OF THE NAVY	SPACE SYSTEMS ACADEMIC GROUP
		NAVAL POSTGRADUATE SCHOOL	
		MONTEREY, CALIFORNIA	
		Battery Box Envelope	
DRAWN BY:	DATE:	DRAWING NUMBER:	SHEET OF:
APPROVED BY:	DATE:		

Fig. A8. PANSAT Support Strut and Battery Volume.

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