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Soft Error Immune GaAs Circuit Technologies

T.R. Weatherford, D.J. Fouts, P.W. Marshall¹, C.J. Marshall² and H. Dietrich²

Naval Postgraduate School, Monterey, CA

¹SFA, Inc. Lanham, MD

²Naval Research Laboratory, Washington, DC

Abstract

Cosmic radiation induced soft errors present a major difficulty for space applications that utilize digital GaAs circuits and systems. Techniques to reduce soft error sensitivity by 5 orders of magnitude or more, to sufficient levels for safe implementation of GaAs ICs in space applications are presented. These results show that the need for redundancy and error correction is eliminated. Space systems will benefit by reduced power and area requirements, plus a substantial improvement in system performance over present radiation hardened silicon-based technologies.

I. INTRODUCTION

Non-permanent errors induced in space-based microelectronic circuits by cosmic particles are referred to as soft errors or single event upset (SEU) [1]. Soft errors are localized non-permanent effects unlike total ionizing dose effects which produce permanent failures by threshold voltage shifts or transconductance degradation. Single ionizing particles known as heavy ions (cosmic rays), or highly energetic particles such as Van Allen Belt protons colliding with lattice atoms can create sufficient ionized charge in an "off" transistor to switch the transistor to an "on" state. This unintentional switching of the transistor can develop erroneous logic states in a bistable circuit or unexpected pulses in a clocked circuit. Soft error effects may range from interrupting noncritical operations, to rendering satellite systems useless until restarted [2].

Techniques to mitigate the sensitivity of soft error effects such as logic gate redundancy at the circuit level, or majority voting and error correction/detection at the system level can compromise system performance. Shielding can incur a serious weight constraint while only limiting the lowest energy particles. Circuit and system level solutions normally include tradeoffs in functionality, power and weight. Device level techniques that do not require these tradeoffs are the most preferable, although they are the most difficult to implement in an IC fabrication process.

To provide a measure of soft error sensitivity, Figure 1 portrays the soft error rate for various technologies against

each power-speed product. The preferable technology for space applications would be one that provides the lowest speed-power product and the lowest soft error rate (the lower left of Figure 1). The GaAs technologies, Complementary-Heterostructure Field Effect Transistor (C-HFET), Complementary-Enhancement Junction FET (C-EJFET), and Enhancement/Depletion METal Semiconductor FET (E/D MESFET), (the upper left of Figure 1) have shown high susceptibility to soft errors, even though these same technologies show excellent radiation hardness to total ionizing dose effects [3].

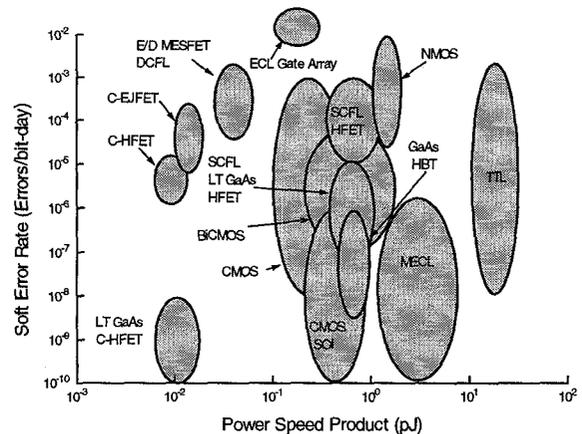


Figure 1 - Comparisons of several digital technologies soft error rate for static operation (i.e. non-clocked flip-flops) in geosynchronous orbit.

Most space systems require soft error rates below 10^{-8} errors/bit-day. A processor or ASIC which includes 10^5 gates may experience 100 errors a day in MESFET Direct Coupled FET Logic (DCFL), or 1 error a day in a C-HFET family. At clock frequencies of 400 MHz, soft error rates may increase by a factor of three [4]. As operating frequencies increase and power-speed products reduce, sensitivity to soft errors increases.

SEU sensitivity is related to several factors: energy transfer in the semiconductor, drift and diffusion of free carriers, transistor dimensions, noise margins, logic swings, capacitance, and the operating frequency of the circuit. In GaAs FET technologies, a progression of improved gate

barriers from a MESFET, to EJFET and HFET has allowed improved logic swings and noise margins which in hand reduced soft error rates, as shown in Figure 1. Figure 2 gives a device and circuit view of an error created by a passage of a cosmic particle through the transistor structure.

II. CIRCUIT AND DEVICE SIMULATION

To understand the mechanics of an upset, combined device and circuit simulations were performed. These simulations analyzed DCFL utilizing implanted GaAs MESFETs. Several physical mechanisms internal to the FET contribute to the terminal photocurrents such as photoconductivity, drift, diffusion, bipolar action, and back channel modulation [5]. Both the circuit components and device parameters interact, however the most critical of these effects in the GaAs FET is the existence of excess charge below the FET channel, specifically hole concentrations.

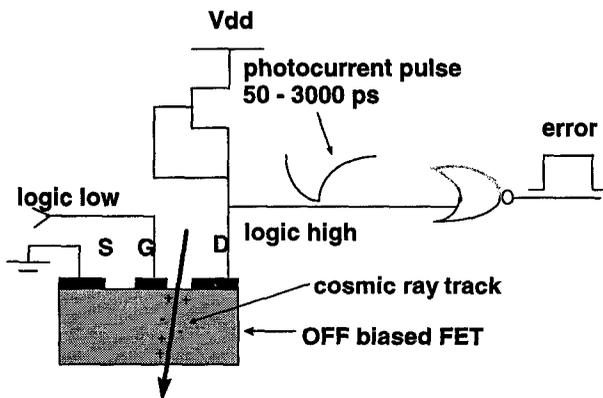


Figure 2 - Schematic of circuit analyzed in computer simulations and measurement.

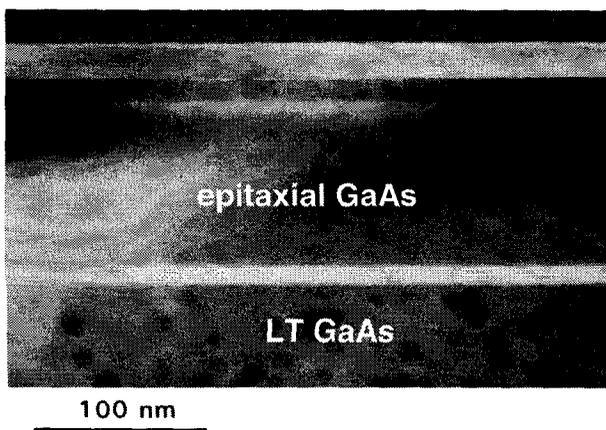


Figure 3 - A Transmission Electron Microscopy image of an LT GaAs FET structure.

One technique that has shown considerable advantages to reducing soft error rates in silicon technologies is silicon-

on-insulator (SOI) structures. However commercial SOI technologies are susceptible to total ionizing dose effects [6], unlike GaAs FET technologies [3].

In contrast to SOI which utilizes the SiO_2 insulator as a potential barrier, it was recognized that if materials with very high recombination rates were utilized as a buffer, the reduction in soft error rates may be more substantial than using an insulator [7]. A practical candidate was to use low temperature grown GaAs (LT GaAs) buffer layers beneath the transistor. This was accomplished by growing Molecular Beam Epitaxy (MBE) GaAs on a bulk GaAs wafer, then lowering the growth temperature to grow non-stoichiometric arsenic-rich GaAs. The low temperature growth is followed by a deposition of high quality epitaxial GaAs above the LT GaAs and an annealing step [8]. The purpose of the arsenic-rich material is to introduce complexes that trap and recombine excess electrons and holes. The effective carrier lifetime of the LT GaAs material is approximately 1-10 ps, several orders of magnitude lower than the bulk GaAs characteristic lifetime of 1 ns [9]. Ionized charge in the buffer layer recombines 2 to 3 orders of magnitude greater than in the substrate or in the upper epitaxial layer. A transmission electron microscopy photograph in Figure 3 shows a cross section of a heterostructure FET on a LT GaAs buffer. The lower region in the figure is where As precipitates are observed, a precursor to high recombination.

To model the effectiveness of utilizing LT GaAs buffers, combined device/circuit simulations were performed to understand both the effects of introducing a LT GaAs buffer below the transistor structure, and effects on charge collected on the circuit nodes. The software utilized was Silvaco's ATLAS™ and MIXEDMODE™ device and circuit simulators.

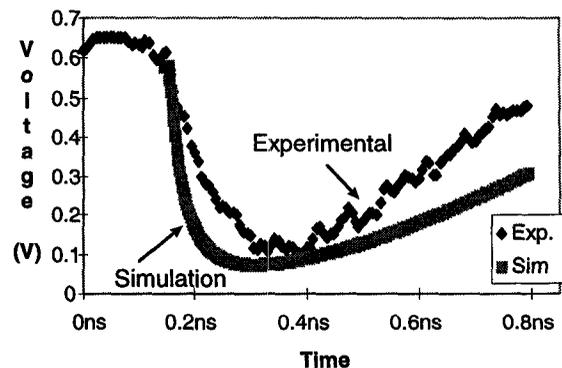


Figure 4 - Simulation and measurement of a soft error voltage transient on the output of a GaAs DCFL inverter

In addition to the computer modeling, actual picosecond time-resolved measurements were obtained inside a GaAs circuit to confirm modeling predictions on the standard technology. A time-resolved photoconductive probe was utilized to measure laser-induced voltage transients internal

to an integrated circuit to simulate a soft error event. Figure 2 provides the schematic for both the device and circuit modeling, and Figure 4 shows a comparison between simulation and measurement of a voltage transient at the output of a DCFL inverter. The initial fall is dependant on photoconductive and drift currents, whereas the eventual return to logic high is influenced by hole lifetimes and circuit time constants.

III. SOFT ERROR HARDENING APPROACH

Figure 5 illustrates the generic structure of the FET incorporating the LT GaAs buffer layer. Two MBE-based digital GaAs FET processes, the Motorola CGaAs™ [10] and the Honeywell CHFET [11] have implemented LT GaAs buffers, and have been measured for soft error effects. Additionally efforts to implement LT GaAs buffer layers into the implanted Vitesse HGaAsIII™ MESFET process are being pursued [12].

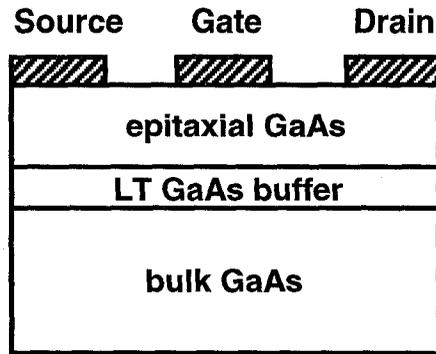


Figure 5 A generic transistor structure showing the location of a LT GaAs buffer.

For the MBE FET processes, the epitaxial wafer with the LT GaAs buffer is virtually identical to the original wafer. Because the LT GaAs buffer is implemented during the wafer growth, the IC fabrication process, layout masks, and circuit designs are unaltered. By substituting the initial wafer, a GaAs commercial process could be hardened for space radiation effects.

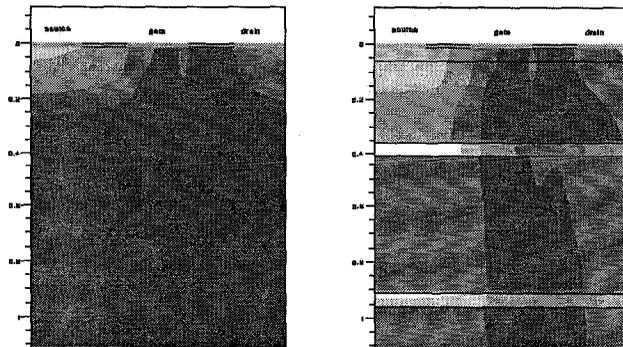


Figure 6 Hole concentration at 8 ps after an event for the conventional (left) and LT GaAs buffer structure (right).

Figure 6 shows the hole concentration of both types of GaAs MESFETs biased in an inverter. Notice that much lower hole concentrations exist in the LT GaAs structure after the initial event. The LT GaAs buffer essentially acts as a sink to absorb excess carriers.

IV. RESULTS

Several experiments have shown excellent reductions in soft error vulnerability for both the Motorola and Honeywell GaAs FET technologies [10,11]. These experiments are from the first iteration of implementing LT GaAs buffers in these technologies. Efforts are continuing in all of the mentioned processes and further improvements are expected. Heavy ion experiments on the Motorola technology has shown three to five orders lower soft error rates for digital GaAs logic operating at 200 to 300 MHz. These levels are equivalent to observing one error for 10⁶ bits every 4 months to 27 years respectively in geosynchronous orbit. The results on a Honeywell, C-HFET shift register operating at 68 MHz showed complete immunity to heavy ions [11]. These soft error rates are more than sufficient to meet the most stringent requirements for space based applications. It is interesting to note that these results are taken during dynamic operation of the GaAs test circuits, where soft error sensitivity is more pronounced than with static tests on memories or latches [4].

Table 1 lists present data available on digital GaAs circuits tested with LT GaAs buffers. Threshold Linear Energy Transfer (LET) in MeV/mg/cm² is the induced charge track density to initiate upset. The sensitive cross section is the sensitive area per bit and the soft error rate (SER) is estimated for geosynchronous orbits. We expect the improvements for the DCFL MESFET technology will not be as large as observed for the cases in Table 1, but SER improvements may be as much as 3 orders of magnitude.

Table 1-LT GaAs Soft Error Results

Tech.	LET (MeV/mg/cm ²)	Sensitive Cross Section (cm ² /bit)	SER (er/bit-day)	SER Improvement Factor
CGaAs™ [10]	12	1e-7	7.7e-8	1e5
CHFET™ [11]	90	<1e-9	<1e-10	>1e5

V. CONCLUSIONS

Utilizing Low Temperature grown GaAs buffer layers in digital GaAs FET processes provides many advantages to

the circuit and system designer requiring radiation hardened ICs for space applications:

1. No redesign of masks or circuits are required. Only a wafer substitution is needed.
2. Digital GaAs processes can now provide Commercial-Off-The-Shelf (COTS) ICs with excellent radiation hardness for new commercial and military space systems. No increased costs are incurred for developing a specifically designed rad-hard integrated circuit processes.
3. Utilizing rad-hard GaAs processors and Application Specific Integrated Circuits (ASICs) in space applications can provide an order of magnitude increase in data rates over present radiation hardened silicon technologies.
4. By eliminating the need for error correction or redundancy to mitigate soft errors, GaAs-based space systems can obtain savings from weight, volume and power reductions.

VI. ACKNOWLEDGEMENTS

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