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Single Event Induced Voltage Transients within InP HBT Circuits

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Abstract

Voltage transients internal to an InP HBT integrated circuit are measured with picosecond resolution. Results show that the single event "shorts" the transistor terminals and the transient response can produce multiple errors at gigahertz frequencies.

Purpose

Space communication system architectures are requiring higher bandwidth digital technologies to accommodate present and future needs. Certain applications require technologies that are virtually immune to space radiation effects. Presently one of the highest speed integrated circuit technologies is the Indium-Phosphide based heterojunction bipolar technology. These circuits have been reported to operate at 40 GHz clock rates [1]. HRL Laboratories has a considerable effort to manufacturer both InP-based analog and digital circuits [2]. The technology is being proposed for space applications due to assumed immunity to total dose effects. Issues related to single event upset in InP based technologies have not been analyzed.

Due to the high speed operation of this technology, the effects of single event transients in the HBT circuit need to be understood to realize reliable operation. We wish to understand where the critical sensitivities can exist in the HBT circuit. If the cause of a single event error is dependent on the circuit, device or semiconductor material response, the knowledge of these mechanisms can provide insight in reengineering the system, circuit, device or material. The measurement of the single event induced voltage transients can also provide input in SPICE models for the circuit designer to test various circuit/system responses.

Measurements of the voltage transients internal to an integrated circuit have been difficult until recently. The measurements presented in this work utilize a laser-driven photoconductive sampling probe in a system located at the University of Michigan's Center for Ultrafast Optical Science [3]. The probe uses a high impedance photogate triggered by the laser. The 7-micron-wide probe tip can either contact metallization on the integrated circuit directly, or operate as a capacitive probe if there is an isolating passivation layer over the circuit traces (i.e., SiO_2, Si_3N_4, etc.). A beam of 100-fs-duration pulses from a Ti:sapphire laser oscillator is divided and used both to activate the photogate and to induce a transient from an HBT within the circuit. The photoconductive probe is positioned at various circuit nodes while the pump pulses are used to simulate the excitation of a single event. These laser pulses are delivered to the circuit via a 4-micron-diameter optical fiber placed above one of the circuit transistors. The technique has previously been used to examine SEE in a GaAs MESFET integrated circuit [4].

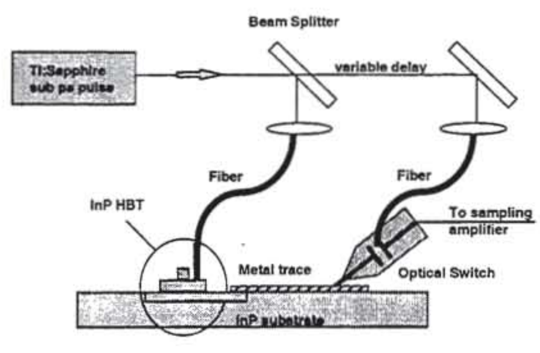

Figure 1 - Setup of the optically sampled photoconductive probe on a InP HBT circuit.

The experimental setup is shown in Figure 1. The beam splitter is used to create two pulse trains - the excitation and probe beams - that have virtually perfect synchronization between each other. The variable delay between the excitation and probe pulses is scanned in time to cover the duration of the voltage transient. At each discrete delay, the voltage level of the upset transient appears on the probe at the output of a hybrid, integrated, JFET source follower. It is then read on a lock-in amplifier and displayed on a computer. The time resolution of the measured signal is ~ 3 ps, and voltage amplitudes of less than 1 microvolt are acquired.

Results

An Emitter-Coupled Logic (ECL) circuit utilizing InP HBT NPN devices was tested using this optical pulse technique. The SPICE circuit schematic is shown in Figure 2 for the first sub-circuit within the IC. Previous experiments studying silicon ECL SEE suggested upset at two locations [6], at the differential pair and possibly at the current sources supplying each stage. We had observed upsets at the output of the InP circuit when devices at the differential pairs within this sub-circuit were irradiated. Upsets inside the circuit were observed using the minimal energy laser input pulse required to observe an upset on the output of the entire circuit. Our results saw two modes of upset at the differential pair, a) inducing an "off" NPN to turn on, and unexpectedly, b) an "on" NPN being turned off.

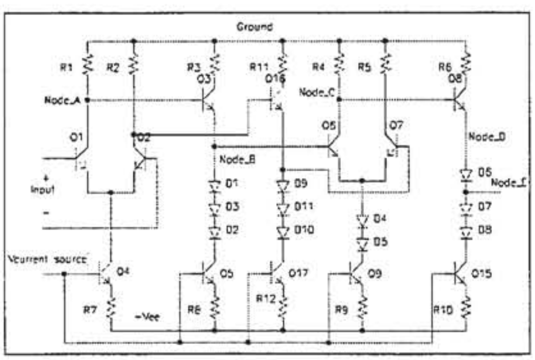

Figure 2 - Circuit Schematic of InP ECL test circuit. Figure 3 portrays the voltage transients from node A, node B and node C.

The transients induced by irradiating the "on" NPN HBT device Q1 in Figure 2 are shown in Figure 3. Node A is the collector of Q1. Notice that the collector voltage increases, due to a reduction in collector current. Q3 acts as an emitter follower to the differential stage, and the delay of the follower is approximately 5 ps. The transition of the second differential pair, node C, (Q6's collector) occurs 11 ps after node B. We can observe charge collection at node A, and this is mimicked at node B due to the emitter follower. However the high bandwidth of the circuit does not pass the slow components of the initial event to node C, because these components are within the circuit's noise margins.

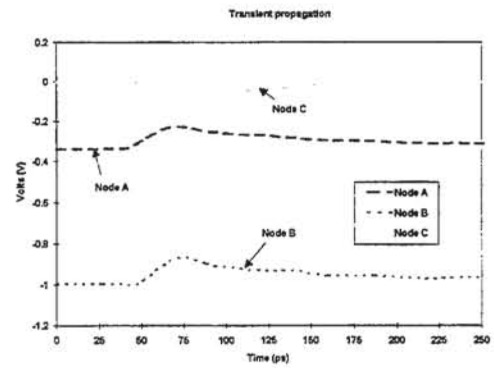

Figure 3 - Instantaneous voltages internal to the InP HBT ECL circuit shown in Figure 2.

The transient voltages around the initial perturbed device, Q1 are shown in Figure 4. The DC component of the measurements has been removed to show the "AC" component of the transients. As observed in the initial charge collection event, the transistor is effectively "shorted" out in the first 10 ps. The hole potential in the base is reduced, and thus the collector current reduces, increasing the collector potential.

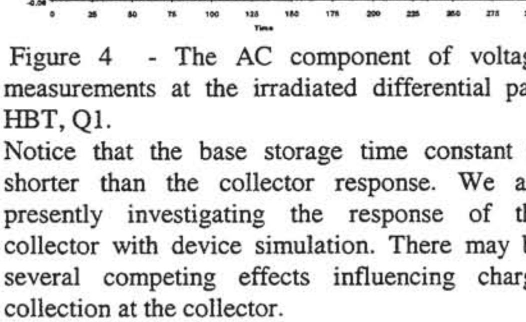

Figure 4 - The AC component of voltage measurements at the irradiated differential pair HBT, Q1.

Notice that the base storage time constant is shorter than the collector response. We are presently investigating the response of the collector with device simulation. There may be several competing effects influencing charge collection at the collector.

An additional setup was utilized where Ti:Sapphire lasers were operated at frequencies near each other to down convert the transient waveform. This technique allowed a single event transient to be observed while clocking the circuit at 10 GHz. Figure 5 shows a transient observed at node B. The charge collection event is induced at Q2 in Figure2.

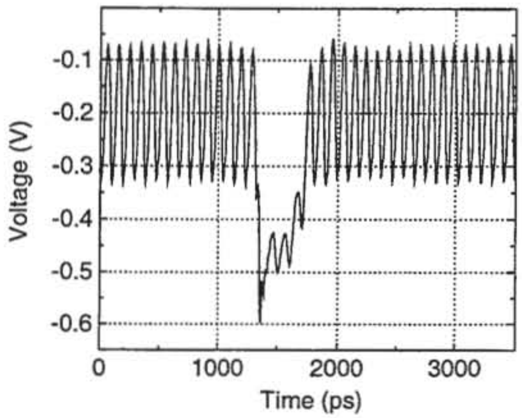

Figure 5 - Transient measured at node B while the circuit was operating at 10 GHz.

The results of Figure 5 are especially important in determining the effect of single events on high frequency circuits. If transients exceed more than one clock period, the ability to detect and correct multiple bit errors in a bit stream becomes difficult. This technique will become very useful for confirming how ultra high speed digital circuits will be vulnerable to single events.

The sensitivity was observed in only a few differential pairs. We expect that circuit design techniques are critical to single event sensitivity, and we will report on this further in the paper.

Effects due to single events on the current sources were not observed in this sub-circuit. Some effects were observed in a flip-flop circuit at the current source, but at much higher energy pulses. Inducing charge at current sources did not show actual bit flips on the output, but minor shifts in the output levels were observed. The analysis of the output level shifting effects will be discussed in the final paper.

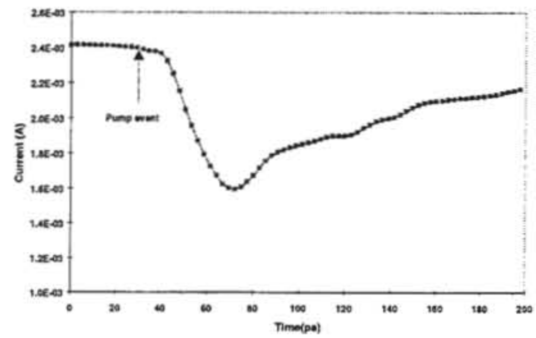

Figure 6 - Current of R1 in Figure 2 obtained by resistor node voltage measurements.

Amplitudes of resistor currents were obtained by measuring voltage transients at each end of a resistor. When Q1 is irradiated, the HBT turns "off" as shown in the load resistor current reduction in Figure 6. The dc current of 2.4 mA is reduced down to 1.6 mA. The ground side of the resistor was observed to vary as much as 7mV from the equilibrium ground potential. From the data of Figure 6 we can estimate (by integrating the AC component) how much charge passes through the resistor. In this case approximately 12fC is supplied by the ground plane. Possibly a larger load resistor in this circuit would reduce the vulnerability. These measurements should provide insight in which circuit parameters would provide the best tolerance to single events. We intend to include SPICE simulations to compare to these measurements. Our two-dimensional device/circuit simulations are to be presented in a separate work analyzing effects within the device structure.

The structure of the HBT incorporates InGaAs, InAlAs and InP. The wavelength of the laser for these measurements was 810 nm. The incident light was mainly absorbed in the InGaAs regions of the base and collector and issues related to absorption due to wavelength will be presented and discussed in the full paper.

Advances to the State-of-the-Art

In summary we have presented the first internal measurements of voltage transients of an InP circuit. The data from these experiments will provide several key needs to understand SEU in high speed HBT devices. The key needs are:

1) to observe where the circuits are sensitive,
2) to determine if the response is dominated by the device and/or circuit,
3) to examine how the heterojunctions and/or substrate react to charge collection,
4) to confirm that 2-D charge transport and SPICE simulations are realistic,
5) to assist in developing a SPICE model to model the collection event.

Additionally we have shown that the use of the photoconductive probe provides a highly accurate and non-destructive technique to investigate internal nodes without limiting the bandwidth of the circuit. This technique in some cases does not require packaged die. Also the technique is capable of measuring transients in active circuits operating in excess of 150 GHz.

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