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Mitigating Circulating Common-Mode Currents Between Parallel Soft-Switched Drive Systems

Robert M. Cuzner, *Senior Member, IEEE*, Daniel J. Nowak, Ashish Bendre, *Member, IEEE*, Giovanna Oriti, *Senior Member, IEEE*, and Alexander L. Julian, *Member, IEEE*

***Abstract*—A mathematical model that is developed for a generalized drive system, including common-mode passive and active elements, is used to explore the issues of paralleling soft-switched resonant dc-link drive systems. Differences between the modulation pattern for each drive system cause common voltage disturbances, which lead to significant circulating currents between the drive systems. Control methods for actively compensating for common-mode circulating currents or reducing the common-mode voltage disturbances are investigated. Practical modifications to the drive system controls are implemented to reduce the circulating currents between paralleled systems.**

***Index Terms*—Component, drive system modeling, electromagnetic interference (EMI), paralleling power converters, soft-switched power converters.**

I. Introduction

DRIVE SYSTEMS with a limited output power capability can be paralleled to feed higher power loads. Such a system requires differential-mode and common-mode impedance or galvanic isolation between the drives to limit circulating currents that occur between them—without additional control means on output inverters. The paralleled inverters of each drive system create both differential- and common-mode voltages, which can give rise to significant differential- and common-mode circulating currents between the drive systems [1]–[5]. If impedance or isolation between drive systems is not sufficient to limit these circulating currents, it is necessary to actively control both differential-mode and common-mode currents in each cabinet. Such is the case when drive systems are paralleled without a transformer, separated motor windings, or large interphase reactors. In such a case, a high-bandwidth differential-mode current regulator is required to share the load on the output phases of the inverter [3]–[5], [8], [9]. In addition, a common-mode circulating current also occurs between drive systems due to the common-mode voltages produced by each [4]. If no common-mode impedance exists between the systems, it is necessary to actively control common-mode current. Various control techniques have been proposed to control this common-mode circulating current [6], [7], [10]–[13]. This paper describes an ac–dc–ac drive system with an active rectifier and an inverter based on the actively clamped resonant dc-link (ACRDCL) converter. The ACRDCL converter was selected because of its spread spectrum output, with the design goal of achieving very low individual harmonic distortion with minimal output filter sizes and low input/output conducted electromagnetic interference (EMI) in the range of 100 kHz and above. The ACRDCL converters were paralleled to achieve increased scalable power in the drive system. As with any converter topology, paralleling requires the control mitigation of common-mode circulating currents between converters. Because the ACRDCL converter has constraints on when switch states can be changed, the methods by which this circulating current are mitigated are different than those used for hard-switched converters.

In this paper, a mathematical model is developed for a generalized system including common-mode passive and active elements. This model is suitable for evaluation of multiple controller implementations in simulation, without significant simulation execution times. The model is applied to the solution of common-mode circulating problems in two paralleled ACRDCL drive systems. An appropriate control solution is determined that minimizes the common-mode circulating current without compromising differential-mode total harmonic distortion (THD). This method is implemented and verified on a hardware platform with demanding packaging density constraints.

II. Drive System Common-Mode Current

Fig. 1 shows the schematic for a single drive system. A drive system may contain all of the components shown. This is particularly the case for military applications where low input/output harmonic distortion and specific EMI performance are required [14], [15]. The main system components are: 1) input EMI filter; 2) input harmonic filter; 3) active rectifier and controls; 4) output inverter and controls; 5) output harmonic filter; and 6) output EMI filter. The purpose of the input and output EMI filters is to reduce the common-mode conducted emissions on the incoming and outgoing lines of the drive system. The purpose of the input and output harmonic filters is to reduce differential-mode input (line) current and output (line-to-line) voltage THD that the distribution system or motor, respectively, will see due to the switching of the active rectifier and the inverter.

The active rectifier and its control regulate the input power factor (usually unity) and sinusoidal input currents. The output

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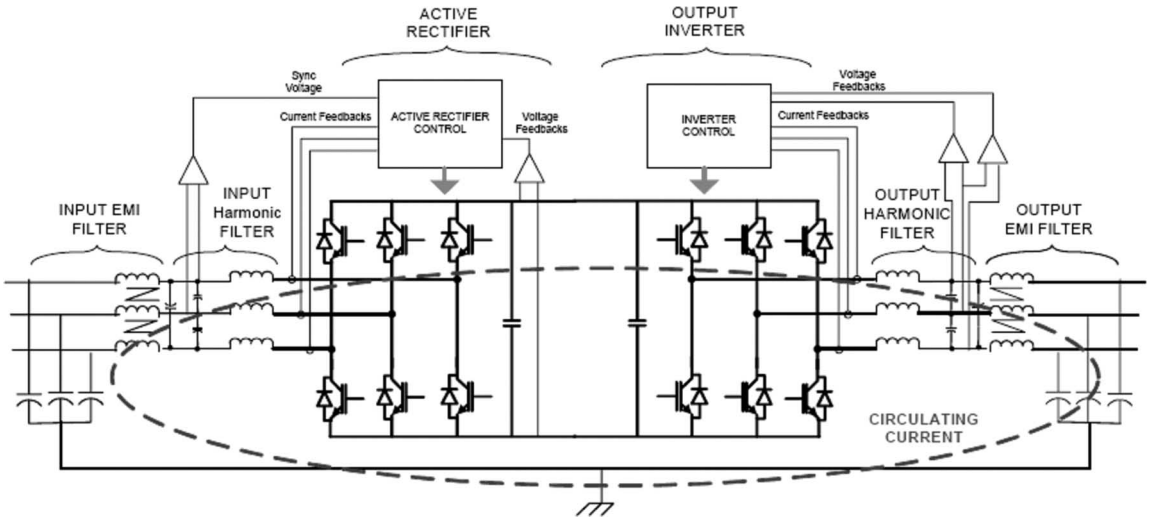

Fig. 1. Drive system schematic.

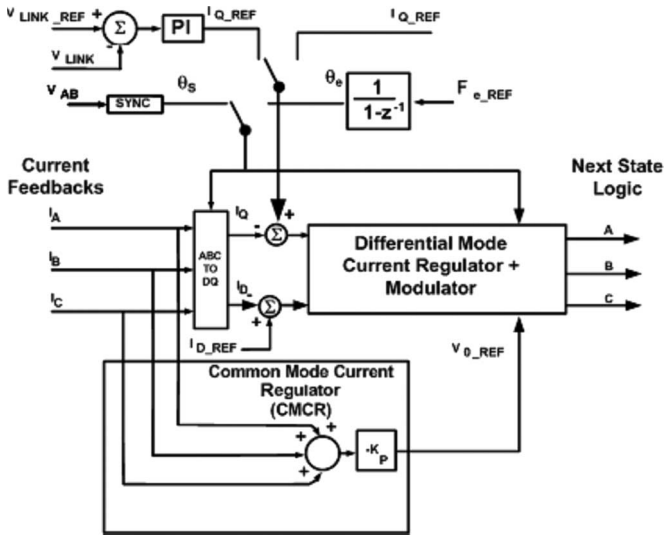

Fig. 2. Inverter or active rectifier control with common-mode current regulator added.

inverter and its control regulate the voltages and frequency applied to the motor at desired levels, based on motor speed requirements, and deliver sinusoidal current to the motor.

The active rectifier and the inverter also produce common-mode voltage, which is the result of the periodic level switching of all three input or output lines with respect to some common potential, i.e., chassis ground [16]. As a result of this switching, a common-mode current can find its way through any path to ground. The flow of this common-mode current through parasitic capacitance outside of the drive system (i.e., through the motor bearings to ground or through power cables to ground) is the cause of bearing currents in the attached motor and the source of conducted EMI. The EMI filter on both input and output of the drive system in Fig. 1 provides a path for these currents to flow inside of the drive system.

Fig. 2 shows a control block diagram for either the active rectifier or the inverter that is required for the control of both differential- and common-mode currents. Fig. 3 shows the internals of the "differential-mode current regulator + modulator" block. In the case of the active rectifier, the "differential-mode current regulator + modulation" D- and Q-axis proportional plus integral (PI) current regulators generate voltage references to the modulator necessary to control input real and reactive currents for the control of dc link voltage and input power factor, respectively. In the case of the inverter, the D- and Q-axis PI regulators generate voltage references based on the needs of some outer loop control (voltage, speed, or torque) to control real and reactive currents that are applied to the load. A common-mode current regulator (CMCR) may be added to either the active rectifier or the inverter to reduce the input-to-output common-mode circulating current shown in Fig. 1, which is due to input/output filter oscillation currents. This technique has previously been applied to control differential-mode disturbances due to interactions of the input or output harmonic filter in voltage-mode modulated converters with high bandwidth capability [17], [18]. The differential-mode THD will be compromised for the converter that incorporates the CMCR because the CMCR will force the selection of nonadjacent switch states, whereas the D- and Q-axis current regulators tend to force the selection of adjacent states if one of the resultant three phase voltage references to the modulator is allowed to be dependent on the other two phase references. Adjacent switch states maximize the voltage utilization yielding low differential-mode THD.

III. Actively Clamped Resonant DC Converter

The three-phase ACRDCL power converter (inverter or active rectifier) is represented in Fig. 4. The components that are highlighted in gray are those additional auxiliary components that are required to achieve soft switching. Operation of the ACRDCL inverter, as well as its potential benefits, is well documented in the literature [18]–[22]. A significant difference between the ACRDCL power converter and a hard-switched power converter is that the converter must wait for a zero-voltage condition to occur across its resonant capacitor voltage V_{RES} (see Fig. 5) before the power semiconductors can be commutated.

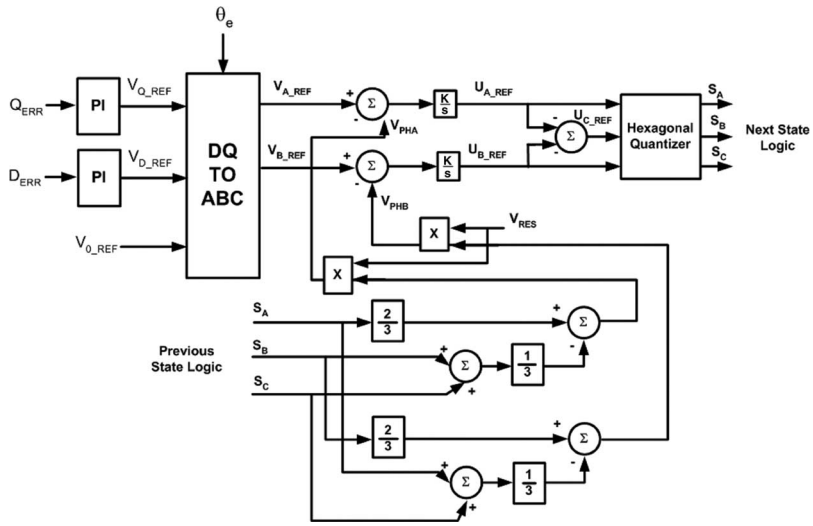

Fig. 3. Differential mode current regulator + sigma delta modulator.

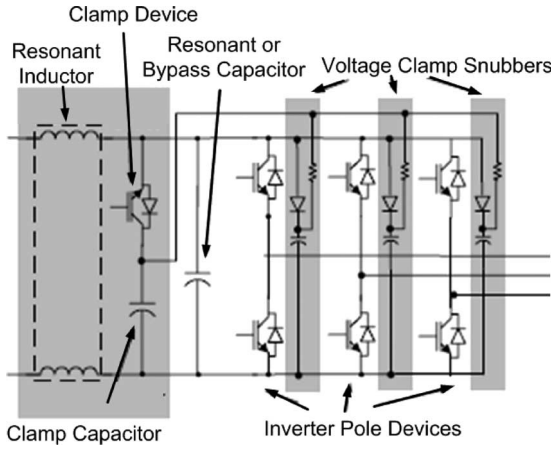

Fig. 4. ACRDCL inverter/active rectifier module.

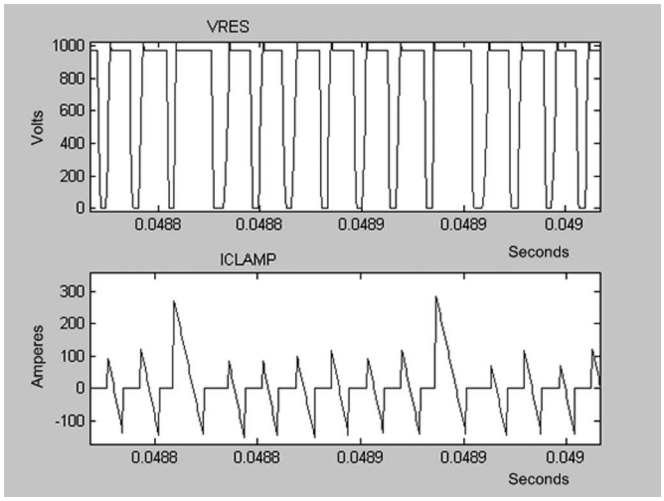

Fig. 5. Simulated resonant link voltage (V_{RES}) and clamp current (ICLAMP).

The resonating/clamped voltage (V_{RES}; Fig. 5) is created by the following sequence.

1) Resonant capacitor voltage is shorted for a short period of time before each switch commutation, which builds energy up in the resonant inductor.
2) Energy is transferred between resonant capacitor and inductor when the switch state is selected and the voltage resonates up to the level of a precharged clamp capacitor.
3) Voltage is clamped through the clamp diode to the clamp capacitor voltage and clamp current flows ("ICLAMP" in Fig. 5), and clamp insulated gate bipolar transistor (IGBT) is turned on.
4) When the clamp IGBT current reaches a predetermined level after reversing direction, the clamp IGBT is turned off, and the resonant capacitor voltage rings back down to zero.

As shown in Fig. 5, the times that the converter is in a clamped or shorted mode considerably vary. This behavior is dependent on the amplitude of current to the load that is being sourced from or absorbed by the ACRDCL circuit.

Various methods have been explored in the literature to control the switch states of the ACRDCL converter [23]–[25]. The simplest is the delta modulation [23], which, at each switching opportunity, selects either a high or a low state for a given phase half-bridge—based on the error between current reference and actual phase current. This approach has the drawback of the resultant THD being very dependent on filter or load. Fig. 6 shows delta modulation that is implemented in conjunction with an active rectifier control.

The most optimal differential-mode THD can be achieved with vector sigma delta modulation (VSDM) [24], [25]. VSDM generates the next switch states based on the integrated error between phase voltage references and differential-mode components of the inverter pole voltage feedback, synthesized from previous switch states and given by the expressions

$$V_{\mathrm{PHA}} = \frac{2}{3} V_{\mathrm{RES}} * \left[Sa - \left(\frac{Sb + Sc}{2} \right) \right] \tag{1}$$

$$V_{\mathrm{PHB}} = \frac{2}{3} V_{\mathrm{RES}} * \left[Sb - \left(\frac{Sa + Sc}{2} \right) \right]. \tag{2}$$

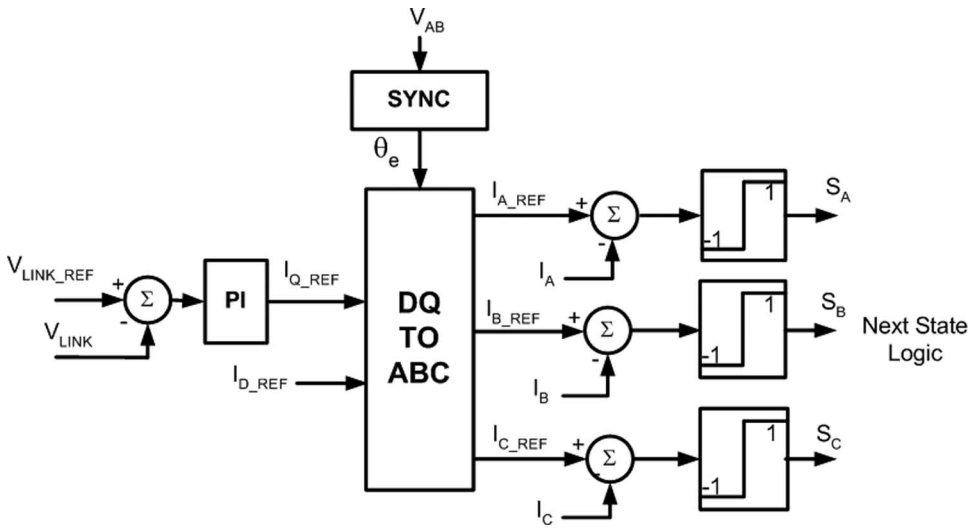

Fig. 6. Active rectifier control + delta modulator.

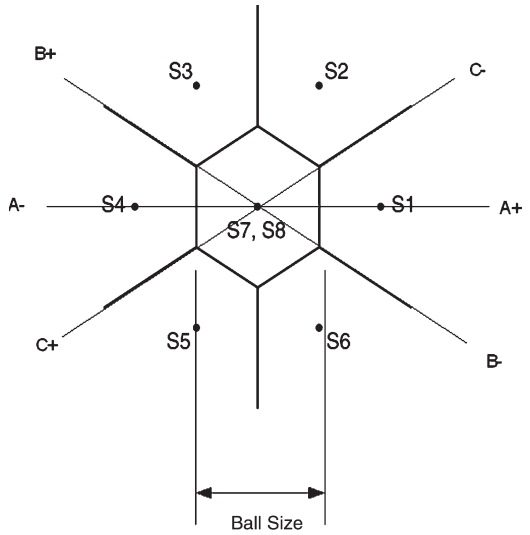

Fig. 7. Hexagonal quantizer.

Equations (1) and (2) are derived from the inverter pole voltages with the constraint that

$$V_{\mathrm{PHA}} + V_{\mathrm{PHB}} + V_{\mathrm{PHC}} = 0. \tag{3}$$

The VSDM imposes this constraint by mapping the inverter states into the 2-D vector space shown in Fig. 7. S1–S8 represent the inverter switch states. The size of the hexagon around each state is determined by the hexagon around the center or "zero" state (S7 or S8). This hexagon is referred to as "ball size" and is a key parameter for the VSDM control. If the integrated errors for all three phases are within the region of this inner hexagon, then the zero state is chosen.

Although with VSDM the selection of switch states tends to be random, if the ball size is set somewhere between 0.5 and 1.0 (on a per-unit basis), then the inverter voltage synthesis tends to follow an adjacent state switching pattern. When the output voltage that is synthesized is high, adjacent state switching yields the best utilization of the dc-bus voltage to produce a low THD differential-mode voltage. On the other hand, an optimal

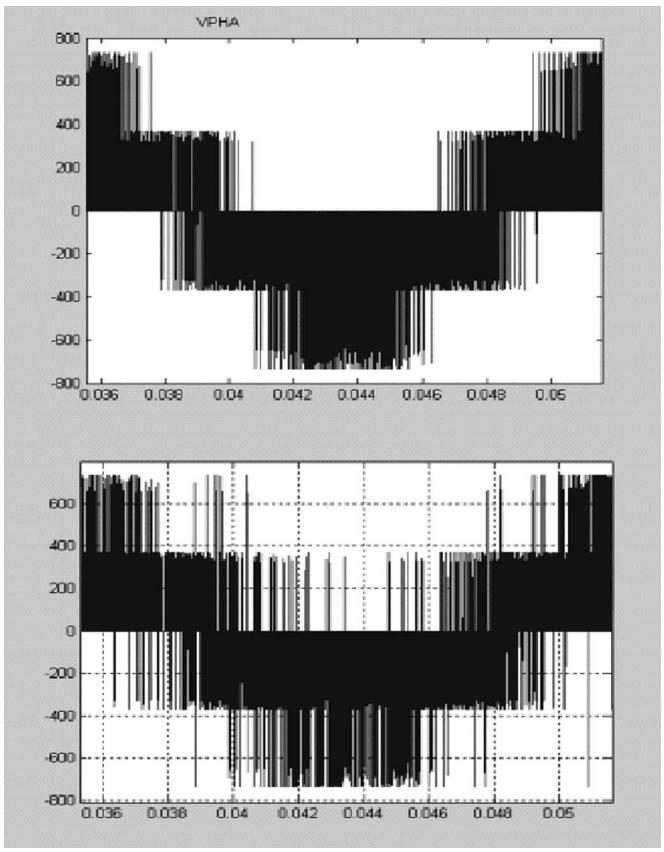

Fig. 8. Inverter phase voltage with optimal ball size (top) and zero ball size (bottom).

ball size maximizes the selection of zero states, which leads to high common-mode voltage, and resultant high common-mode circulating currents. If the ball size is reduced to well below 0.5, the differential-mode THD suffers, but the common-mode voltage is reduced. Fig. 8 shows the line-to-neutral voltage that is produced by the output inverter with an optimal ball size (around 0.8) and with a small ball size ($\ll 0.5$). The voltage that is produced with the small ball size shows a number of nonadjacent switch patterns. With the optimal ball size, the

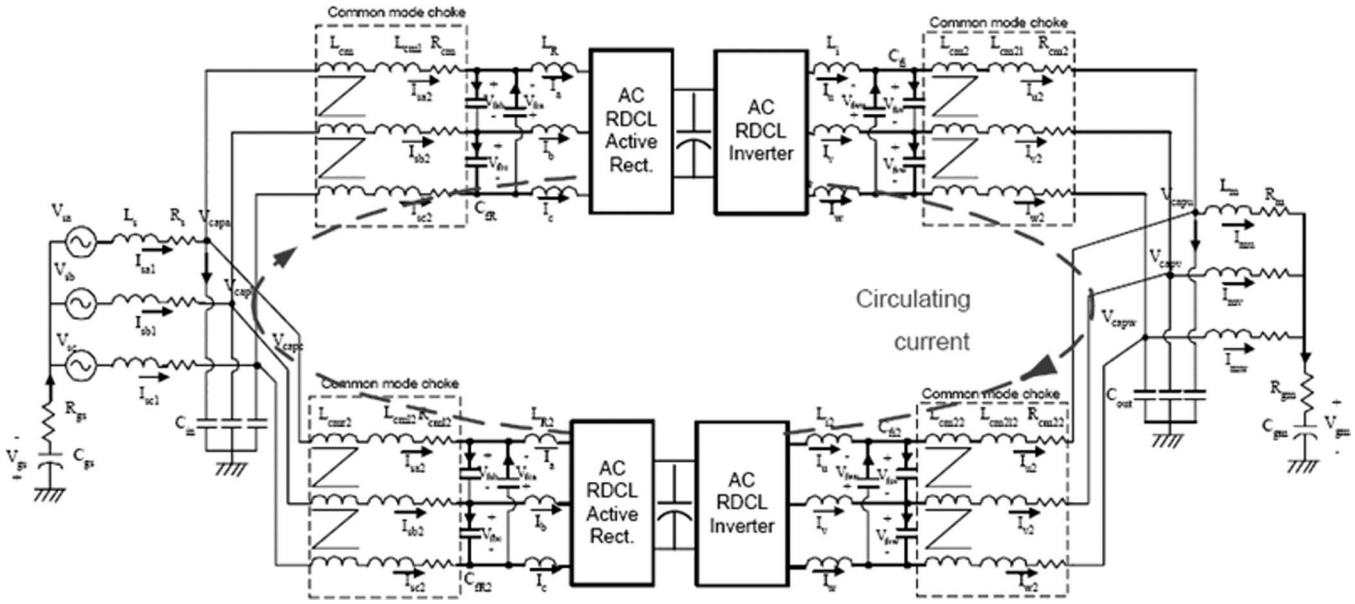

Fig. 9. Parallel ACRDCL drive system.

behavior of the VSDM is closely analogous to the space vector modulation used with hard-switched inverters.

IV. Mathematical Model of Paralleled ACRDCL

A common-mode circulating current occurs between drive systems when they are paralleled, as shown in Fig. 9. This is the case when there is no synchronization between the selection of switch states in the paralleled inverters, and a resulting difference occurs between the common-mode voltages that are generated in each inverter [10].

To understand the causes and the effects, as well as mitigate the common-mode currents between cabinets, a mathematical model was developed for the paralleled drive systems of Fig. 7. This model can be applied to both hard-switched and soft-switched drive systems. Each cabinet includes a rectifier, a dc link, and an inverter. The model includes:

1) source and load differential- and common-mode circuit paths;
2) all input/output differential- and common-mode filters;
3) switching models of the active rectifier and the inverter that include both common mode and differential mode (switch states and controls).

The equations for each drive system are identical. A single drive system model is general enough that full common-mode and differential-mode performances are included and can be adapted to other applications simply by removing components (i.e., the output harmonic and EMI filter components for typical industrial drive systems).

The inputs V_a, V_b, V_c, V_u, V_v, and V_w are the pole voltages that are dependent on their respective pole switch states. The 13 differential equations can be written for the central model using Kirchhoff's voltage law and current law. These equations are written in the matrix format, i.e.,

$$\boldsymbol{G} \cdot \boldsymbol{u} + \boldsymbol{M} \cdot \boldsymbol{x} + \boldsymbol{F} \cdot \dot{\boldsymbol{x}} = 0 \tag{4}$$

from which the following matrices $\boldsymbol{A}$ and $\boldsymbol{B}$ can be derived:

$$\boldsymbol{A} = -\boldsymbol{F}^{-1} \cdot \boldsymbol{M}, \quad \boldsymbol{B} = -\boldsymbol{F}^{-1} \cdot \boldsymbol{G}. \tag{5}$$

For the central model, the matrices $\boldsymbol{G}$, $\boldsymbol{M}$, and $\boldsymbol{F}$ are shown on the next page.

The single drive system model includes the central part of the circuit from the model input voltages $V_{\mathrm{capa}}, V_{\mathrm{capb}}$, and V_{capc} to the model input voltages $V_{\mathrm{capu}}, V_{\mathrm{capv}}$, and V_{capw}. Two additional state-space models, which are not derived in this paper, can represent the rest of the system. The three-phase supply, its *RL* source impedance, and the capacitor voltages $V_{\mathrm{capa}}, V_{\mathrm{capb}}$, and V_{capc} can be represented in one state space model. The *RL* load, the RC impedance of the load to ground, and the capacitor voltages $V_{\mathrm{capu}}, V_{\mathrm{capv}}$, and V_{capw} can be represented in another state space model. The outputs of these two smaller models are inputs to the central part of the circuit.

Thirteen state space variables and 12 inputs describe the central part of the circuit. A single drive system is represented by a state-space model described by the following:

$$\dot{\boldsymbol{x}} = \boldsymbol{A} \cdot \boldsymbol{x} + \boldsymbol{B} \cdot \boldsymbol{u}$$

where the state variables and the state-space model inputs are as shown on the next page, in which

$$\begin{aligned} \mathrm{cf1} &= -(\mathrm{Lcm} + \mathrm{Lcml} + \mathrm{Lcm2}); \ \mathrm{cf2} = -(\mathrm{Lcm} + \mathrm{Lcm2}); \\ \mathrm{cf3} &= -(\mathrm{Lcm} + \mathrm{Lcm2l} + \mathrm{Lcm2} + \mathrm{LR} + \mathrm{Li}); \\ \mathrm{cf4} &= -(\mathrm{Lcm} + \mathrm{Lcml} + \mathrm{LR} + \mathrm{Li} + \mathrm{Lcm2} + \mathrm{Lcm2l}). \end{aligned}$$

V. Simulation Study and Implementation Issues

A simulation was developed for the mathematical model described in Section IV for two parallel drive systems. The simulation tool used was Simulink. The simulation model also included detailed implementations of ACRDCL active rectifiers and inverters.

The drive system requires very low output voltage THD. For this reason, the output inverter was controlled using VSDM

$$\boldsymbol{G} = \begin{bmatrix}
1 & 0 & 0 & -1 & 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 \\
0 & 1 & 0 & 0 & -1 & 0 & 0 & 1 & 0 & 0 & -1 & 0 \\
0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 1 & 0 & 0 & -1 \\
0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}$$

$$\boldsymbol{M} = \begin{bmatrix}
-R_{cml} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -R_{cm2} & 0 \\
0 & -R_{cml} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -R_{cm2} \\
-R_{cm2} & -R_{cm2} & -R_{cml}-R_{cm2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{cm2} & R_{cm2} \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -R_{cm2} & R_{cm2} \\
R_{cm2} & R_{cm2} & R_{cm2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -R_{cm2} & 2R_{cm2} \\
\frac{1}{3C_{fR}} & \frac{-1}{3C_{fR}} & 0 & \frac{-1}{3C_{fR}} & \frac{1}{3C_{fR}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{3C_{fR}} & \frac{2}{3C_{fR}} & 0 & \frac{-1}{3C_{fR}} & \frac{-2}{3C_{fR}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{3C_{fi}} & \frac{-1}{3C_{fi}} & 0 & 0 & \frac{-1}{3C_{fi}} & \frac{1}{3C_{fi}} \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{3C_{fi}} & \frac{2}{3C_{fi}} & 0 & 0 & \frac{-1}{3C_{fi}} & \frac{-2}{3C_{fi}}
\end{bmatrix}$$

$$\boldsymbol{F} = \begin{bmatrix}
cf1 & cf2 & cf2 & -L_R & 0 & 0 & 0 & -L_i & 0 & 0 & 0 & -L_{cm2l} & 0 \\
cf2 & cf1 & cf2 & 0 & -L_R & 0 & 0 & 0 & -L_i & 0 & 0 & 0 & -L_{cm2l} \\
cf3 & cf3 & cf4 & L_R & L_R & 0 & 0 & L_i & L_i & 0 & 0 & L_{cm2l} & L_{cm2l} \\
0 & 0 & 0 & -L_R & L_R & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
L_R & L_R & L_R & -L_R & -2L_R & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -L_i & L_i & 0 & 0 & 0 & 0 \\
L_i & L_i & L_i & 0 & 0 & 0 & 0 & -L_i & -2L_i & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -L_{cm2l} & L_{cm2l} \\
L_{cm2l} & L_{cm2l} & L_{cm2l} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -L_{cm2l} & 2L_{cm2l} \\
0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0
\end{bmatrix}$$

$$x^T = [\, i_{sa2} \quad i_{sb2} \quad i_{sc2} \quad i_a \quad i_b \quad V_{fab} \quad V_{fbc} \quad i_u \quad i_v \quad V_{fuv} \quad V_{fvw} \quad i_{u2} \quad i_{v2} \,]$$

$$u^T = [\, V_{\mathrm{cap}a} \quad V_{\mathrm{cap}b} \quad V_{\mathrm{cap}c} \quad V_a \quad V_b \quad V_c \quad V_u \quad V_v \quad V_w \quad V_{\mathrm{cap}u} \quad V_{\mathrm{cap}v} \quad V_{\mathrm{cap}w} \,]$$

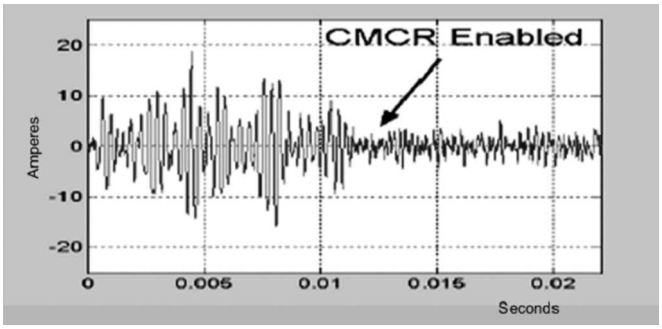

Fig. 10. Ideally simulated drive system common-mode current, 430 V, 58 Hz, ball size $= 0.8$.

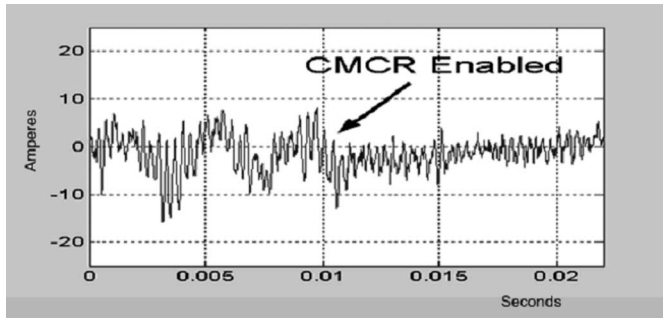

Fig. 11. Simulated drive system common-mode current, with control nonidealities, 430 V, 58 Hz, ball size $= 0.8$.

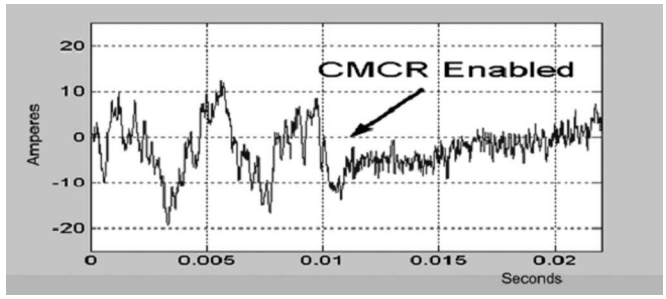

Fig. 12. Simulated common-mode circulating current between paralleled drive systems, 430 V, 58 Hz, ball size $= 0.8$.

without a CMCR enabled. Synchronous frame current regulators [26], in combination with VSDM, force sharing of differential-mode load current between the two inverters and simultaneously produce low THD and good dynamic load current sharing [18]. The differential-mode current regulators are digitally implemented in the simulation at a sampling frequency close to the average resonant link frequency (67 kHz). This matches the actual hardware implementation.

The drive system requires input current THD as per [14]. From the standpoint of the active rectifier differential mode, this requirement is not as demanding as that of the output inverters. Therefore, the CMCR can be implemented on the active rectifiers to help control the common-mode circulating current, and the input current THD specification can still be met. Delta modulation differential-mode current control combined with the CMCR meets the input differential-mode current THD requirement and controls the common-mode circulating current. It should be noted that in addition to the CMCR, independent delta modulation on each input phase current is similar to phase decoupled hysteresis current mode PWM, which inherently limits the common-mode circulating current [9].

The drive system operates from a fixed 460-V 60-Hz three-phase bus. The inverter will provide variable voltage and variable frequency to its loads. The focus of the simulation study is to ensure that the two parallel drive systems share current from the source and to the load. The issue to be explored is whether delta modulation with and without the CMCR is effective in controlling circulating current between paralleled drive systems. This common-mode circulating current, if not controlled, will have the effect of saturating the EMI filter inductor and could cause overcurrents to occur within either drive system.

The extremes of operation are explored assuming a pump motor load on the paralleled drive systems: 1) maximum output voltage/frequency, maximum output current; and 2) minimum output voltage/frequency, minimum output current. Fig. 10 shows the common-mode current in a single cabinet over one output voltage electrical cycle before and after the CMCR is enabled in the active rectifier only (it is necessary to only implement the CMCR either in the active rectifier or the inverter—not both). There are no delays in IGBT gating signals or differences whatsoever between paralleled active rectifiers and paralleled inverters. For this scenario, the common-mode current is only due to interactions between the input and output EMI filter, and the dominant frequency is the resonant frequency of the combined input/output EMI filters ($\sim$2 kHz). There is no circulating current between the paralleled drive systems.

In reality, the ACRDCL active rectifiers and inverters each select instantaneous switch states based on the occurrence of a random event (the resonant voltage zero-voltage conditions of Fig. 5). The frequency of and delays in these events are dependent on instantaneous currents that flow into or out of each ACRDCL power module. The differences in time between the selection of zero states by the paralleled inverters, for example, will cause the common-mode current to flow between paralleled drive systems. These differences occur because of the differences in control hardware latencies and feedback accuracy. Simulations verify (to be shown later) that the key driver of the common-mode current between drive systems is the difference between the common-mode voltages in each inverter.

A realistic approach to simulating the common-mode voltage differences in paralleled system is to introduce the following nonidealities: 1) differences in timing latencies between the executions of output inverter digital differential-mode current regulators; 2) current feedback gain and offset differences; and 3) alternating zero states (S7 and S8) that are asynchronous in each ACRDCL converter.

Considering operating condition (1) (inverter output $=$ 430 V, 58 Hz), Fig. 11 shows the common-mode current in one drive system with nonidealities included, and Fig. 12 shows the common-mode circulating current between drive systems. The current is shown before and after the CMCR is activated. The periodic excursions of circulating current between drive systems are due to the control nonidealities.

Fig. 13 shows the common-mode current in one drive system for operating condition (2) (inverter output $=$ 172 V, 22 Hz).

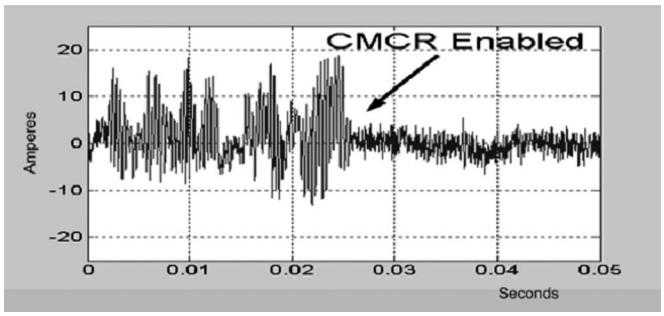

Fig. 13. Simulated drive system common-mode current, with control nonidealities, 172 V, 22 Hz, ball size = 0.8.

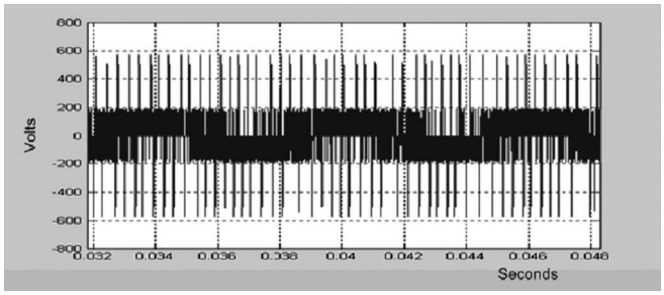

Fig. 14. Common-mode voltage differences between paralleled drives, 430 V, 58 Hz, ball size = 0.8. 200 V/Div.

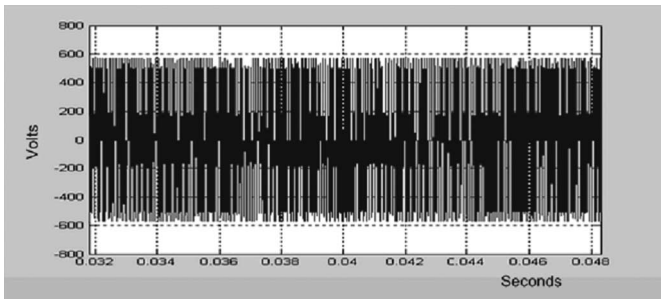

Fig. 15. Common-mode voltage differences between paralleled drives, 172 V, 22 Hz, ball size = 0.8. 200 V/Div.

Again, the current is shown before and after the CMCR is activated. Before the CMCR is activated, the common-mode currents between drive systems are higher for low voltage condition (2) versus higher voltage condition (1) (see Fig. 12).

When the zero-state vectors are selected, the common-mode voltages that are generated by the output inverters are at their maximum. The difference between common-mode voltages in the two paralleled inverters is a disturbance that drives the common-mode circulating current between systems. As explained in Section III, the ball size governs the selection of zero states. For the simulations of Figs. 11–13, the ball size is set to 0.8. Figs. 14 and 15 show the simulated common voltage differences for operating conditions (1) and (2), respectively. The incidence of maximum common voltage is significantly higher for condition (2). This is because more zero voltages are selected to synthesize the lower voltage of 172 V than for the 430-V condition.

Although the CMCR compensates for common-mode circulating currents, the ball size in the output inverter is an additional handle that can be used in the control design that

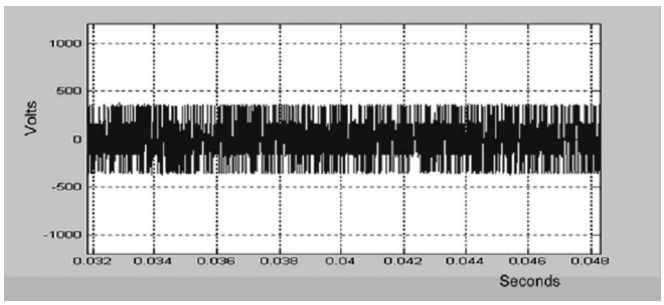

Fig. 16. Inverter common-mode voltage differences, 172 V, 22 Hz, ball size = 0.500 V/Div.

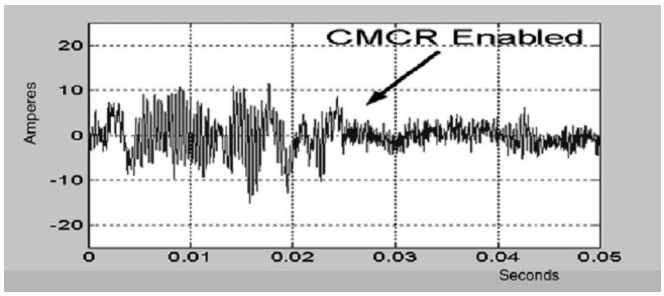

Fig. 17. Simulated drive system common-mode current, with control nonidealities, 172 V, 22 Hz, ball size = 0.

limits the disturbance that causes these currents. Fig. 16 shows the common-mode voltage difference for condition (2) with the ball size set to 0. In this case, the zero-state selection is not allowed, and the common-mode voltage difference is reduced. For ball size = 0, the common-mode current is shown in Fig. 17. As shown in both Figs. 13 and 17, reducing the common-mode voltage disturbance reduced the occurrence of common-mode current peaks before the activation of the CMCR.

It should be noted that observations with regard to the CMCR apply both to hard-switched and soft-switched inverters. There really is no difference between the behavior of both inverters except for the fact that hard-switch inverter modulation techniques are deterministic and can be constrained to follow a particular pattern, whereas the ACRDCL converter selects switch states through random or stochastic means, which trend toward the switching patterns that were observed in simulation and hardware.

VI. Hardware Validation

Parallel ACRDCL drive systems were implemented in hardware. Each drive system rating was limited to 150 kW. The drive systems were paralleled and tested, feeding a load at 300-kW 0.8 power factor. Drive system power IGBT devices were water cooled to maximize switching frequency. The ACRDCL circuit with required passive components and filtering was designed to maximize power density while meeting the specified input current and output voltage THD requirement and input/output conducted EMI requirements.

Delta modulation control of Fig. 6 was implemented on the active rectifiers and current-regulated VSDM (see Fig. 3) with ball size = 0.8 on the inverters. As the voltage/frequency was

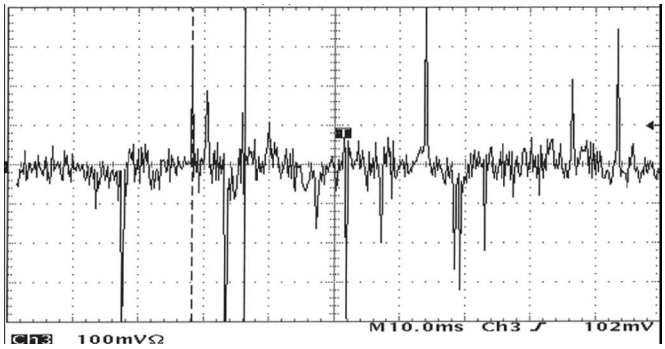

Fig. 18. Measured common-mode circulating current with delta modulation. Operating condition 162 V, 22 Hz; no CMCR; ball size = 0.8, 20 Å/Div, 10 ms/Div.

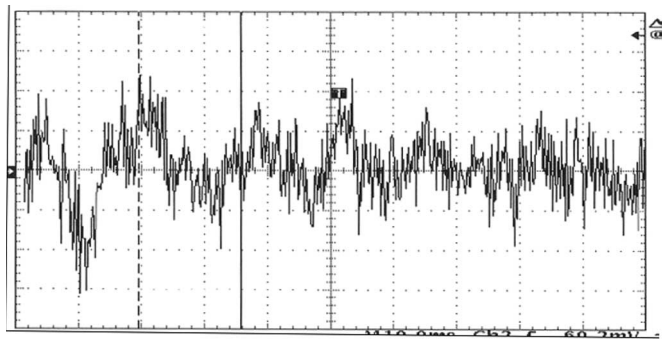

Fig. 19. Measured common-mode circulating current with delta modulation; operating condition 440 V, 54 Hz; no CMCR; ball size = 0.8, 4 Å/Div, 10 ms/Div.

ramped up, it was noted that the common-mode currents in each drive system were excessive at low output voltage but well controlled as the output voltage increased above 380 V. At 162 V and 22 Hz, the measured circulating common-mode current is shown in Fig. 18. The common-mode current is not well controlled, as shown by the current spikes occurring when the common-mode current reaches a level that saturates the EMI filter inductors. At 440 V and 58 Hz, the measured common-mode current is shown in Fig. 19. The current peaks are low enough that the EMI filter inductors do not saturate. This behavior was expected based on the simulation study of Section V.

An attempt was made to implement the CMCR in addition to delta modulation on the active rectifier (the control of Fig. 2). Because of demanding packaging density constraints, only three current sensors could be used. As a result, the common-mode current feedback had to be synthesized by the sum of the three line currents shown in Fig. 2. Implementing the CMCR was really not effective in limiting the current spikes of Fig. 18 and the high circulating current between drives, most probably due to accuracy in the three feedback signals and the cumulative error in the synthesized common-mode current feedback.

As an alternative approach, the per-unit ball size was reduced from 0.8 to 0.1, through a software change in the control, to limit the common-mode voltage disturbance, as described by Figs. 15 and 16. Fig. 20 shows a histogram of the common-mode current peaks encountered for the 162-V, 22-Hz operating condition with the ball size set to 0.8. The histogram records the

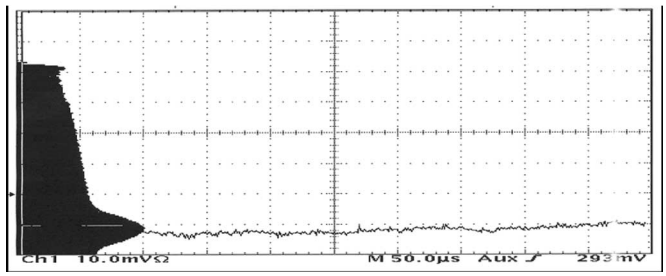

Fig. 20. Histogram of common-mode current peaks; operating condition 162 V, 22 Hz; ball size = 0.8, 40 Å/Div.

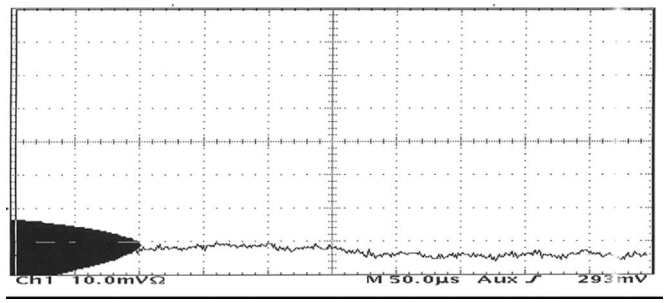

Fig. 21. Histogram of common-mode current peaks; operating condition 162 V, 20 Hz; ball size = 0.1, 20 Å/Div.

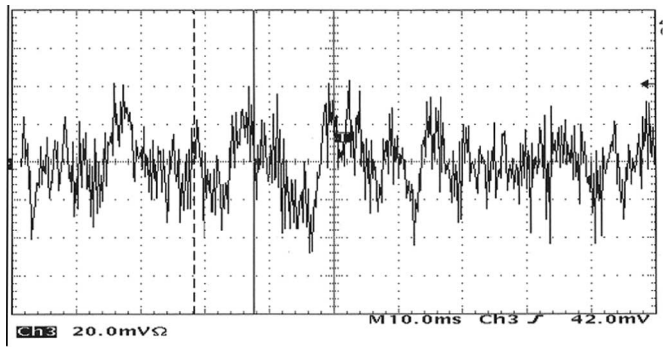

Fig. 22. Measured common-mode circulating current; operating condition 162 V, 22 Hz; no CMCR; ball size = 0.1, 4 Å/Div, 10 ms/Div.

magnitude and the frequency of occurrence of current peaks. Current peaks of over 100 Å occur.

Fig. 21 shows a histogram after the ball size was set to 0.1 for the 162-V, 22-Hz condition. The common-mode current peaks are reduced to well below the point where the EMI filter saturates (less than 20 Å). Fig. 22 shows the measured common-mode current for the low voltage condition with ball size = 0.1. Comparing this with Fig. 19, there are no incidences of EMI filter inductor saturation.

Tests were performed on the drive system to determine the effect of ball size on output voltage THD. For output voltages above 400 V, the THD increased with ball size = 0.1. However, for voltages above 380 V, the common-mode current peaks were well controlled when the ball size was increased to 0.8. The THD performance objectives were met by toggling between 0.8 and 0.1, as output voltage reduced below 380 V.

VII. Conclusion

In this paper, a mathematical model for paralleled drive systems is developed to include differential- and common-mode behavior. The model has been verified through computer simulation as a practical tool for developing solutions for common-mode current control and mitigation in paralleled drive systems. This model is also suitable for predicting the anomalies peculiar to soft-switched ACRDCL converters.

Three methods are identified for control and mitigation of common-mode current: 1) active common-mode current control; 2) inherent common-mode current control through current-mode switch state selection, such as delta modulation on the active rectifier; and 3) active common-mode voltage reduction through inhibiting zero-state voltage selections by the inverter.

Paralleled drive systems were designed and built to meet demanding input current and output voltage THD and input/output conducted EMI requirements. The output voltage THD requirement was met only through utilizing a control technique to maximize voltage utilization at the maximum output voltage (synchronous frame current regulators feeding VSDM ACRDCL inverters). The design also required very high packaging density. Practical implementation showed that common-mode circulating current amplitudes were excessive for low inverter output voltage conditions. Furthermore, the common-mode current saturated the EMI filter inductor, which leads to spurious overcurrent trips and degraded EMI performance. Due to practical limitations in the number and resolution of current sensors, common-mode current regulation could be implemented only through delta modulation on the active rectifier to mitigate this problem. However, the active common-mode voltage reduction proved effective in reducing common-mode circulating currents between drive systems to acceptable levels for low output voltage conditions.

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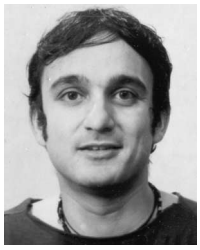

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