2004-10

Stress Management in Sub-90-nm Transistor Architecture

Arghavani, R.; Mascarenhas, A.; Yuan, Z.; Ingle, N.; Jung, K.B.; Seamons, M.; Venkataraman, S.; Banthia, V.; Lilja, K.; Leon, P....

IEEE

Arghavani, R., et al. "Stress management in sub-90-nm transistor architecture." IEEE Transactions on electron devices 51.10 (2004): 1740-1744.
https://hdl.handle.net/10945/60317

Stress Management in Sub-90-nm Transistor Architecture

R. Arghavani, Z. Yuan, N. Ingle, K-B Jung, M. Seamons, S. Venkataraman, V. Banthia, K. Lilja, P. Leon, G. Karunasiri, S. Yoon, and A. Mascarenhas

***Abstract*—This brief focuses on the physical characteristics of three dielectric films which can induce a significant degree of tensile or compressive stress in the channel of a sub-90-nm node MOS structure. Manufacturable and highly reliable oxide films have demonstrated, based on simulation, the ability to induce greater than 1.5-GPa tensile stress in the Si channel, when used as shallow trench isolation (STI) fill. Low–temperature blanket nitride films with a stress range of 2 GPa compressive to greater than 1.4 GPa tensile were also developed to enhance performance in both PMOS and NMOS devices. Combined with a tensile first interlayer dielectric film, the stress management and optimization of the above films can yield significant performance improvement without additional cost, or integration complexities.**

***Index Terms*—Dielectric films, semiconductor device fabrication, semiconductor films.**

I. Introduction

Despite significant challenges to device scaling, Moore's Law has continued to be a driver for the semiconductor industry. In order to continue conventional CMOS device scaling to its extreme theoretical limit and to keep Moore's Law on track, technologists are using strain engineering to further enhance and extend device performance. Unlike junction engineering, gate oxide scaling or poly CD reduction, only strain engineering is able to deliver enough performance boost to enable Moore's Law beyond the 90-nm node [1], [2]. The nearly 4.2% lattice mismatch between the single crystal Ge and Si lattice structure is the foundation of strain engineering in the silicon industry. The electronic conduction and valence band structure of SiGe was well established following the early preparation of homogenous SiGe alloys nearly four decades ago [3], [4]. The advent of pseudomorphic deposition of Si on $Ge_x Si_{1-x}$ extended this understanding to strained lattice structure and enabled examination of electrical characteristics of strained-Si [5]. The cited work conclusively predicted strained-Si to have higher carrier mobility than the relaxed Si lattice structure. The enhanced mobility in strained-Si is partly due to reduced intervalley phonon scattering and lower effective mass. The induction of localized strain via deposition of dielectric films is an alternative way to induce localized stress in the channel of sub-90-nm devices. Films like salicide, oxide and nitride spacers can affect device performance by inducing strain in addition to other effects. In this brief we focus on three dielectric layers that, when integrated, can create significant strain in the channel of a MOS device. In particular, we discuss the phenomenon of stress magnification in the channel of a sub-90-nm device.

Manuscript received July 28, 2004. The review of this brief was arranged by Editor V. R. Rao.

R. Arghavani, Z. Yuan, N. Ingle, K.-B. Jung, M. Seamons, S. Venkataraman, and V. Banthia are with Applied Materials, Santa Clara, CA 95054 USA (e-mail: Reza_Arghavani@amat.com).

K. Lilja and P. Leon are with Mixed Technology Associates, Newark, CA 94560 USA

G. Karunasiri is with the Department of Physics, Naval Postgraduate School, Monterey, CA 93943 USA.

S. Yoon and A. Mascarenhas are with the National Renewable Energy Laboratory, Golden, CO 80401 USA.

Digital Object Identifier 10.1109/TED.2004.835993

II. Trench Isolation

Despite its compressive nature and degradation of NMOS mobility, high density plasma (HDP) is currently the most commonly used gap-fill technology for shallow trench isolation (STI) applications due to ease of polishing and superior wet etch rate results. As geometries shrink, however, the issue of stress and the degradation of NMOS mobility caused by films deposited via HDP technology could be a significant process disadvantage. For example, although STI depth has remained nearly constant in the past few technology nodes, the pitch in a 65-nm node could be as aggressive as < 200 nm. Combined with an estimated poly pitch of less than 200 nm, trench processing can induce significant stress in the channel of the minimum design rule structures. Scott *et al.* [6] first reported considerable reduction of NMOS I_{dsat} as the device width decreases, for a given device length. They therefore concluded that the effect of HDP compressive stress is more profound on the NMOS device performance; PMOS performance remained unaffected by decreasing width.

In this brief, we will discuss an innovative product, the high aspect ratio process (HARP), developed using a new O_3/ tetraethoxylonesilane (TEOS)-based subatmospheric chemical vapor deposition trench fill process. This technology is intended to have two key benefits: a greater than 6:1 aspect ratio gap-fill capability without voids or seams; and the ability to tune an induced stress on silicon. As deposited, this film is nearly 200-MPa tensile. Due to absorption of moisture from the air, the film stress changes from tensile toward compressive over a period of 24 h. By properly annealing the film in an inert gas or a gas with nitridizing agent we can stabilize and tune the stress (Fig. 1). Depending on annealing conditions and ambient gas such as N_2, N_2O, NO or NH_3 one can tune the final stabilized stress to a value from tensile to compressive.

Modeling showed that the high aspect ratio of the shallow trenches at the sub-90-nm node increase the stress near the surface of the silicon. Furthermore the visco-elastic relaxation of the stresses in the deep trench is so much slower than the stress relaxation in a plain oxide film, that with suitable process control, the STI process can control channel stresses. Many steps in the front end of the process also generate mechanical stress, but in general the generated stresses add/subtract to the stress generated by the STI. Note, the steps that substantially change the structure of the silicon or trench (e.g., S/D SiGe epi), also directly change the stresses caused by the STI process.

In our simulations we have used a visco-elastic model, with parameters from Senez *et al.* [7], [8]. After some small calibration adjustments of the model parameters, the model well captures the annealing behavior of the blanket oxide film. The elastic mechanical stresses are created by the difference in the temperature expansion coefficient between silicon and the oxide trench fill. In addition, when the trench fill comprises the new TEOS-based oxide, the structural rearrangement of oxide during the anneal process causes the material to contract, giving rise to additional (and opposing) stresses. At high temperatures ($> 800\ ^\circ$C) and at high stresses the oxide becomes viscous, and the elastic stresses relax. The distribution of the lateral stress component is shown in Fig. 2. In the simulations the HDP oxide is assumed relaxed at the process temperature of 900 °C and the temperature is then ramped down to room temperature. The oxide has a smaller thermal expansion coefficient than silicon, thus, the HDP oxide will not shrink as much as the silicon during ramp down. Hence, a compressive lateral stress will be generated in the structure. In the tensile oxide process, the reactions in the oxide during ramp up cause it to shrink, and generate strong tensile stresses. The tensile stresses are partly relaxed by the viscous flow of the oxide at high temperatures, and somewhat reduced during ramp down due to the larger thermal expansion coefficient of

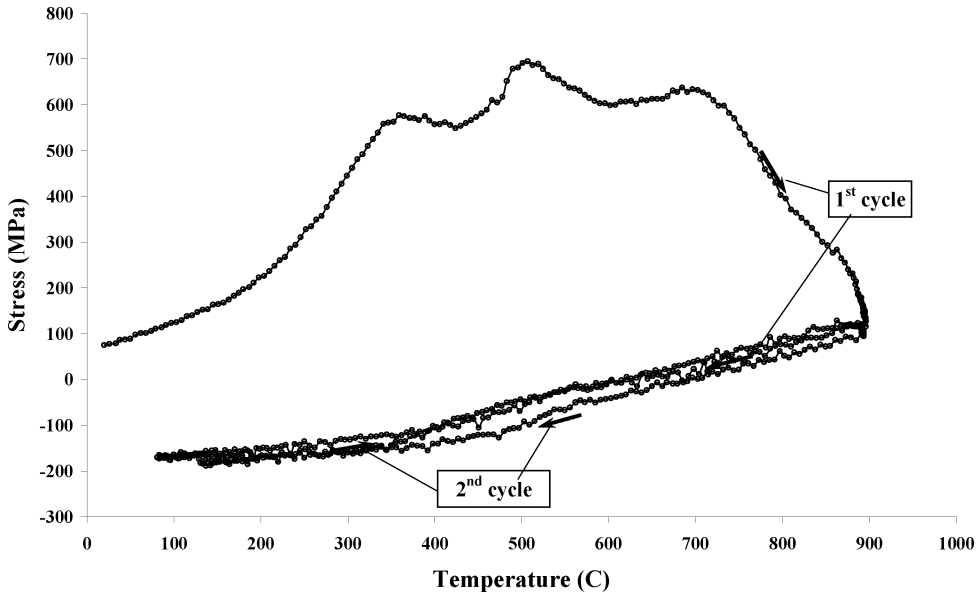

Fig. 1. Hysteresis effect of the as deposited film as a function of temperature (nitrogen ambient). The stress of the film is fully stable after the first anneal cycle.

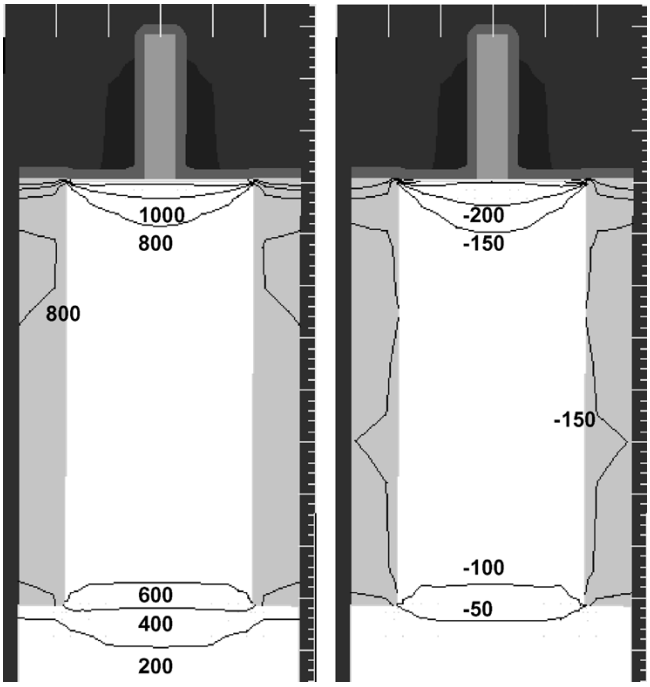

Fig. 2. Lateral component of the stress (MPa) generated by simulation in the HDP process (right) and the newly developed process (left). The figure shows the whole structure with the silicon (white) in the middle surrounded by STI (grey). Poly and spacer are shown on top, but were not included in the simulation.

silicon. However, large tensile stresses can still remain in the structure after the completed process. Note that the lateral stress component increases (around 50%) from the mid-trench up toward the surface of the silicon. This increase is caused by the fact that the oxide contraction (as well as expansion) is both lateral and vertical. When the aspect ratio of the trench is large, the vertical contraction "amplifies" the tensile lateral stress at the surface of the silicon.

The one-dimensional simulation and the wafer bending experiment indicate that, if the oxide in the trench relaxes as much as the oxide film on the flat wafer, most of the tensile elastic stress would be relaxed in a typical annealing process. However, in the visco-elastic model for the oxide behavior the shear (deviatoric) stresses are relaxed much faster than the pressure (dilatational) component. Our modeling results show that as the aspect ratio increases (narrower trenches), the stress relaxation in the trench becomes much slower than in the film on top.

As discussed above, strained silicon improves NMOS device performance by increasing the mobility of carriers in the inversion layer. While the mechanism for electron mobility improvement is still a topic of research, the cause is often assumed to be a reduction in the intervalley acoustic phonon scattering rate, as well as a reduction in effective mass. Currently, the mobility models of standard device simulation programs do not include the effect of strained silicon on inversion layer mobility. However, Oldiges *et al.* [9] has demonstrated that adjusting the surface acoustic phonon scattering term in a standard mobility model is an effective approximation; this is the approach adopted here. Using the Darwish–Klaasen [10] mobility model, the mobility parameters were tuned so as to match the universal mobility data as well as strained silicon mobility data for varying values of the surface acoustic scattering coefficient. The calibrated mobility model was then used in numerical device simulation to estimate the impact of the improved mobility on drain current. The device structure used was the so-called "MIT 50-nm well-tempered MOSFET," one of a series of MOS device structures commonly used in the academic community for scaling and carrier transport research [11]. The results, as seen in Fig. 3, show a larger than 12% increase in drain current for strain. This is equivalent to tensile strain of 1.6 GPa. Experimentally, we verified these results, using micro-Raman scattering measurement. Fig. 4 shows the measured Raman scattering peaks for HARP and HDP along with the Si substrate. The data indicates that Si with HARP is under tensile stress to about 218 MPa while the Si channel with the HDP filled trenches is under compressive stress to about 43 MPa. It is important to note that the measured data represents the average stress in the layer since the excitation light penetrates into the unstressed silicon substrate.

III. Nitrides and First Interlayer Dielectric

An alternative method of local stress induction is applied post salicidation via deposition of a stress inducing nitride layer [1], [2]. In most published brief the stress of the nitride is tuned to tensile. As a result, the silicon beneath would be compressive. The channel of the transistor

TABLE I
AREA/POSITION OF THE THREE PEAKS AND DEPENDENCE OF RATIO/SUM OF N–H AND SI-H AS A FUNCTION OF STRESS

Stress	N-H Line		Si-H Line		Si-N Line		N-H/Si-H Ratio	Sum of N-H & Si-H Areas
GPa	Area	(cm^{-1})	Area	(cm^{-1})	Area	(cm^{-1})	-	-
-1.311	2.05	3332	0.61	2216	59.18	855	3.36	2.66
-0.604	1.86	3337	0.88	2205	57.08	849	2.11	2.74
-0.261	1.52	3339	1.2	2195	59.93	842	1.27	2.72
0.032	1.3	3345	1.34	2188	49.7	837	0.97	2.64
0.468	1.04	3351	2.39	2175	49.97	835	0.44	3.43
0.727	1.06	3356	2.27	2170	39.61	838	0.47	3.33
1	0.59	3357	2.48	2168	34.19	830	0.24	3.07

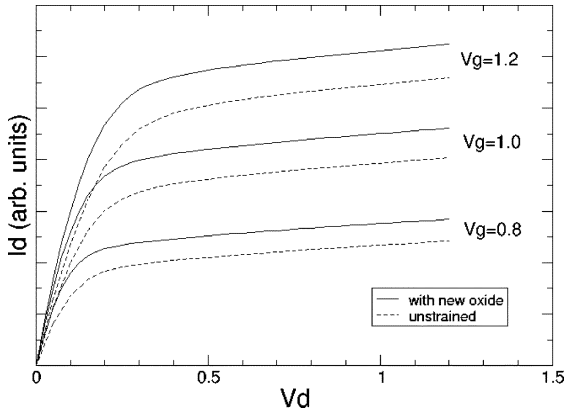

Fig. 3. Drive currents of a simulated NMOS device for stress conditions predicted by the simulations presented in Fig. 2(left).

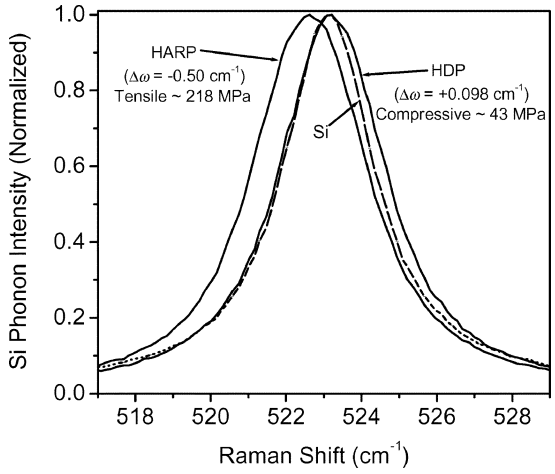

Fig. 4. Micro-Raman average stress comparison of the HARP and HDP filled trenches. The averaged stress in the first 150 nm of Si contributes to the frequency shift signal. Clearly the shift in the frequency indicates an enhanced tensile stress in Si via HARP processing. Note that the magnified stress at the surface of Si (first 50 nm) is averaged with that of the more relaxed Si lattice in the bulk.

would respond to this compressive force by becoming tensile. Nitride deposition, in this brief, is done at a low temperature of 400 °C. Both liquid and gas based silicon sources can be combined with NH_3 to deposit a conformal nitride at low temperature. Other physical characteristics of the film such as etch rate and index of refraction are kept nearly constant throughout this stress variation range.

It is known that the incorporation of hydrogen during the plasma-enhanced chemical vapor deposition (PECVD) growth into the silicon nitride film generates N–H and Si–H bonds in addition to dominant Si–N

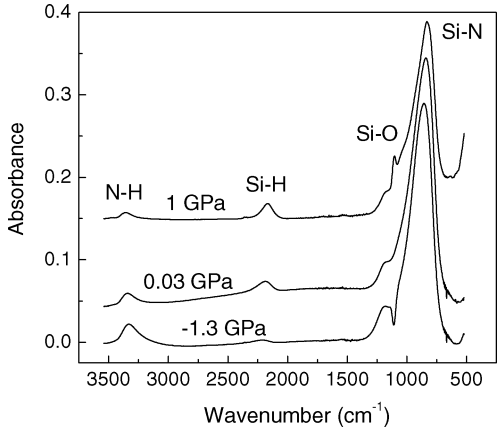

Fig. 5. FTIR spectra showing the N–H, Si–H, Si-O, and Si–N peaks of three samples used in this brief. Note that the spectra are shifted along the vertical axis for clarity.

bonds [12]. The presence of N–H and Si–H bonds plays an important role in determining the stress of the SiN film. Fig. 5 shows the measured absorption FTIR spectra for samples with stresses varying from high compressive to high tensile. Notice that the peak position and absorption strength of the N–H, Si–H, and Si–N vibration modes are affected by the degree of stress in the film.

Table I summarizes the measured N–H, Si–H, and Si–N peak position (cm^{-1}) and the area under each absorption peak. Notice that the N–H peak position increases with the increasing tensile stress, while the opposite behavior is observed for Si–H and Si–N. To understand the role of hydrogen on the film stress, the ratio and sum of the peak areas of N–H and Si–H were calculated. It can be seen that the sum of the N–H and Si–H peak areas remains nearly the same, indicating that total hydrogen content of the films are nearly the same, which was confirmed by the NRA measurement. In addition, as the film becomes more tensile the N–H/Si–H ratio decreases which indicates an increase in Si–H bonds and a decrease in N–H bonds, since the total hydrogen content remains nearly the same. It is known that the formation of Si–H bonds tends to reduce the strength of remaining Si–N bonds attached to the same Si atom due to the electro-negativities of Si, N and H atoms [13]. This implies that as the films become more tensile, the Si–N peak position will red shift, which is clearly seen from the measured Si–N peak positions. As the Si–N bond strength weakens, its length increases, which amounts to a stretching of the SiN film making it more tensile. This can produce a larger compressive stress on the underlying Si substrate. In addition, the weaker Si–N bonds can strengthen the remaining N–H bonds making the N–H peak position blue shift. This was clearly observed in the FTIR measurement when the stress in SiN film changes from 1.3 GPa compressive to 1 GPa tensile the N–H peak position changed from 3332 cm^{-1} to 3357 cm^{-1}. It was also found

that as the Si–H concentration increases, the peak position of the Si–H bond decreases in energy (lower wave number), indicating the increase of the Si–H bond length. One possible explanation is that the stretching of the Si–H bonds is due to attractive force on hydrogen atoms by the nitrogen atoms, which have donated hydrogen atoms to silicon to increase the Si–H concentration. Similar enhancement of attraction was also observed between the remaining N–H bonds as the film becomes more tensile. This study shows that the higher ratio of Si–H bonds to N–H bonds, for a given amount of hydrogen in a SiN film, plays an important role on the stress of the film.

One way of changing the magnitude of the stress in the channel is to modulate the thickness of the nitride film. Due to restrictions on lithography and etch, however, the nitride film cannot be thick enough to allow extension of the stress inducing nitride process to future nodes. In general, the nitride layer film is followed by a first interlayer dielectric deposition, which in most processes is a fixed nontunable compressive film. In this brief we tuned the stress of the nitride and then enhanced the magnitude of the locally induced stress on silicon by depositing a stress tunable first interlayer dielectric, i.e., we used this subsequent layer to increase the effective thickness of the stress inducing nitride layer.

IV. Conclusion

We have demonstrated three dielectrics films that, when integrated together, can induce a significant degree of strain into the channel of a sub-90-nm device. Due to tunability of stress, both PMOS and NMOS devices can benefit from the above films, depending on which integration methods are implemented. Combined with traditional techniques to induce stress in the channel, such as SiGe processing, this unique stress management can significantly boost the next-generation device performance and extend Moore's law.

Acknowledgment

The authors would like to thank E. Yieh, General Manager of the Gap Fill Division, H. M'Saad, Vice President and General Manager of the Blanket Film Division and F. Moghadam, Group Vice President and General Manager of Dielectric System Modules at Applied Materials for valuable discussion and continuous support of this program.

References

[1] T. Ghani *et al.*, "A 90-nm high volume manufacturing logic technology featuring novel 45-nm gate length strained silicon CMOS transistors," in *IEDM Tech. Dig.*, 2003, pp. 978–980.

[2] M. Yang *et al.*, "High performance CMOS fabricated on hybrid substrate with different crystal orientations," in *IEDM Tech. Dig.*, 2003, pp. 453–456.

[3] R. Braunstein, A. Moore, and F. Herman, "Intrinsic optical absorption in germanium-silicon alloys," *Phys. Rev.*, vol. 109, pp. 695–710, 1958.

[4] F. Herman, "Speculation on the energy band structure of Ge-Si alloys," *Phys. Rev.*, vol. 95, pp. 847–848, 1954.

[5] R. People, "Physics and applications of Ge_xSi_{1-x} strained-layer heterostructures," *IEEE J. Quantum Electron.*, vol. QE-22, pp. 1696–1710, Sept. 1986.

[6] G. Scott, J. Lutze, M. Rubin, F. Nouri, and M. Manley, "NMOS drive current reduction caused by transistor layout and trench isolation induced stress," in *IEDM Tech. Dig.*, 1999, pp. 827–830.

[7] J. Egley and D. Chidambarrao, "Strain effects on device characteristics: Implementation in drift-diffusion simulators," *Solid State Electron*, vol. 36, no. 12, pp. 1653–1664, 1993.

[8] V. Senez, P. Ferreria, and B. Baccus, "Two-dimensional simulation of local oxidation of silicon," *IEEE Trans. Electron Devices*, vol. 43, pp. 720–731, May 1996.

[9] P. Oldiges, X. Wang, M. Ieong, S. Fischer, and K. Rim, "A practical approach to modeling strained silicon NMOD devices," in *Proc. SISPAD*, 2001, pp. 292–295.

[10] M. Darwish, J. Lentz, M. Pinto, P. Zeitzoff, T. Krutsick, and H. H. Vuong, "An improved electron and hole mobility model for general purpose device simulation," *IEEE Trans. Electron Devices*, vol. 44, pp. 1529–1538, Sept. 1997.

[11] J. L. Hoyt *et al.*, "Strained silicon MOSFET technology," in *IEDM Tech. Dig.*, 2002, pp. 23–26.

[12] F. Ootsuka *et al.*, "A highly dense, high performance 130-nm node CMOS technology for large scale system-on-a-chip applications," in *IEDM Tech. Dig.*, 2000, pp. 575–578.

[13] R. C. Budhani, S. Prakash, H. J. Doer, and R. F. Bunshah, "Structural order in Si–N and Si–N-O films prepared by plasma assisted chemical vapor deposition processes," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 5, pp. 1644–1648, 1987.

Nitride-Based LEDs With Modulation-Doped $Al_{0.12}Ga_{0.88}N$–GaN Superlattice Structures

T. C. Wen, S. J. Chang, C. T. Lee, W. C. Lai, and J. K. Sheu

***Abstract*—Modulation doped $Al_{0.12}Ga_{0.88}N$–GaN superlattice structures were used to spread pulse current in nitride-based light emitting diodes (LEDs). Although the 20-mA electroluminescence (EL) intensity of the LEDs with modulation-doped AlGaN–GaN superlattice structures was found to be 10% smaller than that of the conventional LEDs, it was found that LEDs with the AlGaN–GaN superlattice structures could all endure a 2000-V reverse electrostatic discharge (ESD) pulse voltage. Some LEDs can even survive with an 8000-V reverse ESD pulse voltage, which is equivalent to "Class 3B" of Human Body Mode testing.**

***Index Terms*—Current spreading, electroluminescence (EL), electrostatic discharge (ESD), light-emitting diodes (LED), modulation-doped AlGaN–GaN superlattice structures.**

Electrostatic discharge (ESD)-induced electrical pulse is one of the main reliability concerns of optoelectronic devices. ESD damaged devices can appear dim, dead or shorted. Generally speaking, nitride-based optoelectronic devices [1] are considered "Class 1" devices [2], which can be destroyed by a discharge of only 10 V. Thus, it is extremely important to improve ESD reliability of the nitride-based devices. To our knowledge, only very few reports regarding to the ESD effects could be found in the literature, particularly for those related to GaN-based optoelectronic devices [3]–[5]. Previously, it has been shown by Inoue *et al.* that one can combine GaN light-emitting diodes (LEDs) with Si-based Zener diodes through flip-chip process

Manuscript received May 5, 2004; revised July 9, 2004. This work was supported by the National Science Council of Taiwan, R.O.C., under Contract NSC-89-2215-E-006-095. The review of this brief was arranged by Editor C.-P. Lee.

T. C. Wen, C. T. Lee, and W. C. Lai are with the Institute of Microelectronics and Department of Electrical Engineering, National Cheng Kung University, Tainan 70101, Taiwan R.O.C.

S. J. Chang is with the Institute of Microelectronics and Department of Electrical Engineering, National Cheng Kung University, Tainan 70101, Taiwan R.O.C. He is also with the Center for Micro-NanoTechnology, National Cheng-Kung University, Tainan, 70101, Taiwan, R.O.C.

J. K. Sheu is with the Institute of Optical Science, National Central University, Chung-Li 320, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TED.2004.835985