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Naval Postgraduate School NPSAT1 Small Satellite

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NAVAL POSTGRADUATE SCHOOL NPSAT1 SMALL SATELLITE

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ABSTRACT

The NPSAT1 mission, conceived and developed by the Naval Postgraduate School (NPS) Space Systems Academic Group (SSAG), is sponsored and executed by the DoD Space Test Program (SMC SDD). The small satellite is manifested for launch aboard the STP-1 Atlas V Mission due to launch in December 2006. The main objective of the NPSAT1 program is to provide educational opportunities for the officer students in the Space Systems Curricula at NPS through the design, testing, integration, and flight operations of a small satellite. The 82 kg (180 lbs) satellite will be earth-pointing using a novel, low-cost, 3-axis attitude control scheme. NPSAT1 will provide a platform for a number of spacecraft technology experiments, including a lithium-ion battery, a configurable, fault-tolerant processor (CFTP) experiment, and flight demonstrations of commercial, off-the-shelf (COTS) components such as microelectromechanical systems (MEMS) rate sensors and a digital camera. The spacecraft command and data handling (C&DH) subsystem is NPS-designed, featuring low-power with error-detection-and-correction (EDAC) memory, an ARM720T microprocessor, and running Linux as the operating system. Two other experiments are provided by the Naval Research Laboratory to investigate ionospheric physics. This paper presents an overview of the spacecraft, its subsystems, and the challenges of a small satellite program in a university environment.

1. NPS SPACE SYSTEMS EDUCATION

The Naval Postgraduate School (NPS), located in Monterey, California is a graduate school of the U.S. Navy. Officer students are represented from all U.S. military services, as well as the military services from approximately 30 other countries. Curricula are taught in areas relevant to the Navy's interests as well as those interests of the Department of Defense. NPS offers graduate programs through its four graduate schools of Business and Public Policy, Engineering and Applied Sciences, Operational and Information Sciences, and the School of International Graduate Studies. The NPS Space Systems Curricula fall under the Graduate School of Engineering and Applied Sciences and is administered by the Space Systems Academic Group.

The NPS Space Systems Curricula include the Space Systems Operations (SSO) curriculum and the Space Systems Engineering (SSE) curriculum. Both curricula encompass a rigorous technical core of courses in space systems areas, such as orbital mechanics, satellite communications, space environment, remote sensing, and space mission design courses. The SSO curriculum focuses on the operations side of space as a means of gaining insight into space system concept of operations, requirements, and architectures with graduates receiving a Master of Science in Space Systems Operations conferred by the NPS Space Systems Academic Group. The SSE curriculum focuses on the engineering aspects of space systems with graduates receiving a Master of Science int the particular engineering discipline of study, such as Mechanical and Astronautical Engineering, Physics, Electrical and Computer Engineering, and the like. A space-related Master's thesis is a requirement for both curricula.

Research is another focus at NPS where students and faculty work in support of the Department of Defense on solutions to a myriad of military issues, including new technologies, computer security, communications, and operations. Research is conducted at NPS in every academic department, school, and institute. NPS hosts a number of unique facilities for research as well as area expertise provided through the highly qualified faculty. In the 2005 fiscal year, NPS had expenditures totaling $80.4 million in sponsored programs [1].

The Space Systems Academic Group (SSAG) has been managing the NPS space systems curricula since 1982. One thrust has been the inclusion of space flight hardware development from very early in the program's history. NPS has flown space flight experiments as piggy-back experiments, such as the FERRO experiment on the Apex satellite [2]; a Shuttle Get Away Special (GAS) thermoacoustics experiment [3]; sounding rocket experiments; and a Shuttle-launched small satellite, PANSAT [4]. Space flight experiments at NPS have evolved into the current Small Satellite Design Studies Program with its objectives to provide 'hands-on' opportunities and exposure to the full life-cycle

development of a space system, to advance spacecraft technology, and to provide a platform for space flight experiments. The current satellite program is the NPS Spacecraft Architecture and Technology Demonstration Satellite, NPSAT1. Integration and launch of NPSAT1 is provided through the Department of Defense Space Test Program where NPSAT1 was ranked among other defense-related experiments for flight and manifested on the STP-1 launch. The NPSAT1 mission, conceived and developed by the Naval Postgraduate School (NPS) Space Systems Academic Group (SSAG), is sponsored and executed by the DoD Space Test Program (SMC SDD).

2. NPSAT1 MISSION OBJECTIVES

The primary objective of NPSAT1 is the education of officer students. This includes the design, analysis, and testing of electronics, software, and mechanical subsystems. Operationally, students define concept of operations, ground system development, and flight operations development and rehearsals. System assembly, test, launch, and flight operations are also key areas for student involvement. Officer students generally are involved through directed study or thesis work.

The second objective of NPSAT1 is to provide a platform for experiment payloads, some of which are part of the spacecraft bus. NPSAT1 carries higher risk as a space system because of the limited resources in an university environment. As a means of mitigating risk, reliability is ensured through thorough testing. Testing of NPSAT1 is focused at the subsystem level where, hopefully, most all of the subsystem anomalies can be detected and fixed. Interface issues that can arise will be caught with thorough system-level functional and environmental testing.

3. SPACECRAFT DESCRIPTION

The NPSAT1 satellite program can be roughly separated into two segments: the space segment and the ground segment. The space segment includes the spacecraft bus, the experiment payloads, and the design addressing issues concerning the space environment, such as effects due to radiation or the thermal environment. The ground segment can be divided between the actual ground station hardware and software for communications, data handling, and user interface, and the ground operations portion which defines the day-to-day operations of the spacecraft and experiments. Greater attention is given here in describing the development of the spacecraft and experiments. Some changes were made from NPSAT1's baseline design [5] in order to offer greater flexibility and robustness in the development or the on-orbit operation of the spacecraft. Two of the major changes were the switch from an Intel X86 architecture for the command and data handler to an ARM-based processor, and the addition of a GPS receiver. Two minor changes was the addition of a backup momentum wheel and the decision to remove lithium-ion polymer batteries, originally planned as both a secondary energy storage medium as well as an experiment. A block diagram of the NPSAT1 spacecraft is given in Fig. 1.

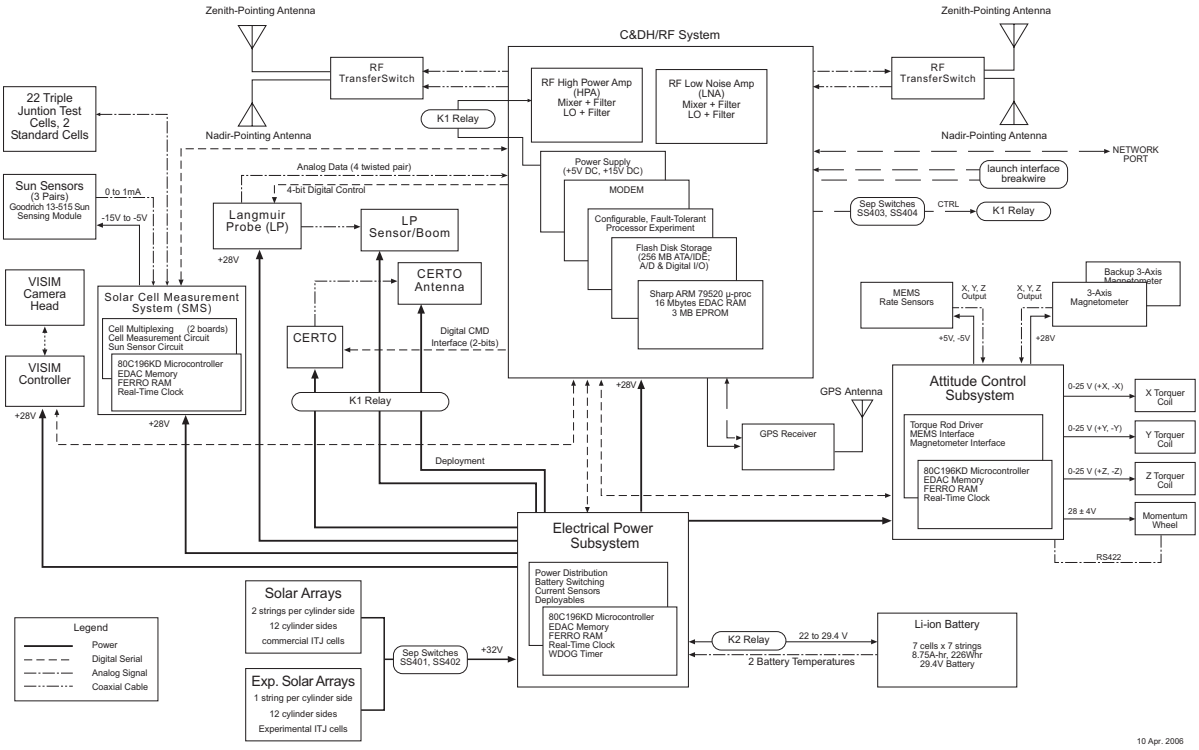


Figure 1. NPSAT1 Block Diagram.

NPSAT1 is a 82 kg [180 lb] satellite configured to interface with the expendable launch vehicle (EELV) secondary payload adapter (ESPA) [6]. The overall configuration is shown in Fig. 2, with the top, side, bottom, and isometric views shown. Fig. 3 shows an expanded assembly drawing of the spacecraft depicting modules located within the spacecraft. The spacecraft is a 12-sided cylinder with body-mounted solar cells on all of the cylinder sides. Antennas are located on both ends of the cylinder to ensure communications with the satellite. Two deployable booms are mounted on the base plate, the CERTO beacon antenna and Langmuir probe boom.

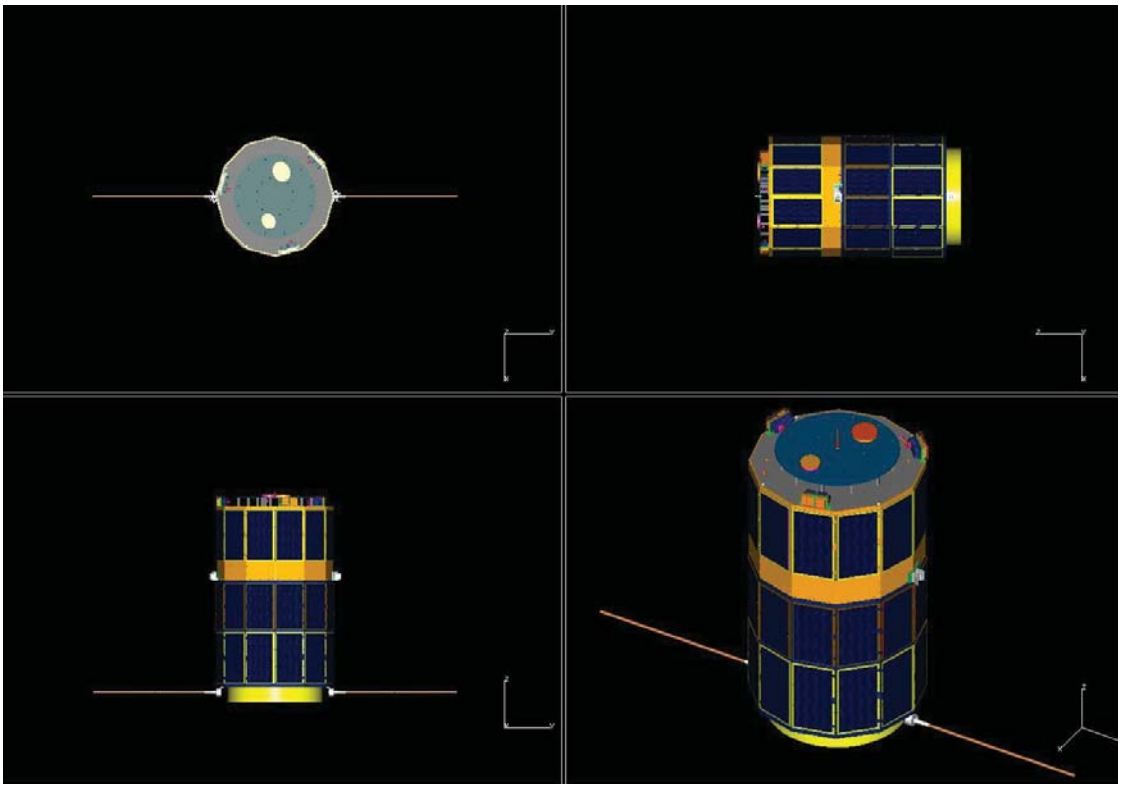


Figure 2. NPSAT1 Configuration Views.

Two equipment decks, in addition to the base plate and the top plate, are located internally and are used for mounting the electronics housings. Mass distribution is of concern in order to maintain favorable moments of inertia for the attitude control subsystem, i.e., $I_{YY} > I_{XX} > I_{ZZ}$. Although not explicitly shown in the figure, a major task is the buildup of the electrical harness which takes into account features to mitigate electromagnetic interference (EMI) issues.

4. EXPERIMENT PLATFORM

NPSAT1 will host a number of experiments some of which are standalone experiments, and others part of the spacecraft bus. Two experiments will be provided by the Naval Research Laboratory (NRL), the coherent electromagnetic radio tomography (CERTO) experiment (a three-frequency beacon) and a Langmuir probe. The other experiments are NPS-built. These are a lithium-ion battery, a solar cell measurement system (SMS) experiment, a configurable fault-tolerant processor (CFTP) experiment, two commercial, 'off-the-shelf' (COTS)-based experiments, a three-axis micro-electromechanical systems (MEMS) rate sensor, and a color digital camera called the visible wavelength imager (VISIM).

5. SUBSYSTEMS AND EXPERIMENTS

5.1 Command and Data Handling (C&DH) Subsystem

The Command and Data Handling subsystem (C&DH) contains several electronic boards which are attached using a PC/104 bus and housed within one box. The circuit boards are a motherboard, a mass storage and A/D and digital output board, the configurable fault tolerant processor (CFTP) experiment board, a power supply and modem and radio frequency (RFS) components. The PC/104 bus is modified to carry alternate signals between the C&DH board stack to allow special operations. However, the bus still allows for use with PC/104 stacks during development.

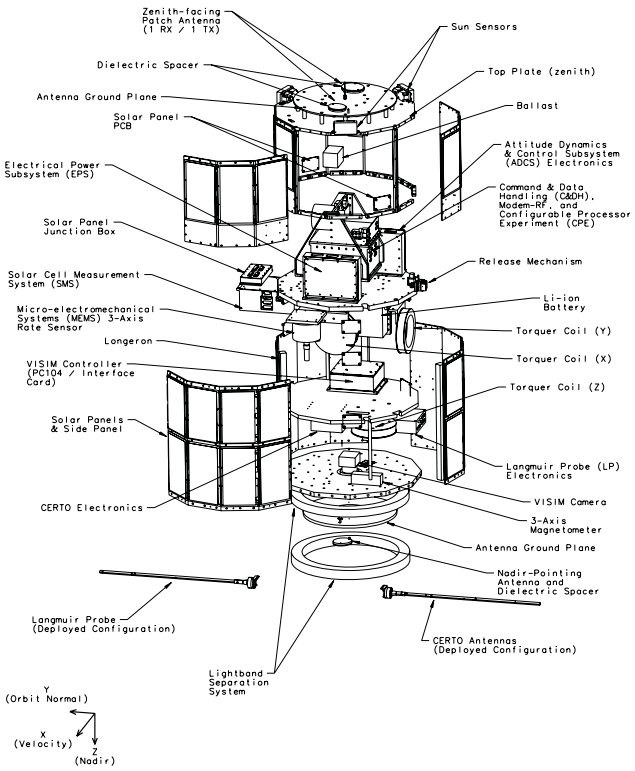


Figure 3. Expanded View of the NPSAT1 Spacecraft.

5.1.1 C&DH Motherboard

The C&DH motherboard is the heart to the spacecraft computer systems. A Sharp LH79520 ARM microprocessor operating at 51 MHz is the CPU of the C&DH. This is a 720T ARM core supporting a 32-bit processor, memory management unit, clock and power management, watchdog timer, three universal asynchronous receiver/transmitter (UART), programmable general purpose input/output, and JTAG interface. The motherboard also contains a Xilinx XCV100 field programmable gate array (FPGA). Essentially nearly all of the ARM signals interface to the FPGA. This allows complete manipulation of microprocessor signals between other devices within the C&DH which can be modified via software reconfigurations during development.

The C&DH motherboard memory consists of 64 kbytes of PROM that contains the boot loader, operating system decompressor, and various low-level tools for system testing and configuration. There are four Sharp LH28F32 flash memory devices, each four Mbytes, which contain quadruplicated versions of the operating system and rootdisk. There are 16 Mbytes of error-detected-and-corrected (EDAC) static RAM. The FPGA implements the EDAC logic and control and interfaces with the SRAM. One-bit error correction and two-bit error detection is possible using the EDAC.

The Linux 2.4.17 operating system has been ported to the motherboard providing a mature and rich software platform for the spacecraft software. Linux is a POSIX-compliant operating system. It was chosen for several reasons. It is open-source software which is robust and highly configurable. Linux is also multitasking and a Unix-like software environment with which the software development personnel have extensive experience. There are plenty of powerful software development tools that are freely (as in no cost) available. Currently the operating system is about 560 kbytes compressed and 890 kbytes uncompressed. The rootdisk is a compressed version of the system application software which must always be present when the C&DH starts up. Currently the compressed rootdisk is about 820 kbytes and about 1.8 Mbytes uncompressed. There is a limit of compressed operating system and rootdisk sizes of one Mbytes and three Mbytes respectively. The uncompressed operating system and rootdisk must uncompress to no more than 5 Mbytes.

An addition to the three UARTs on the LH79520 the C&DH motherboard also contains the Texas Instruments TL16C754B, a quad-port UART. This device provides the four serial channels to the other spacecraft subsystems: ACS, EPS, SMS, and VISIM. A simple protocol operating at 9600 bits per second is used to communicate with the ACS, EPS, and SMS subsystems. The interface with the VISIM is via PPP at 115.2 kbits per second. A complete network socket interface is available between the C&DH and the VISIM.

The ARM cores are known for very low power consumption while providing a powerful architecture for modern operating system support. The C&DH motherboard with the switching power supplies operate at 3.3 Watts of power.

5.1.2 Mass Storage and A/D and Digital Output Board

The mass storage is an array of Sharp flash LHF54 memories. There are eight devices, each with 8 Mbytes, for a total of 64 Mbytes of mass storage. Using flash chips which are common flash interface (CFI) compliant and the memory technology device (MTD) support offered within the Linux kernel provides a sophisticated mass storage unit which will be used for recording experiment data before down-linking to the NPSAT1 ground station.

Two National Semiconductor LH12H458 Analog-to-digital (A/D) devices digitize various analog signals used by the C&DH. One device interfaces with signals within the C&DH. The other device will digitize the four analog channels from the Langmuir Probe at rates up to 1 kHz.

5.1.3 Power Supply, Modem, and RFS board

The C&DH power supply provides all of the power conditioning (1.8V, 2.5V, 3.0V, 3.3V, 5.0V, and 15.0V DC) for all the electronics within the C&DH housing.

The RFS components within the C&DH housing are isolated from the other C&DH electronics to reduce electromagnetic interference. The modem and RFS are physically located in the bottom portion of the C&DH housing. The modem and C&DH motherboard require intimate connection and thus the placement of the modem within the C&DH. Discussion of the modem and RFS is in the RFS section.

5.2 Electrical Power Subsystem (EPS)

The electrical power subsystem (EPS) consists of triple-junction solar cells for energy conversion, an experimental lithium-ion (Li-ion) battery for energy storage, and the electrical power distribution and control electronics, composed of a (digital) processor board and an analog/switching board. A portion of the solar cells are also used for the solar cell measurement system (SMS) experiment.

5.2.1 Solar Array

Each side of the 12-sided cylinder has three solar panels. Two of the panels are made up of commercial triple-junction solar cells, and the third of experimental triple-junction solar cells. All of the panels are tied into the solar panel power bus. Because the solar panel circuit is external to the spacecraft, care was taken to try to reduce unwanted noise into the system. All solar panel power lines are combined in the solar panel junction box which uses filtered connectors. From the solar panel junction box, power is routed to the EPS housing on the third deck.

5.2.2 Lithium-ion Battery

The flight battery is composed of 49 Sony US18650S Lithium-Ion hard harbon cells which were extracted from Sony BP-945 camcorder battery packs. The flight battery box will be maintained at one atmosphere. It is wired in a 7S-7P (7 cells in series, and 7 strings in parallel) configuration providing a battery capacity of 225 Whrs with a full charge voltage of 29.4 Volts. Fig. 4 shows a photo of the battery cells in the 7S-7P assembly. Each string has a current sensor to allow for the monitoring of the current flowing from the string with a maximum error of less than 1%. This data allows for the monitoring of current sharing between strings as the cell ages. This is important due to the fact that there is no charge control electronics at the string or cell level. Assuming that the battery successfully shares current between the strings throughout its lifetime, no charge control will ever be required. Therefore, the battery is less costly and the design is much simpler. There are two thermistors attached to two separate cells in the battery to allow for the monitoring of the battery box internal temperature. To maintain an optimal temperature for the battery, a heater is installed in the battery box.

Individual cell testing is another aspect of the flight battery. A MACCOR battery test system is used for testing. It consists of a total of 16 channels; 8 from a MACCOR 2200 series battery test system and 8 from a MACCOR 2300 series battery test system. The battery test hoods, which contain the individual cells being tested, are temperature controlled through the use of a recirculator. In addition, the temperature of each cell is individually monitored. Both MACCOR battery test systems are controlled by a single computer and data is retrieved from a dedicated server that is capable of retrieving data from multiple controller systems. There are currently low earth orbit (LEO) simulations and accelerated LEO simulations running at multiple current rates since 6 March 2006. The results of these tests have shown first of all that accelerated and non-accelerated testing are not showing comparable results when graphed as capacity versus number of cycles. However, the tests are more comparable when capacity loss is graphed versus actual calendar time. This shows that the degradation of capacity may be a function of time, cycles, or a combination of both. Fig. 5 shows the data plotted using both formats as described. There is further testing that needs to be done on this to validate current results.

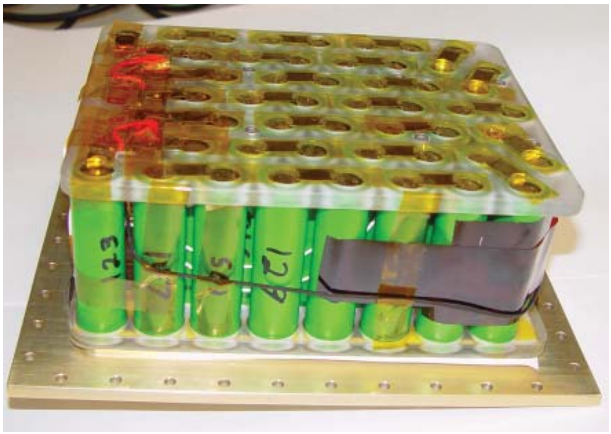
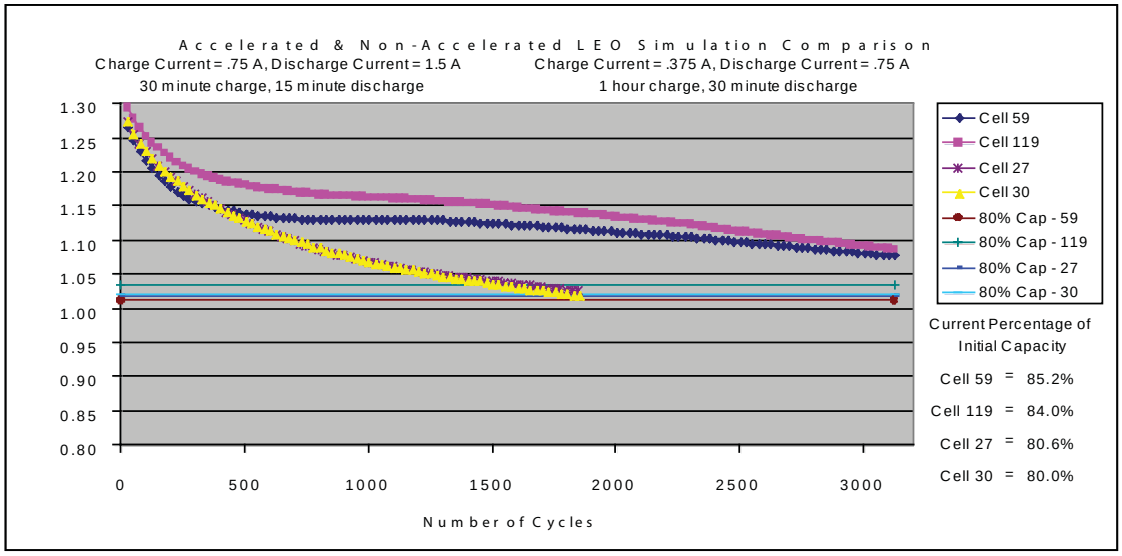


Figure 4. Lithium-Ion Battery Cell Assembly.

5.2.3 Electrical Power Distribution

The EPS electronics is designed around a rad-hard UTMC80C196KD micro-controller on the digital board. The digital board also hosts a real-time clock, rad-hard RAM, the watchdog timer for the C&DH, a serial port to interface with the C&DH, and 8 kilobytes of ferroelectric (FERRO) RAM memory. The analog/switching board hosts all the power distribution to the other subsystems to provide a spacecraft power bus of 24V to 40V. Each subsystem is responsible for regulating the power from the bus for its own specific requirements.



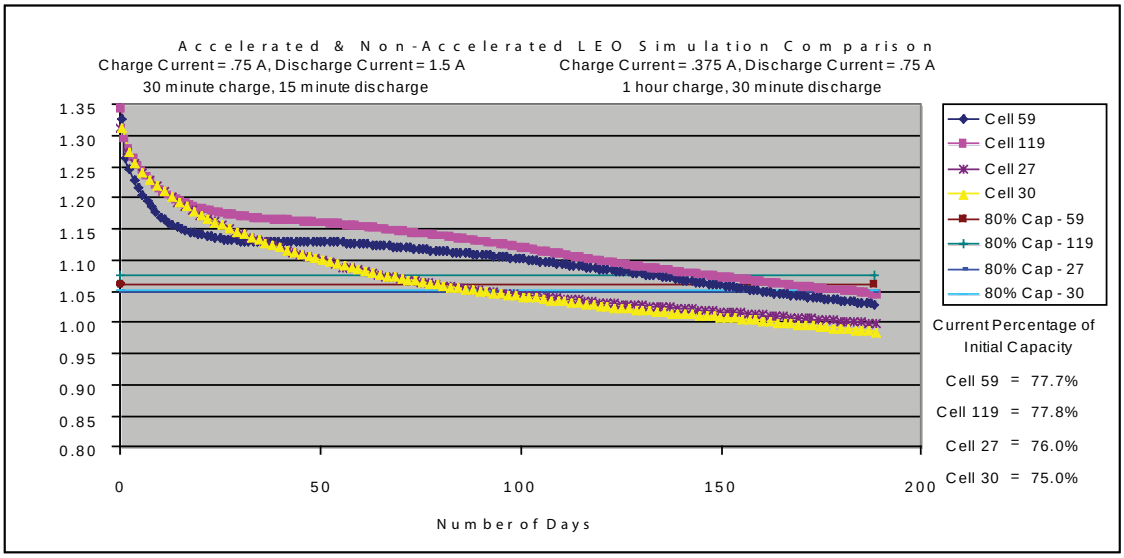


Figure 5. LEO Simulations Data and Accelerated LEO Data.

The analog/switching board is also responsible for taking measurements of such things as battery voltages and temperatures via 32 analog channels which are multiplexed in to a dual, 12-bit analog-to-digital (A/D) converter.

5.3 Attitude Control Subsystem (ACS)

The attitude control subsystem (ACS) consists of three magnetic torquer coils for actuators, a three-axis magnetometer as the sensor, and the ACS controller. Briefly, the ACS controller uses onboard orbit information to obtain the spacecraft's location and performs a table lookup to obtain the values for the local magnetic field vector at that latitude, longitude, and altitude. Magnetometer measurements are compared to the lookup value and the control algorithm attempts to null the error between the two. Although the magnetic field (B-field) vector gives only one reference vector, because the spacecraft is orbiting the Earth and is continually 'chasing' the B-field vector, three-axis stabilization can be achieved. Simulation results yield a pointing accuracy better than 2° can be achieved [7].

The ACS electronics is almost identical to the EPS controller. A processor board with a rad-hard UTMC80C196KD and rad-hard RAM will be used to implement the control algorithm. The analog board drives the torquer coils, and takes measurements from the magnetometer, MEMS rate sensor, and temperature sensors. The analog board also provides the electrical power for the MEMS rate sensor and magnetometer. Navigational information is provided by the simple two-body orbit propagator running in the C&DH.

5.4 Radio Frequency Subsystem (RFS)

Then NPSAT1 radio frequency subsystem (RFS) is a full-duplex communication system providing 100 kbits

per second on both the uplink and downlink channels. The uplink channel operates at 1767.565 MHz and the downlink channel operates at 2207.3 MHz. The RFS uses in-house built patch antennae, one antenna for each frequency. The spacecraft has antennae pairs for both nadir-pointing and zenith-pointing capabilities which can be switched. Normally, only the nadir-pointing portion is used when the spacecraft is maintaining correct attitude. An asynchronous Gaussian minimum-shift keying FM is used for modulation. A maximum bit-error rate of 1x10-5 has been set as a system requirement.

The system uses a dual conversion to baseband with the first conversion at 140 MHz and the second at 10.7 MHz for the uplink channel. A Philips SA639 Mixer FM IF System performs the IF to baseband conversion.

The downlink channel uses an Analog Devices AD9852 direct digital synthesizer to modulate the serial data to a frequency modulated signal. There is a dual conversion up to the downlink RF channel. Both the uplink and downlink channels use a common local oscillator to achieve the RF to IF and IF to RF conversions.

5.5 Mechanical

The only moving parts of NPSAT1 are the separation system and the deployable booms, not including mechanical or magnetic latching relays. The NPSAT1 launch vehicle interface was designed for the Lightband separation system [8]. The mechanisms for the deployable booms are provided by NRL. The major mechanical subsystems are the structure and thermal design. Electronics housings are also mechanical in nature as is a great deal of the subsystem and system-level testing. The lithium-ion battery housing required detailed analysis to ensure that it would meet safety requirements, in particular a pressure capability of 3:1 of the normal operating pressure was shown and tested.

A mass simulator is required for NPSAT1, in addition to the flight vehicle, in the event that the spacecraft is not ready for integration and launch. As a secondary payload, NPSAT1 cannot impose any impact to the overall mission. The mass simulator is another mechanical subsystem in parallel development with the flight vehicle structure. The mass simulator is a simple three-piece structure which bolts together, but does not separate from the ESPA carrier.

5.5.1 Structures

The NPSAT1 flight vehicle structure successfully underwent qualification testing in September 2005 at the Naval Research Laboratory (NRL) in Washington, D.C. The structure is of aluminum 6061-T6 and, as shown in Fig. 3, consists of four equipment decks with side panels mounted to the decks and longerons that run vertically between the equipment decks. The side panels form four sides of the cylinder each on the lower section and three sides of the cylinder on the upper section.

The qualification program for the structure includes sine burst testing for static loads simulation to 15 g peak in each axis, followed by random vibration testing to +6 dB above the maximum predicted environment (MPE), or 14.2 g(rms) using an engineering development unit (EDU). Following this, the flight vehicle structure can undergo random vibration acceptance level testing at +0 dB of the MPE. The EDU was identical to the flight load-bearing structure with mass simulators of the electronics housings mounted to the structure. Measurements were taken at the four different mounting decks to gage the dynamic environment for the individual housings. Fig. 6 shows a photograph of the NPSAT1 EDU structure on the vibration shaker at NRL.

Figure 6. NPSAT1 EDU Vibration Test (Photo courtesy Naval Research Laboratory).

5.5.2 Thermal

The thermal design of the spacecraft is primarily a passive one. However, because the lithium-ion batteries have a narrow range of operations and the environment is expected to be on the colder side but within the range of military electronics, heaters are built into the battery housing. A detailed thermal analysis performed by Gruhlke [9], showed that five-Watt heaters are sufficient to maintain battery temperatures to within acceptable temperature limits.

5.6 CERTO and Langmuir Probe

The coherent electromagnetic radiotomography experiment and Langmuir probe are experiments provided by the Naval Research Laboratory Plasma Physics Division. A more detailed description of the experiment is given in [5]. The coherent electromagnetic radio tomography (CERTO) experiment is a radio beacon that transmits at 150, 400 and 1067 MHz. Working with a network of ground receivers, the CERTO beacon will be used to measure the integrated electron density of the ionosphere in the plane of observation. CERTO will also be used to develop and test tomographic algorithms for reconstruction of ionospheric irregularities; to provide a database for global models of the ionosphere; to characterize the ionosphere for geolocation; and to perform scintillation studies of the ionosphere. The Langmuir probe will be operated to collect on four separate 12-bit A/D channels at sample rates between 1 and 1000 samples per second. The Langmuir probe provides in-situ measurements at the spacecraft altitude where the data can be processed for correlation with the ground observations of the CERTO beacon.

5.7 Configurable, Fault-Tolerant Processor Experiment (CFTP)

The CFTP experiment will test the use of a FPGA-based processor board to implement a flexible, triple-modular, redundant (TMR) computer architecture for reliable computing for space applications. Single event effects (SEE) are detected and corrected through voting logic without the need to reboot the processor. The CFTP is used to investigate different fault-mitigation techniques to detect and correct a single-event upset (SEU) before they become functional errors. Recent work included ground-based radiation testing [10] of the CFTP board, and investigations into configuration memory errors and mitigation techniques through implementation of triple-modular redundancy [11].

The heart of the CFTP circuit board consists of two Xilinx XCV600 FPGA devices. Each FPGA is capable of implementing a stand-alone processing unit. Direct communication to the ARM processor is via the 16-bit wide PC/104 interface. Upon reset, the CFTP automatically configures its master FPGA to implement a PC/104 controller. Indirectly, the master XCV600 device can be programmed from the ARM via the JTAG interface. This JTAG manipulation allows the master device to be reprogrammed from its original configuration. The master device is capable of orchestrating reconfigurations of the second FPGA.

5.8 Solar Cell Measurement System (SMS)

The SMS will investigate both a new type of triple-junction solar cell as well as the experiment control hardware which will be used to construct the current versus voltage (IV) plots. The IV curves are the means of characterizing solar cells. Most notable are the closed-circuit current, open-circuit voltage, and maximum power points. As stated earlier, one of three solar panels on each of the 12 sides of the NPSAT1 cylindrical sides is made up of experimental cells. On each of the experimental panels, two cells are exclusively used for IV-curve testing. In addition to the IV curve data, the cell temperatures and the sun vector are recorded and time-stamped.

The sun sensors used for the SMS are the Goodrich 13-515 Sun Sensing Module. These are single-axis sun sensors with a field-of-view of ±64°. Two sensors are co-located with one rotate 90° to provide both the azimuth and elevation angles with respect to the spacecraft. With each sun sensor pair viewing 128°, a minimum of three pairs are required for a full 360° view in azimuth. LtJG Steffen Schenkel, (German Armed Forces) most recently worked on the sun sensors as part of his Studienarbeit. Schenkel was responsible for the final procedures for assembly and calibration of the sun sensor. Fig. 7 shows the calibration of the sun sensor under a solar simulator. The sun sensors will be used to select the pair of solar cells best meeting the illumination criteria for the IV curve data acquisition.

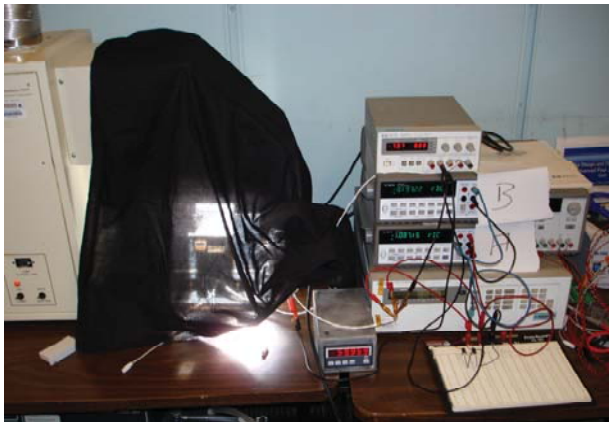


Figure 7. Sun Sensor Calibration.

5.9 Micro-Electromechanical Systems (MEMS) Rate Sensor

The MEMS rate sensor is a three-axis rate sensor using three BEI QRS11 devices mounted orthogonally. Each device has seven pins for power, rate output, as well as a built-in test. The sensor assembly fits within a sealed housing that is purged with dry nitrogen. In addition, filters are needed to ensure good signal quality of the low-voltage outputs. A non-flight sensor was calibrated by CPT(P) Tom Pugsley (U.S. Army) who also performed random vibration testing on the device. The flight assembly is followed up by another officer student, LtCol(S) C. J. Didier (USAF). Fig. 8 shows the calibration of the flight sensor assembly.

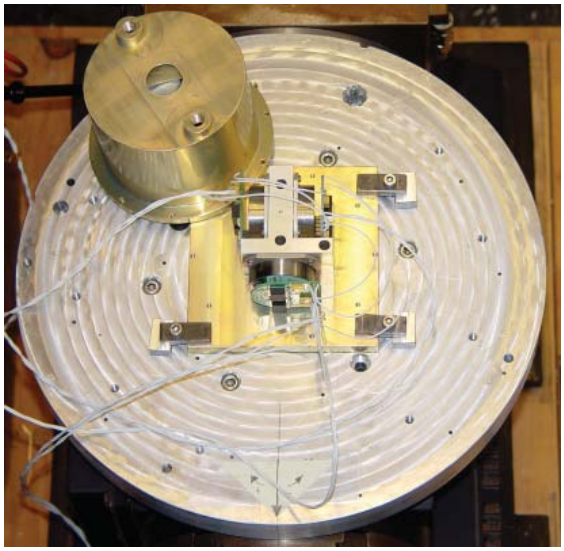


Figure 8. MEMS Rate Sensor Calibration.

5.10 Visible Wavelength Imager (VISIM)

The VISIM experiment is a color digital camera that is used primarily as a data generator for the CFTP experiment and for an educational outreach for kindergarten through 12th grade students to foster interest in aerospace studies. The VISIM consists of two components, the camera controller and the camera head. The camera controller is a PC/104 single board computer running the Linux operating system attached a the camera controller board and a power supply card. The VISIM controller receives commands from and sends its image data to the command and data handling (C&DH) subsystem. The C&DH orchestrates the operation of the VISIM experiment, even to the point of powering it on via commands to the EPS. The C&DH also sets parameters for image taking, such as gain, bias, and exposure. The camera head is an Electrim EDC-1000E. The optics selection was performed by Lt. Dustin Büttner (GAF) [12] as part of his Studienarbeit. Büttner also followed up his work on the optics with a determination through thermal-vacuum testing that the proposed shutter was potentially very risky [13]. The shutter was intended to mitigate the risk of damage to the camera in the event it was staring at the sun. The decision was made to remove the shutter.

6. CONCLUSIONS

The NPSAT1 small satellite offers NPS space systems officer students excellent engineering and operations opportunities in a space system development. Experience is attained by applying the knowledge gained through their course work toward real-life problems. Educational objectives are already met with each officer student involved in the project.

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